논문 2012-49-12-20

RF MOSFET을 위한 SPICE 기판 모델의 스케일링 정확도 분석

(Scaling Accuracy Analysis of Substrate SPICE Model for RF MOSFETs)

이 현 준*, 이 성 현**

(Hyun-Jun Lee and Seonghearn Lee)

요 약

RF 직접 추출 방법을 통해 얻은 정확한 MOSFET 기판 파라미터를 이용하여 기판저항만을 가진 BSIM4 모델은 스케일링 부정확성 때문에 넓은 영역의 게이트 길이에 적용하기에는 물리적으로 맞지 않다는 것이 증명됐다. BSIM4의 비물리적인 문제점을 제거하기 위해서 추가적인 유전체 기판 캐패시터를 가진 수정된 BSIM4 모델이 사용되었고, 이 모델의 물리적 타당성은 우수한 게이트 길이 scalability를 관찰함으로써 증명되었다.

Abstract

Using accurate MOSFET substrate parameters obtained by a RF direct extraction method, it is demonstrated that a BSIM4 model with only substrate resistances is not physically valid to apply in the wide range of gate length because of scaling inaccuracy. In order to remove the unphysical problem of the BSIM4, a modified BSIM4 model with additional dielectric substrate capacitance is used and its physical validity is verified by observing excellent gate length scalability.

Keywords : MOSFET, RF, Modeling, SPICE model, substrate model, scalable model, parameter extraction

Ⅰ. INTRODUCTION

For the accurate SPICE RF circuit simulation, the Berkeley short-channel IGFET model 4 (BSIM4) has been widely recognized as a standard MOSFET model[1]. Since substrate modeling becomes quite important in designing output matching circuits for RF ICs[2~3], BSIM4 provides a flexible substrate model with resistance network. Generally, a scalable SPICE RF model in the wide range of the gate length L_g should be developed to apply for a wide use of RF IC design, but a scaling validity of the BSIM4 substrate resistance model with regard to L_g in the high frequency region has not been reported yet.

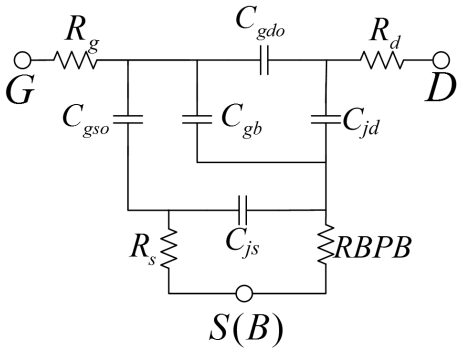
Therefore, in this paper, a scaling accuracy of the BSIM4 substrate model in terms of L_g is physically analyzed in detail. The modified BSIM4 substrate model is proposed to improve the L_g scaling accuracy in the high frequency region.

* 학생회원, ** 정회원, 한국외국어대학교 전자공학과
(Department of Electronics Engineering, Hankuk University of Foreign Studies)
※ 이 연구는 2012학년도 한국외국어대학교 교내학술연구비의 지원에 의하여 이루어진 것임.
접수일자: 2012년7월17일, 수정완료일: 2012년11월26일

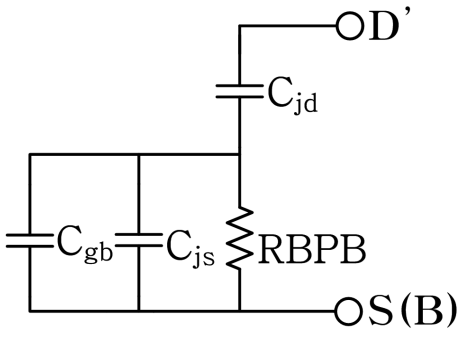
Ⅱ. EXTRACTION AND ANALYSIS

S-parameters are measured on multi-finger N-MOSFETs (unit finger width W_u=5㎛ and the number of gate finger Nf=16) with different L_g of 0.13㎛, 0.18㎛ and 0.25㎛. An accurate de-embedding procedure was carried out to remove pad and interconnection parasitics from each measured S-parameters[4].

Since a five substrate resistance network in BSIM4 is too complex to be directly determined, a simple substrate model with single resistance[5] is generally used. Fig. 1(a) shows an AC equivalent circuit of the simple BSIM4 model with the substrate resistance $RBPB$ at V_{gs}=0V. The substrate equivalent circuit of Fig. 1(b) is defined by $Y_{22}^d + Y_{12}^d$ of Fig. 1(a) for $RBPB \gg R_s$ and R_g, where Y^d-parameters are obtained by subtracting the drain resistance R_d from measured S-parameters. Fig. 1(b) is represented by the simple circuit block of the parallel resistance R_p and capacitance C_p. Using the direct method[6], R_d is extracted from y-intercepts of high-frequency $Real(Z_{22} - Z_{12})$ versus ω^{-2} at V_{gs}=0V.



(a)



(b)

그림 1. (a) 단일 기판저항을 사용한 단순 BSIM4 모델의 AC 등가회로(V_{gs}=0V)
(b) $Y_{22}^d + Y_{12}^d$의 기판 등가회로

Fig. 1. (a) The AC equivalent circuit of a simple BSIM4 model with a single substrate resistance (V_{gs}=0V)
(b) The substrate equivalent circuit of $Y_{22}^d + Y_{12}^d$.

To extract R_p and C_p accurately, an RF direct method[7] is performed using the following equations derived from Fig. 1(b):

$$R_p = \frac{1}{Real(1/Z_s)} \tag{1}$$

$$C_p = (1/\omega)Imag(1/Z_s) \tag{2}$$

where

$$Z_s = \frac{1}{Y_{22}^d + Y_{12}^d} - \frac{1}{j\omega C_{jd}} \tag{3}$$

As shown in Fig. 2, the drain junction capacitance C_{jd} in (3) is extracted by the following equation derived from Fig. 1(b) at low-frequencies (LF):

$$C_{jd} \approx (1/\omega)Imag(Y_{22}^d + Y_{12}^d)_{LF} \tag{4}$$

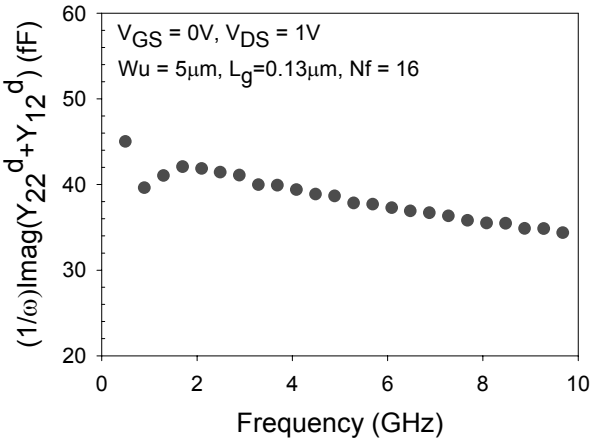


그림 2. 주파수에 따른 측정된 $(1/\omega)Imag(Y_{22}^d + Y_{12}^d)$

Fig. 2. Measured data of $(1/\omega)Imag(Y_{22}^d + Y_{12}^d)$ versus frequency.

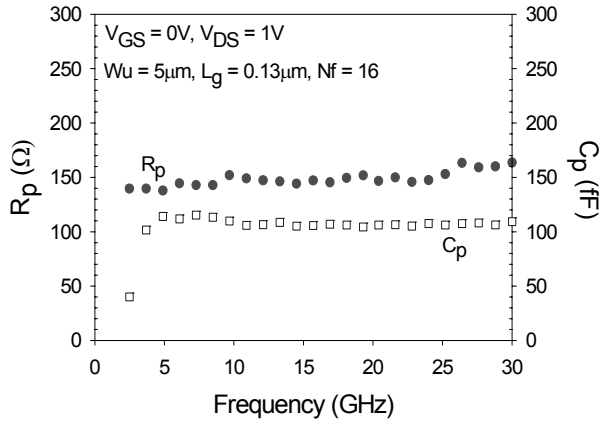


그림 3. 주파수에 따른 추출된 R_p와 C_p
Fig. 3. Extracted data of R_p and C_p versus frequency.

This direct extraction method for R_p and C_p is much simpler than the previous ones using two different data in the high and low frequency region[8]. The extracted values of R_p and C_p seem to be frequency-independent up to 30 GHz as shown in Fig. 3, verifying the extraction accuracy.

In a simple BSIM4 model of Fig. 1(a), $R_p = RBPB$ and $C_p = C_{gb} + C_{js}$, where C_{gb} is the gate-bulk capacitance and C_{js} is the source junction capacitance. The value of C_{gb} is extracted at V_{ds} =0 using low-frequency data of the following equation[9].

$$C_{gb} \approx (1/\omega) Imag(Y_{11} + 2Y_{12})_{LF} \quad (5)$$

As shown in Fig. 4(a), the extracted values of C_{gb} increase linearly as a function of L_g. Using (2) and (5), C_{js} data are extracted by $C_p - C_{gb}$ and plotted as a function of L_g in Fig. 4(b). Theoretically, as L_g is longer, C_{gb} increases but C_{js} is unchanged. However, the extracted C_{js} data show an abrupt decrease with increasing L_g which is not physically acceptable. This unphysical extraction of C_{js} indicates that the simple substrate model in Fig. 1(a) is invalid. Even if five substrate resistances offered in BSIM4 are fully used, this

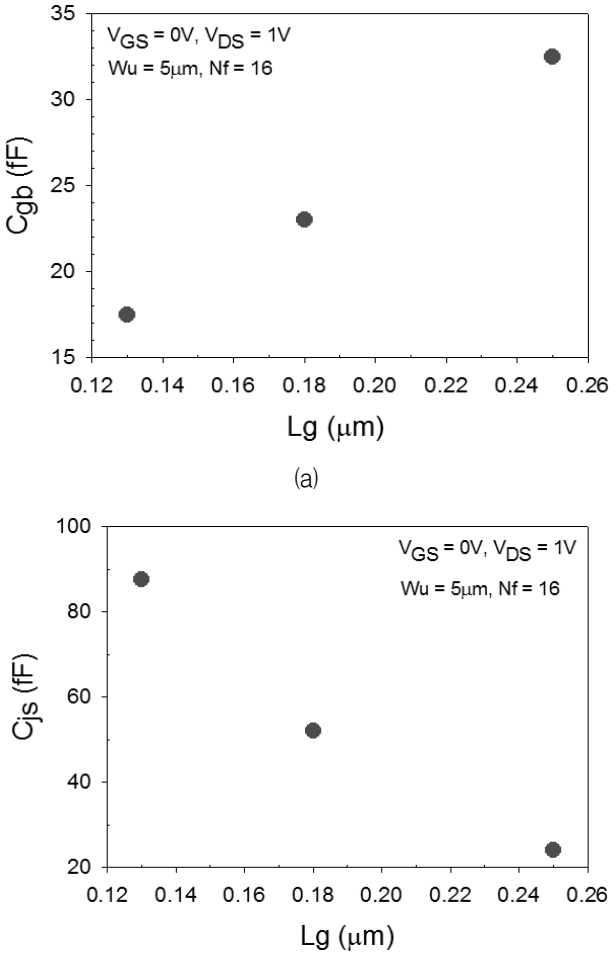


그림 4. (a) C_{gb} 대 L_g의 추출 데이터
(b) C_{js} 대 L_g의 추출 데이터
Fig. 4. (a) Extracted data of C_{gb} versus L_g
(b) Extracted data of C_{js} versus L_g.

unphysical scaling problem of C_{js} extraction still occurs, because of the connection of these resistances to C_{js}.

In order to avoid this unphysical scaling problem of C_{js} vs. L_g in Fig. 4(b), we propose a modified BSIM4 model that includes parallel substrate capacitances(C_{subd}, C_{subs})[2~3, 8] to represent a lossy dielectric Si substrate region in Fig. 5(a). Also, the substrate equivalent circuit of Fig. 5(b) is defined by $Y_{22}^d + Y_{12}^d$ of Fig. 5(a) at V_{gs}=0V.

R_{subd} and C_{subd} are extracted by (1) and (2), respectively. In Fig. 6, extracted R_{subd} values are

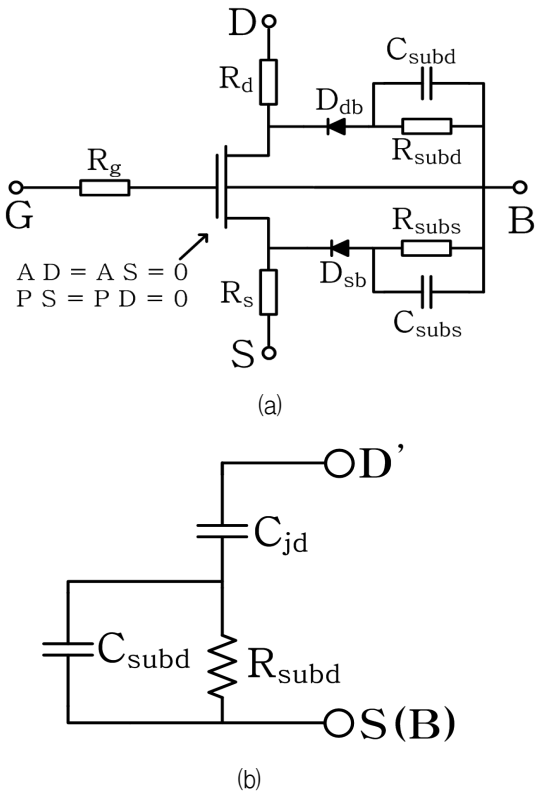


그림 5. (a) 손실 유전체 기판회로를 사용한 수정된 BSIM4 Macro 모델. 내부 소스와 드레인 접합 다이오드를 제거하기 위해 AD=AS=PD=PS=0로 놓음.
(b) $Y_{22}^{d}+Y_{12}^{d}$의 기판 등가회로

Fig. 5. (a) Modified BSIM4 Macro model using a lossy dielectric substrate circuit. AD=AS=PD=PS=0 is set to remove internal source and drain junction diodes.
(b) The substrate equivalent circuit of $Y_{22}^{d}+Y_{12}^{d}$.

proportional to L_g, while C_{subd} values are inversely proportional to L_g. This L_g scalability is physically valid because the MOSFET lossy substrate region between the drain and bulk contacts is shown to be longer with increasing L_g[3]. This verifies the L_g scaling accuracy of the lossy dielectric substrate model in Fig. 5(a).

Fig. 7 shows AC equivalent circuits of the simple and modified BSIM4 models in the saturation region. In order to extract other intrinsic model parameters directly without any optimization, the equivalent circuits without C_{js} neglected in the low frequency

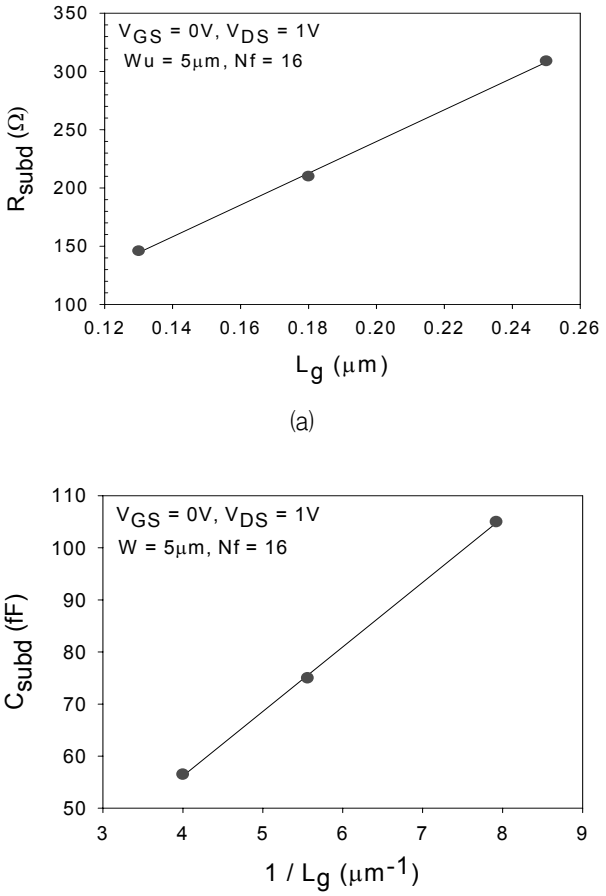


그림 6. (a) R_{subd} 대 L_g 추출 데이터와 피팅 선
(b) C_{subd} 대 1/L_g 추출 데이터와 피팅 선

Fig. 6. (a) Extracted data and fitting line of R_{subd} vs. L_g
(b) Extracted data and fitting line of C_{subd} vs. 1/L_g

region are used to derive the following equations[8, 10].

$$C_{gs}=(1/\omega)Imag(Y_{11}^{i}+Y_{12}^{i}) \tag{6}$$

$$C_{gd}=(-1/\omega)Imag(Y_{12}^{i}) \tag{7}$$

$$r_{ds}=1/Real(Y_{22}^{i}) \tag{8}$$

$$g_{mo}= \quad Y_{21}^{i}-Y_{12}^{i} \tag{9}$$

where Y^{i}-parameters of the intrinsic MOSFET are obtained by subtracting C_{jd}, substrate parameters,

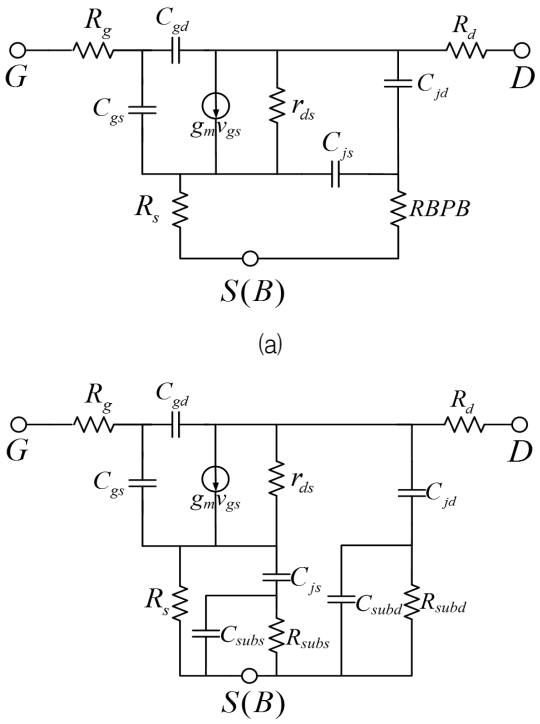


그림 7. 포화영역에서 BSIM4 모델의 AC 등가회로 ($g_m = g_{mo}e^{-j\omega\tau}$)
(a) 단순 모델, (b) 수정 모델

Fig. 7. AC equivalent circuit of BSIM4 model in the saturation region.
(a) Simple model (b) Modified model

R_s and R_g from measured Y^d-parameters. Using the direct method[6], R_g and R_s are extracted from y-intercepts of high-frequency $Real(Z_{11}-Z_{12})$ and $Real(Z_{12})$ versus ω^{-2} at V_{gs}=0V, respectively.

In Fig. 8, the scaling accuracy of a modified BSIM4 model in Fig. 7(b) is reconfirmed by finding better agreement between measured and modeled S_{22} -parameter than a simple one of Fig. 7(a) at L_g= 0.25㎛.

Ⅲ. CONCLUSIONS

RF MOSFET substrate parameters are accurately extracted using a RF direct method. The original BSIM4 model with only substrate resistances is proved to be physically unacceptable for the L_g scaling. The L_g scaling accuracy of a modified BSIM4 model including the dielectric substrate capacitance is justified by observing the physical validity that R_{subd} and C_{subd} in a lossy dielectric substrate is proportional to L_g and $1/L_g$, respectively. The simulated S-parameters of the modified BSIM4 model have better agreements with

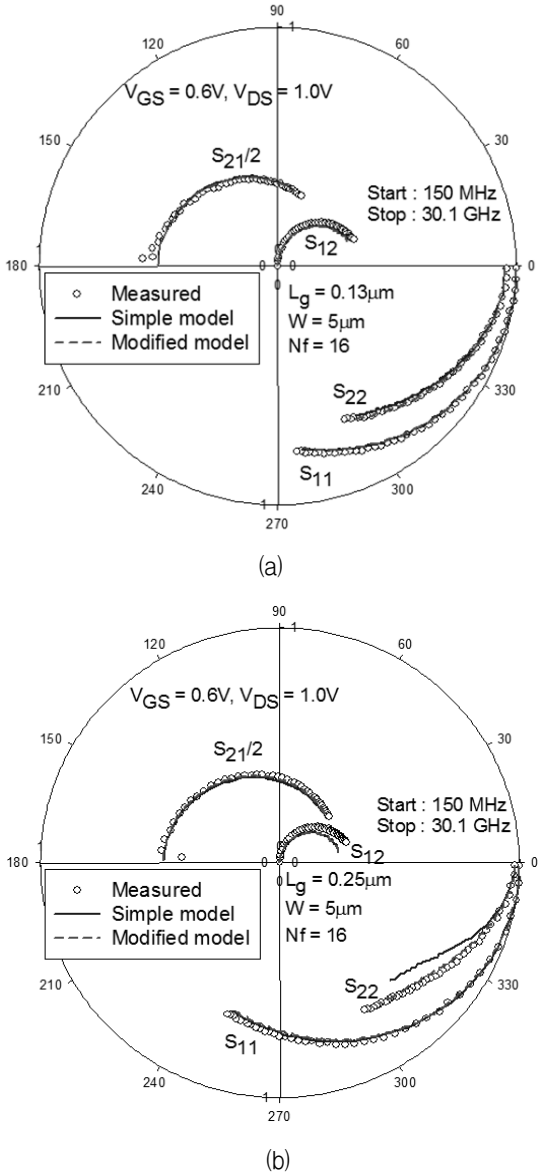


그림 8. 측정데이터와 비교된 단순 모델과 수정 모델의 S-파라미터 데이터
(a) L_g=0.13㎛ (b) L_g=0.25㎛

Fig. 8. S-parameters of simple and modified models compared with measured data.
(a) L_g=0.13㎛ (b) L_g=0.25㎛

measured ones than a simple BSIM4 model, verifying the scaling accuracy of its model.

참 고 문 헌

[1] BSIM4 Manual, Department of Electrical Engineering and Computer Science, University of California, Berkeley, 2001.

[2] S. Lee, C. S. Kim, and H. K. Yu, "A small-signal RF model and its parameter extraction for substrate effects in RF MOSFETs," IEEE Trans. Electron Devices, vol. 48, pp. 1374-1379, July 2001.

[3] 이용택, 최문성, 구자남, 이성현, "Deep Submicron MOSFET 기판회로 파라미터의 바이어스 및 게이트 길이 종속 데이터 추출," 전자공학회 논문지 제 41권 SD편 제 12호, pp. 27-34, 2004.

[4] J. Cha, J. Cha, and S. Lee, "Uncertainty analysis of two-step and three-step methods for deembedding on-wafer RF transistor measurements," IEEE Trans. Electron Device, Vol. 55, pp. 2195-2201, 2008.

[5] S. Lee and H. K. Yu, "A semianalytical parameter extraction of a SPICE BSIM3v3 for RF MOSFET's using S-parameters," IEEE Trans. Microwave Theory Tech., vol. 48, pp. 412-416, March 2000.

[6] S. Lee, "Accurate RF extraction method for resistances and inductances of sub-0.1 μm CMOS transistors", Electronics Letters, Vol. 41, No. 24, pp. 1325-1327, 2005.

[7] 이현준, 이성현, "소신호 MOSFET 등가회로의 기판 파라미터 직접 추출 방법," 대한전자공학회 2012년 하계종합학술대회, pp. 130-131, 2012.

[8] S. Lee, "Direct extraction technique for a small-signal MOSFET equivalent circuit with substrate parameters," Microw. Opt. Technol. Lett, vol. 39, no. 4, pp. 344-347, 2003.

[9] J.-Y. Kim, B.-H. Ko, M.-K. Choi, and S. Lee, "RF extraction method for source/drain overlap and depletion length of deep-submicron RF MOSFETs using intrinsic gate-bulk capacitance," Electron. Lett., vol. 46, no. 23, pp. 1566-1568, 2010.

[10] 최민권, 김주영, 이성현, "새로운 파라미터 추출 방법을 사용한 Multi-Finger RF MOSFET의 기판 모델 정확도 비교," 전자공학회 논문지 제 49권 SD편 제 2호, pp. 9-14, 2012.

저 자 소 개

이 현 준(학생회원)

2012년 한국외국어대학교 전자공학과 학사 졸업.

2012년～현재 한국외국어대학교 전자정보공학과 석사과정.

<주관심분야 : RF CMOS 소자 모델링>

이 성 현(정회원)-교신저자

1985년 고려대학교 전자공학과 학사 졸업.

1989년 미국 University of Minnesota 전기공학과 석사 졸업.

1992년 미국 University of Minnesota 전기공학과 박사 졸업.

1992년～1995년 한국전자통신연구원 선임연구원

1995년～현재 한국외국어대학교 전자공학과 교수

<주관심분야 : CMOS 및 바이폴라 소자 모델링>