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Dual Sampling-Based CMOS Active Pixel Sensor with a Novel Correlated Double Sampling Circuit

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Abstract

In this paper, we propose a 4-transistor active pixel sensor(APS) with a novel correlated double sampling(CDS) circuit for the purpose of extending dynamic range. Dual sampling techniques can overcome low-sensitivity and temporal disparity problems at low illumination. To accomplish this, two images are obtained at the same time using different sensitivities. The novel CDS circuit proposed in this paper contains MOS switches that make it possible for the capacitance of a conventional CDS circuit to function as a charge pump, so that the proposed APS exhibits an extended dynamic range as well as reduced noise. The designed circuit was fabricated by using 0.35 ㎛ 2-poly 4-metal standard CMOS technology and its characteristics have been evaluated.

Keywords : Dual Sampling, APS, Noise, Charge Pump

1. INTRODUCTION

Complementary metal oxide semiconductor(CMOS) image sensors(CIS) have a wide range of applications from consumer applications and machine vision applications to scientific research applications[1]. Some challenging issues in CIS are noise and dynamic range(DR), which are defined as the ratio of a pixel's saturation level to its signal threshold, decided based on noise level. Noise and DR are important parameters in determining the performance of CIS. Various approaches have been proposed to reduce noise and extend DR, based on various approaches such as linear-logarithmic CIS, multiple sampling, overflow integration capacitor and dual sampling[2-15]. These approaches, however, suffer from variously noise, nonlinearity, lower sensitivity, reduced operating speed, and lower resolution. Logarithmic sensors may greatly widen the dynamic range in the high illumination region by compressing the image signal, but they suffer from noise problems in the low illumination region. In the case of linear-logarithmic sensors, linear sensors compensate for this problem. Although the problems in low illumination can be compensated for, the nonlinearity problem of logarithmic sensors still exists. Multiple sampling combines several images with different light integration times. Generally, an image that has a long light integration time shows good quality in the dark area of the incident scene but leaves the bright areas saturated. A short light-integrated image can compensate for this deficiency. Since this technique samples the amount of photo generated electrons just before saturation, not only dynamic range but also signal-to-noise ratio(SNR) is improved. However, this approach requires a high frame rate readout for a wide dynamic range. Many researchers have tried to control the amount of accumulated charge. For this purpose, charges in highly illuminated pixels are partially transferred to a small capacitor via a switch. As this approach requires a capacitor and a switch, its pixel size is larger than standard. Dual- and multi-sampling based on analog or digital techniques has been widely researched for obtaining images with different sensitivities. However, the additional time requirements for the additional charge accumulation induces low sensitivity and time disparity among two or more of the light-integration periods, this induces image distortion. This paper suggests a new approach to dual sampling with a novel CDS circuit to overcome the low sensitivity, temporal disparity, and noise[16]. To accomplish this, two images are obtained at the same time and these obtained images have different sensitivities.

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Additionally, the proposed CDS circuit contains MOS switches that makes it possible for the capacitance of a conventional CDS circuit to function as a charge pump, which can reduce noise and extend dynamic range[17]. The designed circuit was fabricated by using 0.35 ㎛ 2-poly 4-metal(2P4M) standard CMOS technology and tested in order to evaluate the feasibility of the proposed technique.

2. CIRCUIT DESIGN

2.1 Operational principle

Figure 1 and 2 show a schematic diagram of the proposed 4-transistor APS with a novel CDS circuit and a timing diagram for operation, respectively. Figure 3 shows the layout of the proposed APS array. The proposed CDS circuit has two functions: to increase the reset voltage and to reduce fixed pattern noise(FPN). The sequence of operation runs as follows: First, the charge pump sharing C_{sig} of the CDS circuit increases the gate voltage of the transistor M_1 from t_1 to t_3, as shown in Fig. 2, which results in an increase of the reset voltage of Nint(the charge accumulation node). This increased reset voltage helps to extend the dynamic range of the APS, which is confirmed by the data for the proposed mixed output voltage as shown in Fig. 4. Second, the FPN is reduced by the mechanism of correlated double sampling from t_2 to t_6 as shown in Fig. 2[18]. The proposed 4-transistor APS sequentially performs resets of the photodiodes(both high- and low-sensitivity photodiodes), accumulating signal charge and combining all the signals of both photodiodes. The reset operation is performed by turning on the transistor M_1 using the function of the charge pump. The energy level of the two photodiodes is set at the increased reset voltage, which extends the dynamic range, as shown in Fig. 4. During that period, the transistor M_{14} is also turned on to reset both photodiodes. M_1 and M_{14} are turned off after resetting, when photo-generated charges are simultaneously accumulated in both photodiodes. The charge accumulation rates(or quantum efficiencies) of these two photodiodes are different; therefore, the high- and low-sensitivity photodiodes produce long- and short-time exposed images of a conventional multi-sampling approach. After a certain period of charge accumulation, transistor M_{14} is turned on. During that time, an image combining operation is performed. This indicates an improvement of dynamic range at high illumination exhibiting the mixed output voltage seen in Fig. 4. In a state of low-illumination, both photodiodes cannot be fully charged; therefore, the APS sends the combined signal from both the photodiodes. In a state of relatively high-illumination, however, the high-sensitivity photodiode is fully charged. In that case, the APS shows lower sensitivity characteristics compared with the result obtained in a state of low-illumination. The illumination level for saturation is determined by the low-sensitivity photodiode.

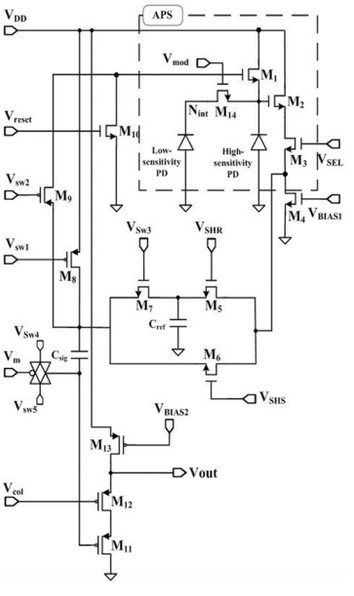


Fig. 1. Proposed APS with a novel noise reduction circuit.

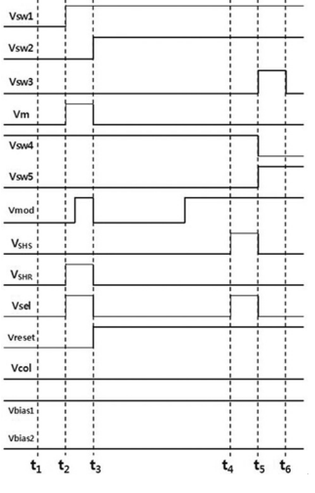


Fig. 2. Timing diagram of the proposed APS.

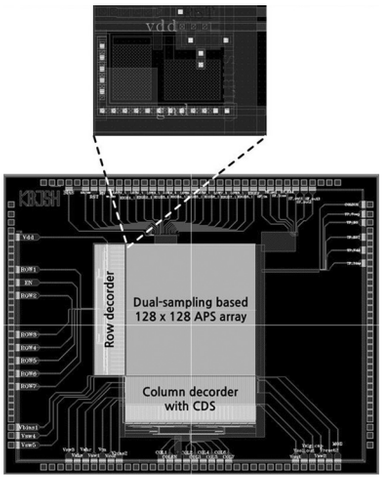
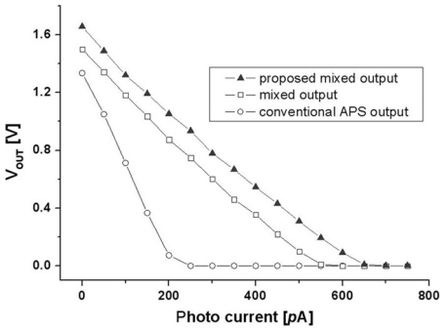
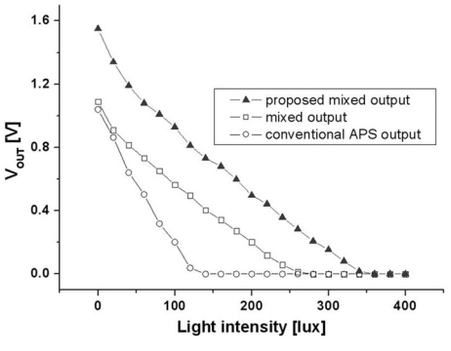


Fig. 3. Layout of the proposed APS array.



(a)



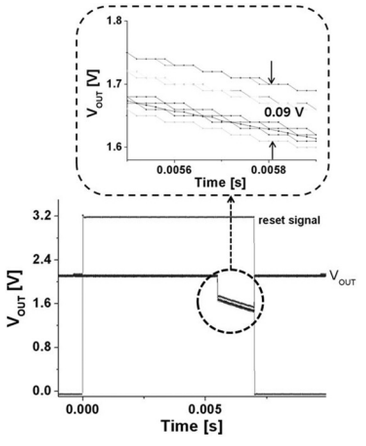
(b)

Fig. 4. Variation of the output voltage with photo current and light intensity. (a) Simulation results, (b) experimental results.

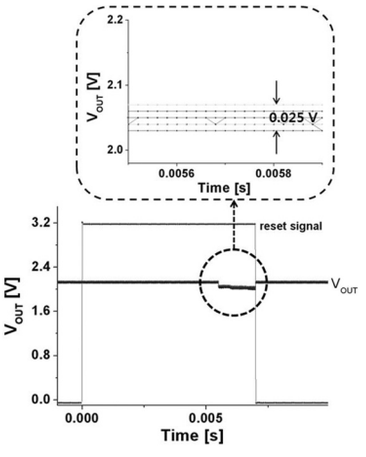
Figure 5 shows the output voltage of the APS. The noise reduction ratio of the proposed CDS circuit is obtained by measuring the variation of the APS output voltage for ten pixels when the same light is incident on the entire array of the proposed image sensor. Figures 5 (a) and (b) show the variation of the output voltage(0.09 V) without the CDS circuit and the variation of the output voltage(0.025 V) with the CDS circuit, respectively. These result indicates that the noise is reduced by approximately 70 % with the CDS circuit.

3. DISCUSSION

Compared to previously reported APS and CDS circuits, the proposed approach has several advantages. The proposed sensor performs the combination of two images by turning on the internal transistor M_{14}; therefore, external equipment and digital signal processing are not required. All that is needed is a simple pulse signal.



(a)



(b)

Fig. 5. Output voltage of the APS. (a) Without the CDS circuit, (b) with the CDS circuit.

The two photodiodes in the proposed APS operate simultaneously unlike in other conventional multiple sampling techniques; therefore, no extra time is needed for additional charge accumulation. DR extension is adjustable by controlling parasitic capacitance and the sensitivity of both photodiodes.

In addition, charge accumulation times for both photodiodes are the same, as such, they are free from the temporal disparity problem. An expected drawback of the proposed APS is the increase of pixel size, which could be minimized by applying a stacked photodiode structure[19]. The output voltage of the APS can be decreased by using a reduced supply voltage resulting from the scaling down of the semiconductor process. The proposed CDS circuit can not only extend the dynamic range while reducing noise but also mitigates a decrease in output voltage. Due to these advantages, this technique can be applied to CMOS image sensors with a global shutter method that requires a few μs for the charge pump to function before noise reduction.

4. CONCLUSIONS

A dual sampling 4-transistor APS with a novel CDS circuit was designed and fabricated using 2-poly 4-metal standard CMOS technology. Compared to previously reported APS with CDS circuits, the proposed circuit has several advantages: no-external equipment or signal processing for combining images is required, no-additional time-requirement for additional charge accumulation is needed, it has adjustable DR extension and no temporal disparity. Experimental results agree well with simulation results. From the simulation and experimental results, we can say the proposed 4-transistor APS with a novel CDS circuit can not only extend dynamic range but also reduce noise. As such this technique can be applied to the CMOS image sensors with a global shutter method.

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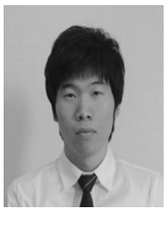

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