Journal of Sensor Science and Technology
Vol. 21, No. 1 (2012) pp. 1-6
http://dx.doi.org/10.5369/JSST.2012.21.1.1
pISSN 1225-5475/eISSN 2093-7563

Current-to-Voltage Converter Using Current-Mode Multiple Reset and its Application to Photometric Sensors

Jae-Hyoun Park+ and Hyung-Do Yoon

Abstract

Using a current-mode multiple reset, a current-to-voltage(I-V) converter with a wide dynamic range was produced. The converter consists of a trans-impedance amplifier(TIA), an analog-to-digital converter(ADC), and an N-bit counter. The digital output of the I-V converter is composed of higher N bits and lower bits, obtained from the N-bit counter and the ADC, respectively. For an input current that has departed from the linear region of the TIA, the counter increases its digital output, this determines a reset current which is subtracted from the input current of the I-V converter. This current-mode reset is repeated until the input current of the TIA lies in the linear region. This I-V converter is realized using 0.35 ㎛ LSI technology. It is shown that the proposed I-V converter can increase the maximum input current by a factor of 2^N and widen the dynamic range by 6^N. Additionally, the I-V converter is successfully applied to a photometric sensor.

Keywords : Current-to-Voltage Converter, Current-Mode Multiple Reset, Trans-Impedance Amplifier, Dynamic Range

1. INTRODUCTION

In general, current-to-voltage(I-V) converters are one of the core circuits in current-mode systems or amperometric sensors. An I-V converter has several requirements such as low noise, wide dynamic range(DR), linearity, high speed, low power dissipation, and small occupation area[1-3]. Particularly in optical sensors, an I-V converter with a wide dynamic range(DR) is often required because of a large span of light intensity levels between moonless dark nights and direct sunlight. It is well known that the human visual system exhibits an optical DR of about 200 dB, but commercial artificial imagers, such as charge coupled devices(CCDs) and complementary metal-oxide-semiconductor(CMOS) image sensors, have a DR of at most 70 dB[4-7]. For this reason, many studies and experiments have been carried out in order to produce an optical sensing system with a wide DR[2-7].

There are several possible methods to help achieve a wide DR. Multiple or locally adaptive exposure processes have been widely used in CMOS image sensors for automotive applications, which require a wide DR[4, 5]. These exposure processes are basically charge accumulation methods. Other approaches include logarithmic converters, which are commonly used for wide DR I-V converters. The logarithmic converters make use of the exponential current-voltage characteristics of metal-oxide-semiconductor field-effect transistors(MOSFETs). These characteristics are come from diffused current in the sub-threshold region of MOSFETs[6-9]. The former method shows good linearity, but the signal-to-noise ratio(SNR) is decreased or more complex circuitry is needed[3-5]. The latter method has simple circuitry and good conversion speed, but the signal conversion is non-linear or logarithmic[3, 6-8].

In this paper, a novel I-V converter using a current-mode multiple reset process is proposed. The converter consists of a trans-impedance amplifier(TIA), an analog-to-digital converter(ADC), and an N-bit up-counter. The proposed I-V converter shapes a large input current that has departed from the linear converting region by means of multiple current resets in order to achieve a wide DR without any degradation in linearity. This I-V converter was implemented using a 0.35 ㎛ 3.3 V CMOS process and was applied to a photometric sensor using a P-I-N photodiode.

2. CIRCUIT DESIGN

Korea Electronics Technology Institute
+Corresponding author: jhpark@keti.re.kr
(Received : Oct. 6, 2011, Accepted : Nov. 21, 2011)

The signal flow diagram of the proposed I-V converter is shown in Fig. 1. The principal idea behind this I-V converter is a current-mode multiple reset process using current subtraction. The operational procedure is as follows: When the input current of the I-V converter is higher than the maximum input value of the TIA used, the output voltage of the TIA is non-linear or saturated and, as such, is higher than the reference voltage VREF. If then, the integer variable k is increased by 1 or the N-bit binary counter is up-counted, a reset current proportional to k is generated. The current-mode reset process is performed by subtracting the reset current from the input current of the I-V converter and the current resulting from this subtraction is converted to voltage by the TIA. Until the output voltage of the TIA lies in the linear region of the TIA or is smaller than the reference voltage, these processes with the current-mode reset are repeated. Consequently, the N-bit counter has binary-weighted rough information about the input current of the I-V converter. Then, the output voltage of the TIA is digitized by the ADC. Finally, the digital output of the overall I-V converter consists of the outputs of the ADC as less significant bits and the outputs of the N-bit counter as more significant bits.

In order to verify the proposed I-V conversion algorithm, an I-V converter with a 12-bit digital output was designed using 0.35 ㎛ 2-poly 4-metal 3.3 V CMOS mixed-signal technology. The designed I-V converter consists of a linear TIA, a current-mode reset circuit using a current subtractor, a 2-bit up-counter with a reset current generator, and a 10-bit successive approximated ADC. A block diagram of the designed I-V converter is shown in Fig. 2.

A circuit diagram of the linear TIA is shown in Fig. 3, this basically consists of two pairs of transistors[3, 10]. One pair is a diode-connected n-type MOSFET, which is well-known to be a logarithmic converter in the sub-threshold region[6-8]. The other pair is a p-type common-source amplifier with a low voltage gain in order to linearize logarithmic converting characteristics. There are two bias current sources, I_{biasN} and I_{biasP}, in the designed TIA, as shown in Fig. 3. The I_{biasN} can determine the linearity and conversion gain of the TIA. We can remove the logarithmic characteristics of the diode-connected MOSFET in the sub-threshold region and shift a dark level by properly designing the I_{biasP}. Additionally, this TIA has a p-type source-follower as an output buffer.

The reset current generator consists of a comparator, a 2-bit up-counter, and a binary-to-thermometer decoder with a reference current source, as shown in Fig. 4. The comparator has the reference voltage V_{REF} as its negative input, this is the maximum non-saturated output voltage of the TIA and corresponds to the maximum linear input current of the TIA or the reference current I_{REF}. The positive input of the comparator is the output voltage of the TIA and the comparator output is connected to the input of the first J-K flip-flop of the 2-bit up-counter. The output, therefore, of the up-counter is increased by a binary 1 per clock until the comparator output is high or the TIA output is higher than V_{REF}. Actually, the TIA used has an output voltage that is inversely proportional to the input current, thus the comparator should be followed by a NOT-gate. On the other hand, the binary output of the up-counter is decoded to a thermometer code where the number of ones is equal to the integer k, and this thermometer code generates the reset current which is k times the I_{REF}.

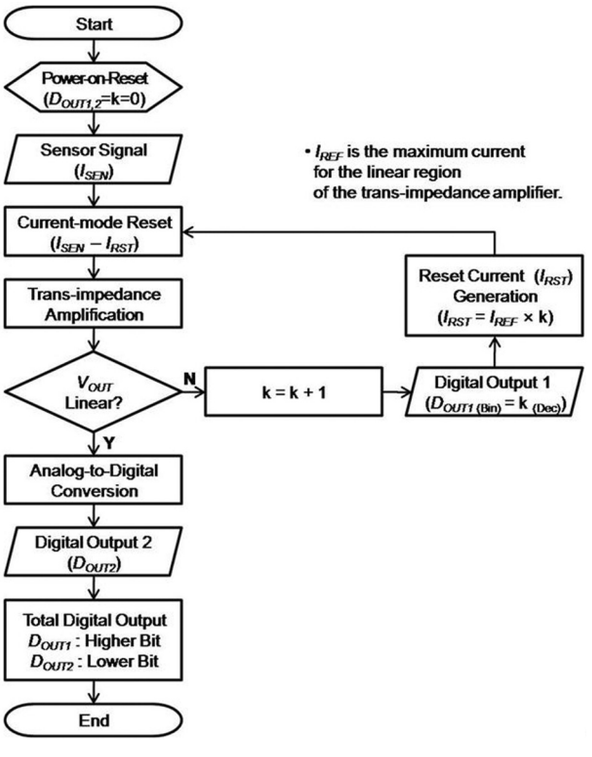


Fig. 1. Signal flow diagram of the proposed current-mode multiple reset algorithm for I-V conversion.

Using this generated reset current, the current-mode reset process is performed. That is, the reset current is subtracted from the input current of the I-V converter, and then the current resulting from the subtraction or the input current of the TIA is returned to zero or the initial value, this process is similar to a voltage or charge reset. Due to this,

the current subtraction is referred to as the current-mode reset process. This current subtraction is carried out using Kirchoff 's current law, which can be simply realized using current mirrors, as shown in Fig. 5. A cascade current mirror is used to prevent errors caused by the finite output impedance of the current mirror. Then, the current resulting from the subtraction is converted to an analog voltage by the TIA, which determines the comparator output. When the TIA output voltage is finally lies in the linear region of the TIA, the up-counter has a higher 2-bit output of the overall I-V converter and the TIA output voltage is converted to a lower 10-bit output of the overall I-V converter by the ADC.

At this point, let us appraise the effects of the proposed algorithm on the maximum input current or on the dynamic range. In the designed I-V converter, as a 2-bit up-counter is used, the integer k should be less than four and the maximum reset current is equal to $3I_{REF}$. The maximum linear input current of the I-V converter can be increased to $2^2 I_{REF}$. This can be generalized as an increase of the maximum input current by a factor of 2^N for an N-bit up-counter. Furthermore, the dynamic range can be widened to 6N without considering the signal-to-noise ratio, which is expected to improve owing to a dark level shift by the I_{biasP}.

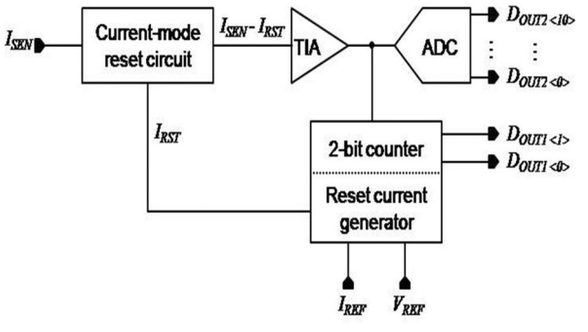


Fig. 2. Block diagram of the designed I-V converter.

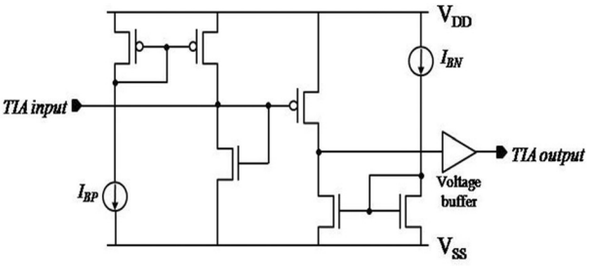


Fig. 3. Circuit diagram of the linear trans-impedance amplifier.

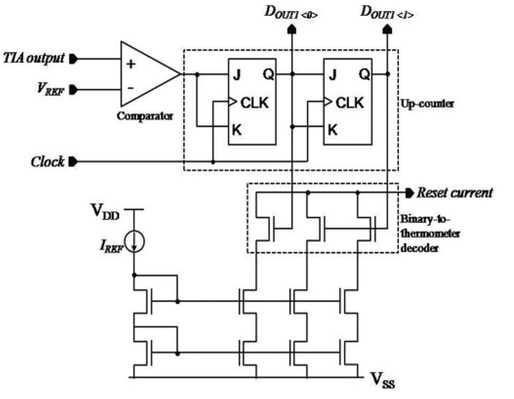


Fig. 4. Reset current generator using the up-counter and the binary-to-thermometer decoder.

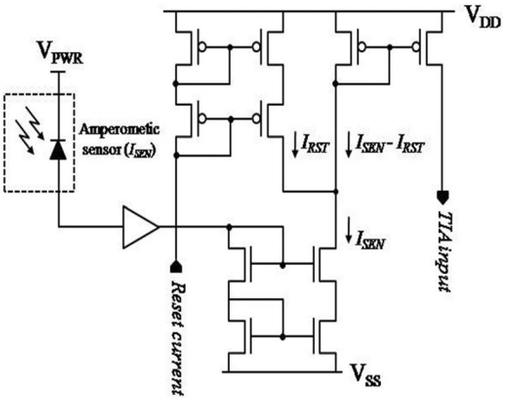
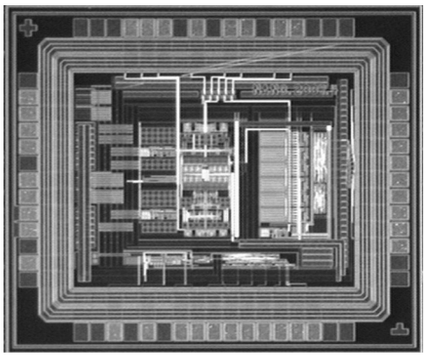


Fig. 5. Current-mode reset circuit using the current subtractor.

3. RESULTS AND DISCUSSIONS

We fabricated the designed I-V converter using a 0.35 ㎛ CMOS process and packaged the fabricated I-V converters using 48-pin quad flat packages. Photographs of the fabricated bare chip and the packaged chip are shown in Fig. 6. The completed I-V converter has been tested using an evaluation system with a P-I-N photodiode, as shown in Fig. 7, in order to verify its applicability to optical sensing systems. When we precisely tested the I-V conversion characteristics of the TIA and the I-V converter, the input current of the evaluation system was supplied by a programmable constant current source instead of the PIN photodiode. The analog output voltages are probed using an oscilloscope and the digital outputs are indicated by several Light Emitting Diodes(LEDs) on the evaluation system.



(a) bare chip

(b) packaged chip

Fig. 6. Photograph of the fabricated I-V converter chip.

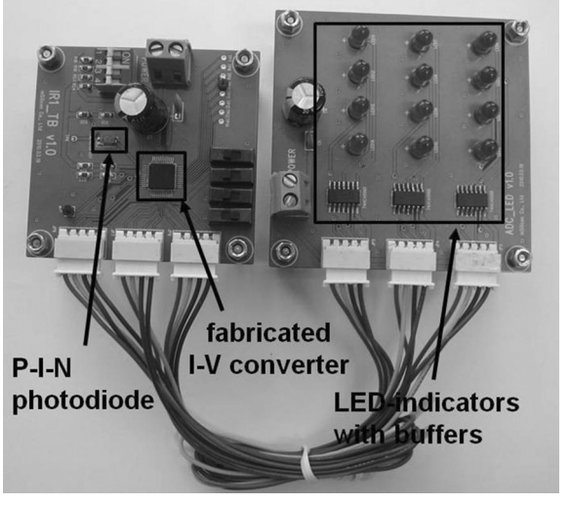


Fig. 7. Photograph of the evaluation system.

Most of all, the I-V conversion characteristics of the TIA alone should be exactly obtained in order to optimize the performance of the fabricated I-V converter. Using the TIA alone means that the integer k is equal to 0, that is, there is no reset current. The input current was controlled from 0 to 3.0 μA in 500 nA steps for currents above 100 nA and in 30 nA steps for currents below 100 nA using the programmable constant current source. The TIA has three operation regions, as shown in Fig. 8. For input currents of less than about 100 nA, i.e. in region I, the TIA has logarithmic converting characteristics because the diode-connected MOSFET operates in the sub-threshold region and the diffused current is a major part of the drain current in this region.[6-8] This logarithmic characteristic, however, can be eliminated if the I_{biasP} is set to above 100 nA. The TIA has a linear characteristic well suited for an input current range from 100 nA to 2.5 μA, i.e. in region II. This region will be used repeatedly in the designed I-V converter. The output voltage of the TIA is saturated for input currents of above 2.5 μA, i.e. in region III. From this result, we can see that the fabricated TIA has a maximum linear input current of less than 2.5 μA, thus the reference current should be set below this current.

The conversion curve of the implemented I-V converter for when the reference current I_{REF} is set to 2 μA is shown in Fig. 9. In order to evaluate linearity for the overall expanded input current range, the left axis is defined as an effective analog output voltage V_{eff}, which can be calculated by

$$V_{eff} = V_{anlg} + [(2^k - 1) - k]V_{REF} \quad (1)$$

where V_{anlg} is the actual output voltage of the I-V converter, V_{REF} is the output voltage of the TIA at the reference current I_{REF}, and the integer k is the decimal value of the up-counter's output. We can see that the effective analog output voltage is linearly inversely proportional to the overall expanded input current range from 0 to 8 μA. The digital outputs of the I-V converter, shown on the right axis, vary from 000h to fffh with good linearity for the expanded input current range. As mentioned above, the digital outputs consist of upper 2 bits from the up-counter and lower 10 bits from the successive approximated ADC. From the results measured so far, the I-V converter has a maximum linear input current of 8 μA and a DR of approximately 80 dB, even though the TIA used has a linear input current of 2 μA and a DR of about 68 dB. As the 2-bit up-counter is used in this I-V converter, the maximum input current range is expanded by four times, and the DR is widened by 12 dB. If a 4-bit up-counter was used, the maximum input current and the DR could reach 32 μA and 92 dB, respectively.

In the evaluation system for a photometric sensor, the P-

I-N photodiode used has an output current of about 0.01 ㎂ to 8 ㎂ at an ambient brightness of 10 lux or twilight and 20,000 lux or full daylight, respectively. It has been confirmed that these levels can be linearly converted to a 12-bit digital output by the fabricated I-V converter. Even though a different input current range or a wider DR is required, the proposed I-V conversion algorithm or current-mode multiple reset can be applied by means of adapting the I_{REF}, I_{biasN} and I_{biasP} and/or increasing the bit-number of the up-counter.

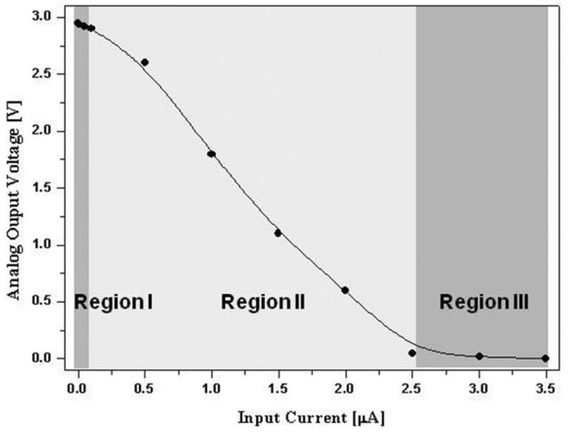


Fig. 8. Current-to-voltage conversion characteristic of the TIA alone.

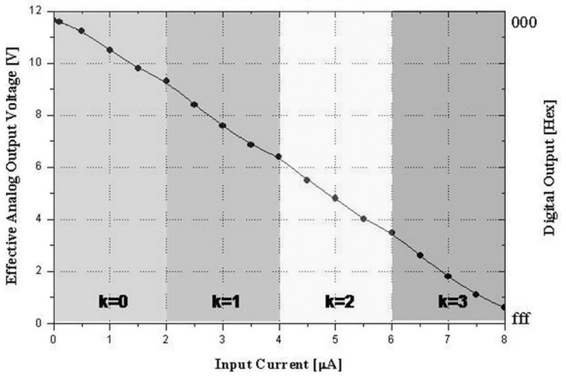


Fig. 9. Current-to-voltage conversion characteristic of the overall I-V converter.

4. CONCLUSIONS

In this paper, a current-mode multiple reset algorithm for I-V conversion was proposed, this algorithm achieves a large input current range and a wide DR. We successfully verified the proposed algorithm by producing an integrated I-V converter using 0.35 ㎛, 3.3 V CMOS mixed-signal technology, consisting of a linear TIA, a 2-bit up-counter and a 10-bit ADC. The fabricated I-V converter using the proposed conversion algorithm has linear I-V conversion characteristics up to an input currents above 8 ㎂ and a DR of approximately 80 dB, even though the TIA used in the I-V converter has a maximum linear input current of less than 2.5 ㎂. It is possible to generalize and say that the proposed current-mode multiple reset method expands the maximum input current and DR by a factor of 2^N and 6N, respectively, without any degradation of linearity, when an N-bit up-counter is used. In addition, the fabricated I-V converter was successfully applied to a photometric sensor system with a P-I-N photodiode. From these results, it was confirmed that the proposed I-V conversion algorithm could be applied to large-current sensing systems, such as P-I-N or avalanche photodiodes.

ACKNOWLEDGMENT

This work was supported by the IT R&D program of MKE/KEIT [2009-S-001-01, Development of Informative & Electronic Core Technology in Company Needs].

REFERENCES

[1] C. C. Hsieh, C. Y. Wu, and T. P. Sun, “A new cryogenic CMOS readout structure for infrared focal plane array”, *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1192-1199, 1997.

[2] D. Mičušik and H. Zimmermann, “Transimpedance amplifier with 120 dB dynamic range”, *Electron. Lett.*, vol. 43, no. 3, 2007.

[3] C. Wang and J. Wang, “Design of linear transimpedance amplifier”, *Proc. of 4th Int. Conf. ASIC*, pp. 232-235, 2001.

[4] M. Schanz, C. Nitta, A. Bußmann, B. J. Hosticka, and R. K. Wertheimer, “A high-dynamic-range CMOS image sensor for automotive applications”, *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 932-938, 2000.

[5] B. J. Hosticka, W. Brockherde, A. Bußmann, T. Heimann, R. Jeremias, A. Kemna, C. Nitta, and O. Schrey, “CMOS imaging for automotive applications”, *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 173-183, 2003.

[6] M. Schanz, W. Brockherde, R. Hauschild, B. J. Hosticka, and M. Schwarz, "Smart CMOS image sensor arrays", *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1699-1705, 1997.

[7] L. W. Lai, C. H. Lai, and Y. C. King, "A novel logarithmic response CMOS image sensor with high output voltage swing and in-pixel fixed-pattern noise reduction", *IEEE Sensors J.*, vol. 4, no. 1, pp. 122-126, 2004.

[8] C. A. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley, Boston, pp. 33-40, 1989.

[9] M. Förtsch, H. Zimmermann, and H. Pless, "220-MHz monolithically integrated optical sensor with large-area integrated PIN photodiode", *IEEE Sensors J.*, vol. 6, no. 2, pp. 385-390, 2006.

[10] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation", *IEEE J. Solid-State Circuits*, vol. SC-22, no. 3, pp. 357-365, 1987.

Jae-Hyoun Park received Bachelor's, Master's, and Ph. D. degrees in electronic engineering from Kyungpook National University, Daegu, Korea, in 1994, 1996, and 2005 respectively.

From 1996 to 2001, he worked with Deawoo Telecom Ltd., Busan, Korea, as a junior engineer. In 2004, he joined the Korea Electronics Technology Institute, Seongnam, Korea, and he is currently a managerial research engineer. His research interests include CMOS image sensors, readout ICs, and LED driver ICs.

Hyung-Do Yoon received a Ph. D. degree in electronic engineering from Sungkyunkwan University, Korea, in 2001.

In 1993, he joined the Korea Electronics Technology Institute, Seongnam, Korea, and he is currently a director of the compound semiconductor devices research center. His research interests include optic devices, OEIC, and LED lighting.