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Wideband VHF and UHF RF Front-End Receiver for DVB-H Application

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Abstract – This paper presents a wideband and low-noise direct conversion front-end receiver supporting VHF and UHFbands simultaneously. The receiver iscomposed of a low-noise amplifier (LNA), a down conversion quadrature mixer, and a frequency divider by 2. The cascode configuration with the resistor feedback is exploited in the LNA to achieve a wide operating bandwidth. Four gain-step modesare employed using a switched resistor bank and a capacitor bank in the signal path to cope with wide dynamic input power range. The verticalbipolar junction transistors are used as the switching elements in the mixer to reduce 1/f noise corner frequency. The proposed front-end receiver fabricated in 0.18 μm CMOS technology shows very low minimum noise figureof 1.8 dB and third order input intercept pointof -12dBm inthe high-gain mode of 26.5 dBmeasured at 500 MHz.The proposed receiverconsumeslow current of 20 mA from a 1.8 V power supply.

Keywords: CMOS, Wideband, Multistep gain, LNA, Mixer

1. Introduction

The integration level of mobile terminals, such as hand-held phones or tablet devices, has increasedas more features have beenadded. Hence, size-efficient design has become more important. Furthermore, since mobile devices, nowadays are planned for worldwide use. multi-band or multi-standard designs are inevitable. Integrating multi-standards and multi-bands in a small spacehas become a significant issue, even for chip or module designers.

Mobile broadcasting has been serviced usingseveral frequency bands, usually very-high frequency (VHF) or ultra-high frequency (UHF), with different standards ofdigital video broadcasting-handheld (DVB-H), terrestrial digital media broadcasting (T-DMB),or integrated services digital broadcasting-terrestrial (ISDB-T).To support multi-standards and multi-bands, until now, multi-antennas and multi-low-noise amplifiers (LNAs)have been usually used in the RF receiversas in [1, 2]. However, the size and costcompetitivenesscan be increased with the reduced number of required componentsif multiple bands,such as VHF and UHF bands, can be accommodated in asingle antenna and a single LNA [3-5].

Toembed two bandsusing a single antenna, the receiver configuration,especiallythe LNA, has to be redesigned to cover wide operating frequencies from VHF to UHF [6, 7] andthe receiver should haveenough low noise figure (NF) toprevent the system sensitivityin the two bands to deterioratesimultaneously. However, thesewide bandwidth systems are inevitably vulnerable to interference, which can deteriorate in-band signal purity. Hence, high linearity requirement is essential. These two requirements should be met over the wholerange of input power and throughout the operating bandwidth. Introducing a multi-step gain mode is an effective way of trading off between the two constraints.

In thispaper, a widebandand very low noise direct conversion front-end receiver supportingVHF and UHF bandsis introducedfor mobile broadcasting. The multi-gain mode is employed using a switched resistor bank and a capacitor bank in the signal path.

2. Receiver Design

Fig. 1 shows the system overview. The proposed front-end receiver is designed as the part of a mobile broadcasting direct-conversion receiver applicable to DVB-H/T, ISDB-T, and T-DMB.The tuner supports UHF and VHF band simultaneously with a single LNA with a single input. The single input designis more advantageous

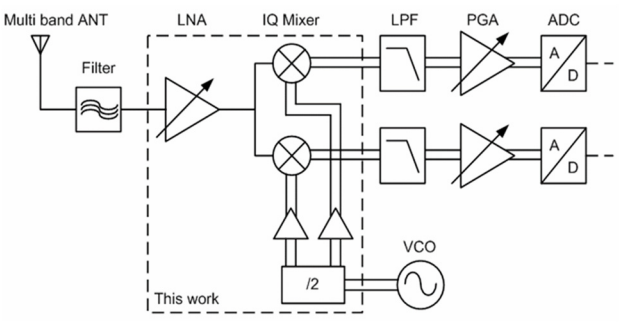

Fig. 1. System overview

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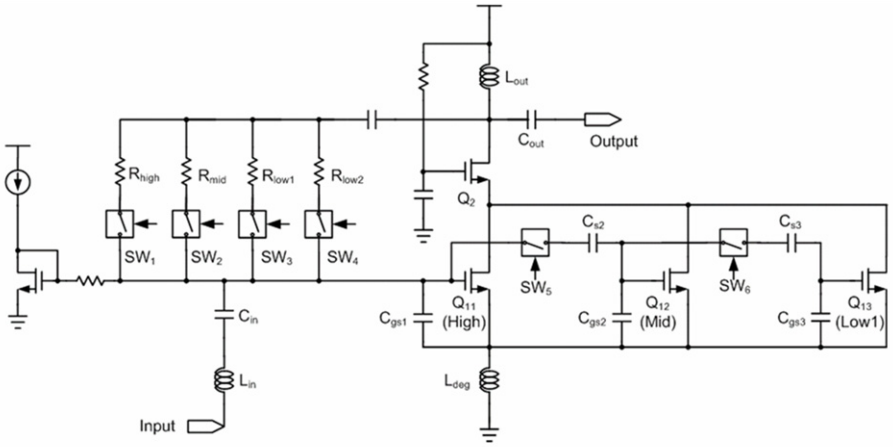

	Q_{11}	Q_{12}	Q_{13}	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6
High	O	X	X	O	X	X	X	X	X
Mid	X	O	X	X	O	X	X	O	X
Low1	X	X	O	X	X	O	X	O	O
Low2	X	X	X	X	X	X	O	X	X

Fig. 2. Low-noise amplifier circuit schematic and control logic table (External Component: C_{in}= 10 n F, L_{in} = 12 nH)

compared withthe differential input becauseno additional bulky balunbetween the antenna and the LNA is required. Hence, the single input design is helpful in reducingthe module size andcost.

The LNA schematic is described in Fig. 2. The LNA employs common gate (CG) and common source (CS) stages with a degeneration inductor, L_{deg}. The feedback resistorsare employedto increase operating bandwidth. By changing the feedback resistor values and adding the capacitive losses, four-gain steps are achieved. Through these two techniques, accurate step gains and wideband input matching can be obtained.

In high-gain mode, SW_1 is turned on and the feedback resistance is chosen as R_{high}, whereas SW_2 –SW_6 are turned off and Q_{12} and Q_{13} are off-biased. Then, the input signal is amplified with high gain by the common source transistor, Q_{11}. In mid or low1 gain step, the signal amplification is accomplished in the common source transistor, Q_{12} or Q_{13}, respectively. However, the feedback resistances are lowered by switching on SW_2 or SW_3 and the input voltages to Q_{12} or Q_{13} experience capacitor dividing by the ratio of C_{s2}, C_{s3}, C_{gs2}, and C_{gs3}. Hence, the gains at mid or low1 gain mode decreaseabout 9 and 18 dB compared to the high gain mode. But the thirdinput intercept point increases as much as the gain decreases. In low2 gain step,the biases of all transistors are turned offand all switches are off except SW_4. The input signal passes through the passive elements to the output of LNA with 2 dB loss. The power consumption in the low2 gain mode becomes zero. The on and off status and bias conditions are summarized in the inset of Fig. 2. The degeneration inductor, L_{deg}(0.35 nH), is implemented with a down-bonded wire.Capacitors, C_{gs1}–C_{gs3} are selected to match possible noise and gain optimum pointsat each gain mode.

Toimprovethe electro-static discharge (ESD) perfor- mance, back-to-back diodes and clamp circuits are employed, as depicted in Fig. 3. The parasitic capacitance of ESD is around 150 fF, and the pad parasitic for bond-wire is around 100 fF. The parasitics (C_1 =0.3 pF, L=2 nH, C_2 = 0.25 pF) of the package and the pad lower theinput impedance of the LNA, which are characterized by anelectro-magnetic simulator and included in the circuit simulation.

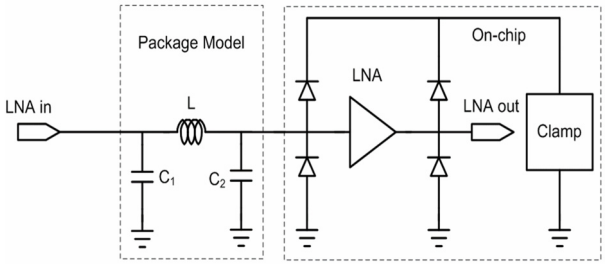

Fig. 3. Schematic of ESD protection and package model

The down conversion I-Q mixer in Fig. 4 is based on the differential Gilbert cell, and includes a function of single to differential conversion. The common gate, $Q_1$and the common source, Q_2 convert the input single-phase voltage to the differential currents i_p and i_n. The mismatch arising fromthe series resistance of the inductor,L_s is compensated by adding a very small resistor R_s of 2 Ohm. Thus, the trans-conductance (g_m) of the CS and CG stagescan be equalizedtoprovidethe true differential currents without lowering the gain of the CS stage.

In this direct conversion architecture, one of the most critical problems is flicker noise, mainly generated in the switching transistors of a Gilbert-type down-conversion mixer. To overcome this, vertical bipolar junction

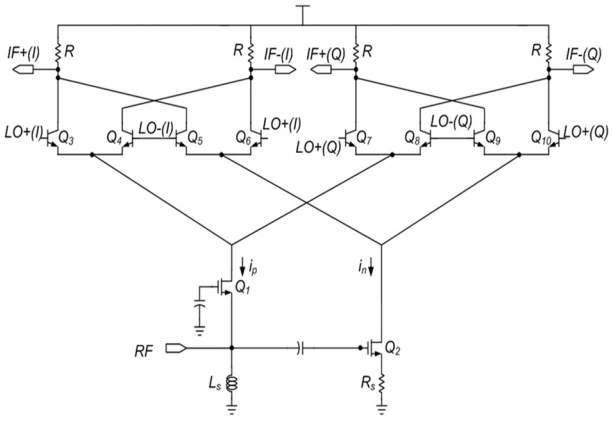

Fig. 4. IQ Mixer schematic using the vertical BJT

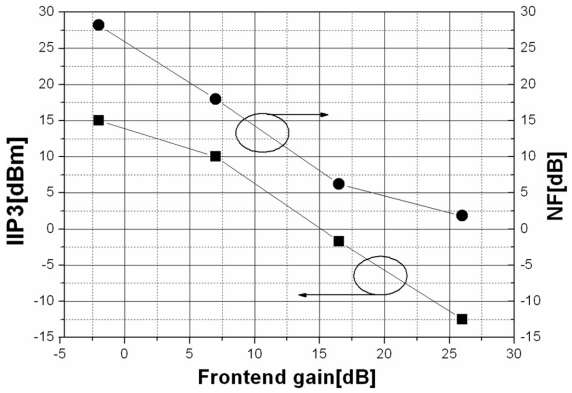

Fig. 5. Measured IIP3 and NF versus front-end gain at 500 MHz

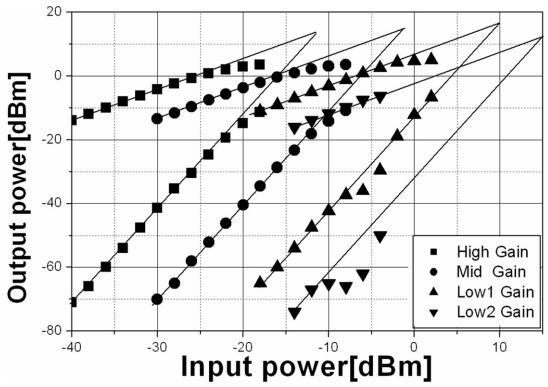

Fig. 6. Measured fundamental and intermodulation power vs. input power

transistors(BJT) are adopted as switching devices Q_3–Q_{10} in the I-Q mixer. The BJTsimprove flicker noise characteristicswhile sacrificing very little linearity [8]. The usage of the vertical BJT in the switching stage greatly reduces 1/f noise corner frequency in twoorders compared with the NMOS transistor. The limitation of the vertical BJT is low unit-gain frequency, f_T less than 2 or 3 GHz in 0.18 μm CMOS technology, and relatively low input impedance [7]. However, vertical BJTs can be successfullyemployed as switching elementsbecausethe switching operation is less than 1 GHz in this application.The frequency divider is laid out as close to the mixer as possiblebecause the mixer performance depends on the driving power of the local carriers. The frequency divider is designed inthe conventional CML typeto generate the quadrature phase signals for the down-conversion mixer.

3. Experiment Result

The receiver was implemented using 0.18 μm CMOS technology. The fabricated chip was packaged in 32-QFN, glued on the printed circuit board (PCB), and measured using an NF meter, two-tone signal generator, and a spectrum analyzer.

The NF and the third-order input intercept points (IIP3)measured at 500 MHz are depicted in Fig. 5. Measurement was done at the 4-gain mode of 26.5, 16, 7, and -2 dB, respectively. At the high-gain mode determiningthe whole system sensitivity, a verylow minimum NF of 1.8 dB is given. At the low-gain mode, a high IIP3 of 27 dBm isachieved. The 1/f noise corner frequency was measured to be less than 1 kHz,attributedto the low-noise vertical BJTs.

The linearity of the receiver is estimated by applying two-tone input signals with 2 MHz frequency spacing. Fig. 6 shows the measurement results of the fundamental and intermodulation output powers versus input power at each gain mode. The IIP3 is obtainedby extrapolating the measurement data and the secondorder intercept point (IIP2) measured using thesame method. The estimated IIP3s are about -12, -2, 10, and 15 dBm at each gain step. Fig. 7 shows the frequency variation of important design requirements. The gain variation is less than 5 dB from 150 MHz to 850 MHz.The minimum NF is centered at around 400 MHz, and theaverage NF between 470MHz and 700 MHzwas measured less than 2.8 dB.The IIP2 measurement results showed more than 22 dBm. Fig. 8 shows the input matching characteristics. The targeted return loss was less than -8 dB in the whole frequency range of 170 MHz to 250MHz (VHF) and 480 MHz to 700 MHz (UHF). However, the measured return loss was higher than expected. The difference is ascribed to the pad and package model inaccuracy. The high return loss at the VHF band can cause a slight NF degradation. The front-end chip consumes low current of 20 mA composed of 10 mA at LNA, 4 mA at the mixer core, 4 mA at the mixer buffers, and 2 mA at divider-by-2. The chip size is 800 × 2400 μm^2 as shown in Fig. 9.

The measured data werecompared with the recently published front-ends that cover VHF and UHF frequency bands with a single LNA or multiple LNAs. The proposed receiver showslower or comparable NFin both bands with reasonable linearity.

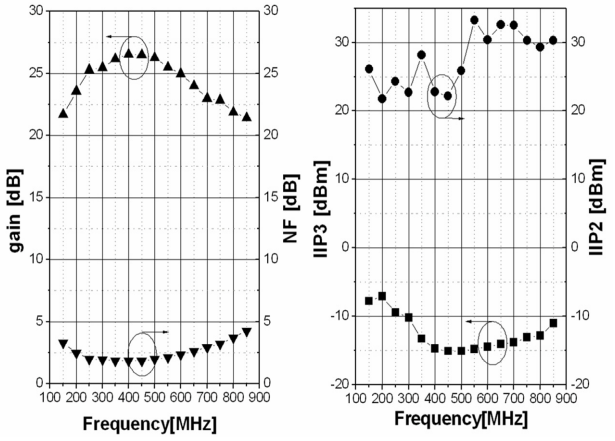

Fig. 7. Measured gain, NF, IIP3, and IIP2 vs. frequency

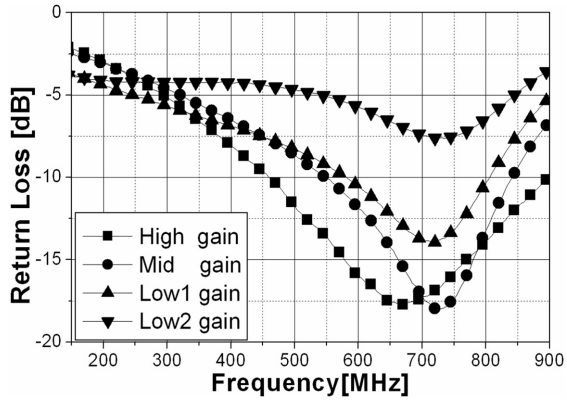

Fig. 8. Measured return loss characteristics

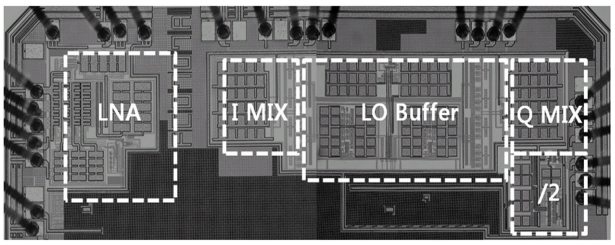

Fig. 9. Photograph of the fabricated radio frequency front-end (800 × 2400 μm^2)

Table 1. Photograph of the fabricated RFfront-end

	Ref[9]	Ref[10]	Ref[11]	Ref[12]	This work
Tech.	CMOS 65 nm	CMOS 0.18 μm	CMOS 65 nm	CMOS 0.18 μm	CMOS 0.18 μm
Config.	Multi LNA	Single LNA	Multi LNA	Single LNA	Single LNA
NF, dB* @Max Gain (VHF/UHF)	2.5 to 3 /2.2 to 3.2	5 to 6 /5 to 7	2.7 to 3.0 /3.6 to 4.8	4 to 7	1.8 / 2.8
IIP3, dBm @high Gain	-4/-6	-30/-23	-	-13.8 at 500 MHz	-10/-15
IIP2, dBm @high Gain	26/30	-	-	-	22/29
Supply (V)	1.2, 2.5	1.8	1.8	1.8	1.8

* VHF Band: 170 MHz to 210 MHz; UHF Band:470 MHz to 700 MHz

6. Conclusion

A fully integrated wideband and low-noise radio frequencyfront-end receiver supporting VHF and UHF bands simultaneously has been realized in 0.18 μm CMOS technology. To enlarge the operating bandwidth and accommodate the multi-step gain mode, a cascode configuration with a switched resistor feedback and a switched capacitive loss are proposed. The single to differential conversion is performed in the input stage of the in phase-quadrature(IQ) mixer. The parasitic vertical BJT, which is the switching device of the IQ mixer, is used to minimize 1/f noise contribution.The proposed front-end receiver shows low minimum NF of 1.8 dB and IIP3 of -12 dBm in the high-gain mode of 26.5 dB measured at 500 MHz. The proposed receiverconsumes low current of 20 mA from a 1.8 V power supply

Acknowledgements

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