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# A Novel Control Strategy of Three-phase, Four-wire UPQC for Power Quality Improvement

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**Abstract** – The current paper presents a novel control strategy of a three-phase, four-wire Unified Power Quality (UPQC) to improve power quality. The UPQC is realized by the integration of series and shunt active power filters (APF) sharing a common dc bus capacitor. The realization of shunt APF is carried out using a three-phase, four-leg Voltage Source Inverter (VSI), and the series APF is realized using a three-phase, three-leg VSI. To extract the fundamental source voltages as reference signals for series APF, a zero-crossing detector and sample-and-hold circuits are used. For the control of shunt APF, a simple scheme based on the real component of fundamental load current (I CosΦ) with reduced numbers of current sensors is applied. The performance of the applied control algorithm is evaluated in terms of power-factor correction, source neutral current mitigation, load balancing, and mitigation of voltage and current harmonics in a three-phase, four-wire distribution system for different combinations of linear and non-linear loads. The reference signals and sensed signals are used in a hysteresis controller to generate switching signals for shunt and series APFs. In this proposed UPQC control scheme, the current/voltage control is applied to the fundamental supply currents/voltages instead of fast-changing APF currents/voltages, thus reducing the computational delay and the required sensors. MATLAB/Simulink-based simulations that support the functionality of the UPQC are obtained.

**Keywords**: Power quality, UPQC, Load balancing, Power factor correction, Voltage harmonic mitigation, Current harmonic mitigation, Source neutral current mitigation.

## 1. Introduction

The main power quality problems in three-phase, four-wire distribution systems are poor voltage regulation, high reactive power demand, harmonics current burden, load unbalancing, excessive neutral current, voltage harmonics, and voltage sags and swells. The quality degradation leads to low power factor, low efficiency, overheating of transformers, and so on. Moreover, in case of the distribution system, the overall load on the system is hardly balanced, causing excessive neutral currents in a three-phase, four-wire distribution system. Overheating of the neutral conductor occurs because of the fundamental and high-frequency contents in the neutral current [1-3]. With the application of sophisticated and more advanced software and hardware for the control systems, power quality has become one of the most important issues for power electronics engineers. To control power quality problems, many standards are proposed by different agencies, such as the IEEE-519 standard [4]. Ideally, voltage and current waveforms are in phase, the power factor of load equals unity, and the reactive power consumption is zero. This situation enables the most efficient transport of active power, leading to the attainment of the cheapest distribution system. In the past, the solutions to mitigate these identified power quality problems were through conventional passive filters. However, their limitations, such as fixed compensation, resonance with the source impedance, and difficulty in tuning time dependence of filter parameters, have ignited the need for active and hybrid filters [5-7]. Under this circumstance, a new technology called Custom Power Devices (CPDs) emerged [8, 9]. This technology is applicable to distribution systems for enhancing the reliability and quality of power supply.

The Unified Power Quality Conditioner (UPQC) is one of the best solutions to compensate both current- and voltage-related problems simultaneously [10-12]. As the UPQC is a combination of series and shunt active power filters (APFs), two APFs have different functions. The series APF filter suppresses and isolates voltage-based distortions, whereas the shunt APF cancels current-based distortions. At the same time, the shunt APF compensates for the reactive current of the load and improves power factor. Many control strategies to determine the reference signals of the voltage and the current of three-phase four-wire UPQC are reported in the literature. The most common are the **p-q-r** theory [13], modified single-phase **p-q** theory [14], Synchronous Reference Frame (SRF)

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theory [15], symmetrical component transformation [16], and the Unit Vector Template technique [17]. Apart from this, the one-cycle control [18] (without reference calculation) is also used for the control of three-phase, four-wire UPQC.

For the mitigation of neutral current, along with other power quality compensation, in the supply currents, different topologies of three-phase four-wire UPQC are reported in the literature. Some of these are three-leg VSI with a split capacitor [13], three-single phase Voltage Source Inverter (VSI) [16], four-leg VSI [14, 18], and Current Source Inverter [19]. As the UPQC is a combination of series and shunt APFs, six single-phase, VSI-based UPQCs require 24 semiconductor devices; hence, they are not attractive. The three-leg VSI with a split capacitor [13] has difficulty in maintaining equal DC voltages of two series-connected capacitors. As such, a four-leg VSI-based UPQC is a better choice in terms of the number of switches, complexity, cost, and so on. In the current paper, the shunt APF of the three-phase, four-wire UPQC is realized using a four-leg VSI and a three-leg VSI is used for series APF. To extract the fundamental source voltages as reference signals for series APF, a zero-crossing detector and sample-and-hold circuits are used. The control of shunt APF is based on I CosΦ theory [20, 21].

The performance of the proposed system is demonstrated through simulated waveforms using SimPowerSystems (SPS) MATLAB/Simulink environment. The UPQC configuration is discussed in Section II, and the control algorithm for UPQC is illustrated in Section III. The SPS MATLAB/Simulink-based simulation results are explained in Section IV. Section V concludes the paper.

## 2. System Description

The system under consideration for three-phase, four-wire distribution system is shown in Fig. 1. The UPQC is connected before the load to make the source and the load voltage free from any distortions. At the same time, the reactive current drawn from the source should be such that the currents at source side would be in phase with utility voltages. Provision is made to realize voltage harmonics in the source voltage by switching on/off the three-phase diode bridge rectifier. The UPQC, carried out by using two VSIs, is shown in Fig. 2: one VSI acts as the shunt APF and the other as the series APF. The shunt APF is realized using a three-phase, four-leg VSI, and the series APF is carried out using a three-phase, three-leg VSI. Both APFs share a common dc link between them. The four-leg, VSI-based shunt active filter is capable of suppressing the harmonics in the source currents, negative sequence of the source current, load balancing, and power-factor correction. The implemented control algorithm consists mainly of the computation of the three-phase reference voltages of load voltages ($v^*_{la}$ , $v^*_{lb,}$ and $v^*_{lc}$), and the reference currents for the source current ( $i^*_{sa}$ , $i^*_{sb,}$ and $i^*_{sc}$).

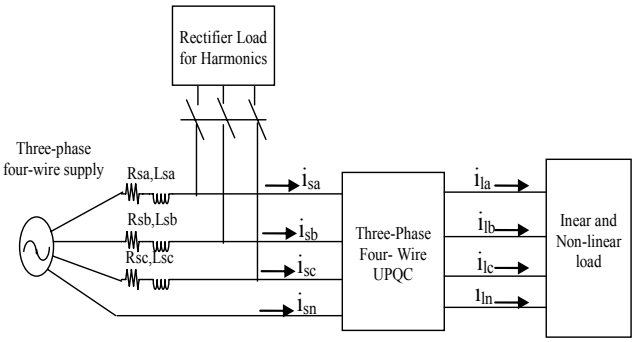


**Fig. 1.** The system

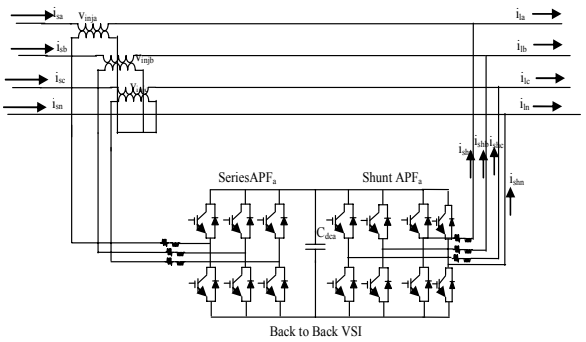


**Fig. 2.** UPQC block diagram

The voltage at the source side before UPQC, load voltage at the load, voltage injected by the series APF, and dc link voltage between two inverters are represented by $v_s$, $v_L$, $v_{inj,}$ and $V_{dc}$, respectively. The current on the source side, current drawn by the loads, neutral current on the source side, load neutral current, and current injected by the shunt APF are represented by $i_s$, $i_l$, $i_{sn}$, $i_{ln,}$ and $i_{sh,}$ respectively.

## 3. Control Strategy of the UPQC

The proposed control strategy aims to generate reference signals for both shunt and series APFs of the UPQC. The proposed control technique is capable of successfully extracting most of the load current and source voltage distortions. The series APF is controlled to eliminate the supply voltage harmonics; whereas the shunt APF is controlled to alleviate the supply current from the harmonics, negative sequence current, reactive power, and load balancing.

### 2.1 Reference voltage signal generation of the series APF

The control algorithm for the series APF is shown in Fig. 3. As the supply voltage is distorted, a phase-locked loop

(PLL) is used to achieve synchronization with the supply voltage [14]. Three-phase distorted supply voltages are sensed and given to PLL, generating two quadrature unit vectors (i.e., sinwt and coswt). The in-phase sine and cosine outputs from the PLL are used to compute the in-phase, 120º displaced and -120º displaced, three unit vectors ($u_a$ ,$u_b$ and $u_c$) using Eq. (1) as follows:

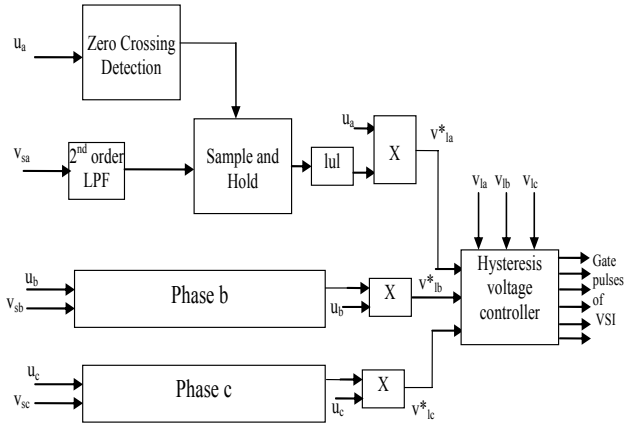


**Fig. 3.** Control scheme of the series APF

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \tag{1}$$

The amplitude of the fundamental source voltage is extracted at the zero crossing of the in-phase unit template of the PCC voltage from the source voltages. This extraction is conducted by shifting the source voltages by +90º using a set of low-pass filters. The filters have a 50 Hz cut-off frequency to obtain the magnitude of the fundamental source voltage. A zero-crossing detector and a sample-and-hold circuit are used to determine the amplitude of the fundamental source voltage at the zero crossing of a corresponding in-phase unit template. The amplitude of the fundamental source voltage is then multiplied by the unit vector of the corresponding unit vectors to obtain the reference load voltages ($v^*_{la,}$ $v^*_{l\,b,}$ and $v^*_{lc}$) as per Eq. (2):

$$\begin{aligned} \left[v^*_{la}\right] &= \left[V_{sa1}\right]\cdot\left[u_a\right] \\ \left[v^*_{lb}\right] &= \left[V_{sb1}\right]\cdot\left[u_b\right] \\ \left[v^*_{lc}\right] &= \left[V_{sc1}\right]\cdot\left[u_c\right] \end{aligned} \tag{2}$$

where, $V_{sa1}$,$V_{sb1}$, and $V_{sc1}$ are the extracted magnitudes of the fundamental source voltages in phases a, b, and c, respectively. The computed load reference load voltages ($v^*_{la,}$ $v^*_{lb,}$ and $v^*_{lc}$) from Eq. (2) are then given to the hysteresis controller along with the sensed three-phase actual load voltages ($v_{la}$ , $v_{lb,}$ and $v_{lc}$). The output of the hysteresis controller switches signals to the six switches of the VSI of the series APF. The hysteresis controller generates the switching signals such that the voltage at PCC becomes the desired sinusoidal reference voltage. Therefore, the injected voltage across the series transformer through the ripple filter cancels out the harmonics present in the supply voltage. The load voltage then becomes distortion-free.

## 2.2 Reference current signal generation of the shunt APF

The control algorithms for the shunt APF consists of the generation of three-phase reference supply currents ($i^*_{sa,}$ $i^*_{sb,}$ and $i^*_{sc}$). The control algorithm based on the modified I CosΦ algorithm is shown in Fig. 4.

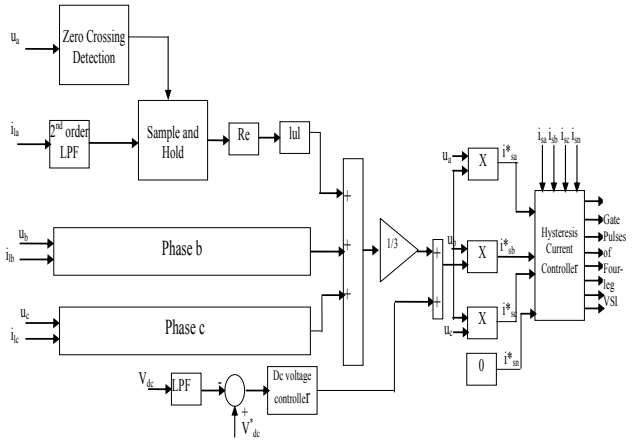


**Fig. 4.** Control scheme of the shunt APF using I CosΦ theory

The amplitude of the active component (I CosΦ) of the fundamental load current is extracted at the zero crossing of the in-phase unit template of the PCC voltage from the load currents by +90° using a set of low-pass filters. The filters have a 50 Hz cut-off frequency to extract the fundamental load current. A zero-crossing detector and a sample-and-hold circuit are used to extract the I CosΦ (amplitude of the fundamental load current at the zero crossing of the corresponding in-phase unit template). The magnitude of the real component of the fundamental load current in each phase is given as follows:

$$\begin{aligned} \left|\mathrm{Re}\left(I_{La1}\right)\right| &= \left|I_{La}\right|\cdot Cos\phi_a\,; \\ \left|\mathrm{Re}\left(I_{Lb1}\right)\right| &= \left|I_{Lb}\right|\cdot Cos\phi_b\,; \text{ and} \\ \left|\mathrm{Re}\left(I_{Lc1}\right)\right| &= \left|I_{Lc}\right|\cdot Cos\phi_c \end{aligned} \tag{3}$$

To ensure balance and sinusoidal source currents with the unity power factor, the magnitude of the desired active

component of the reference source currents can be expressed as

$$I_{sP}^{*} = \left(|I_{La}|Cos\phi_a + |I_{Lb}|Cos\phi_b + |I_{Lc}|Cos\phi_{cd}\right)/3 + I_d \tag{4}$$

where $|I_{La}|Cos\phi_a; |I_{Lb}|Cos\phi_b; |I_{Lc}|Cos\phi_c$ are the amplitudes of the load active currents, and $I_d$ is the output of DC bus voltage PI controller for self-supporting bus of the UPQC, which can be expressed as:

$$I_{d(n)} = I_{d(n-1)} + K_{pd}\left\{V_{de(n)} - V_{de(n-1)}\right\} + K_{id}V_{de(n)} \tag{5}$$

where $V_{de(n)} = V_{dcr} - V_{dca(n)}$ denotes the error in $V_{dc}$ calculated over reference value of $V_{dc}$. and average value of $V_{dc}$. $K_{pd}$, and $K_{id}$ are proportional and integral gains of the dc bus voltage PI controller. The three-phase component of the source currents can be obtained with the in-phase unit templates as follows:

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = I_{sp}^{*} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{6}$$

The proposed control algorithm compares the sensed (i.e., $i_{sa}$, $i_{sb}$, and $i_{sc}$) and reference source currents (i.e., $i^{*}_{sa}$, $i^{*}_{sb}$, and $i^{*}_{sc}$) in a hysteresis current controller to generate the switching signals to the switches of the shunt APF, making the supply currents sinusoidal, balanced, and in phase with the voltage at the PCC. Hence, the supply current contains no harmonics or reactive power component. The source-neutral current is compensated for to follow a reference signal of zero magnitude by switching the fourth leg of the VSI through the hysteresis controller. By such arrangement, the supply-neutral current can be eliminated. In this proposed control scheme, the current control is applied over the fundamental supply currents instead of the fast-changing APF currents, thus reducing the computational delay. In addition, the load or the filter-neutral current is not sensed, hence reducing the current sensors.

## 4. Results and Discussion

The developed model of a UPQC system in a MATLAB/Simulink environment is shown in Fig. 5. To the realize voltage harmonics in the source voltage, a three-phase rectifier load is switched on at t = 0.05 s. The load under consideration is a combination of linear and non-linear loads. Two single-phase lagging power-factor loads are taken as a linear load, whereas a three-phase diode bridge rectifier with a resistive load on the dc side is considered a non-linear load. The values of the circuit parameters and load under consideration are given in the Appendix. The performance of the UPQC is evaluated in terms of voltage and current harmonics mitigation, load balancing, neutral source current mitigation, and power-factor correction for a combination of linear and non-linear loads.

### 4.1 Performance of the UPQC in load balancing, power-factor correction, current, and voltage harmonics mitigation

The response of the UPQC in load balancing, power-factor correction, voltage harmonic mitigation, and current harmonic mitigation is presented in Fig. 8. To verify the effectiveness of the control algorithm for voltage harmonic

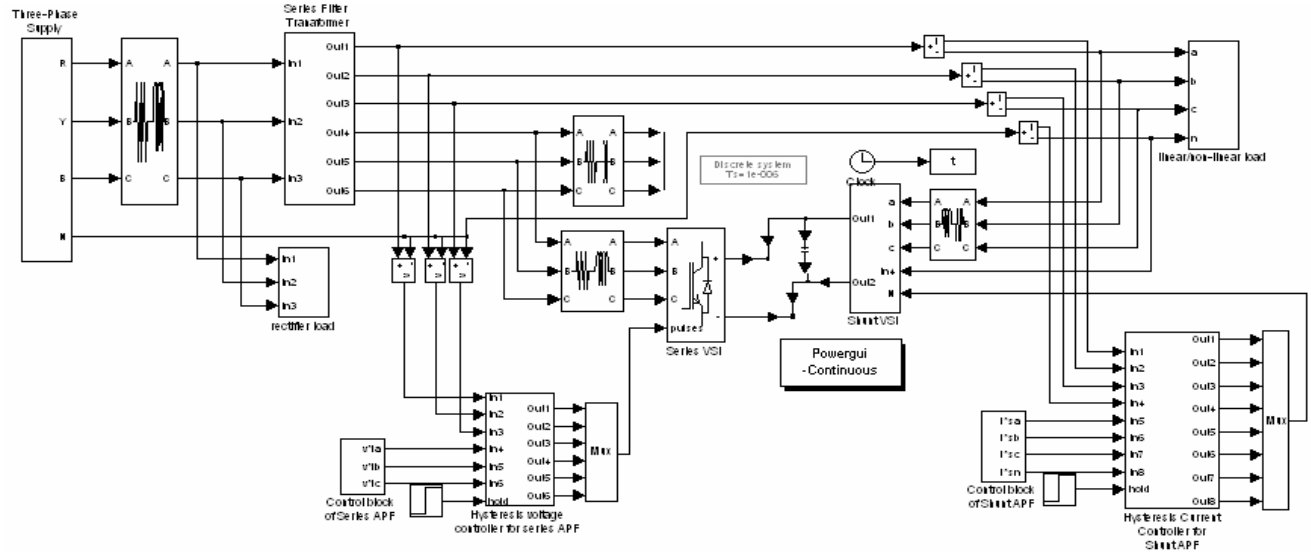


**Fig. 5.** MATLAB model of the UPQC system

mitigation, a three-phase diode bridge rectifier with resistive load on the dc side is switched on at $t_1$= 0.05 s. Thus, the voltage across the load becomes distorted. To visualize the individual performance of the shunt APF and series APF, both APFs are put into operation at different times. At time $t_2$=0.1 s, the shunt APF is put into operation first. As shown in Fig. 6(d), the supply currents are balanced, sinusoidal, and in-phase, with the voltages even under non-sinusoidal utility voltage. The source current THD in phase "c" is improved from 15.36% to 2.36%. At time $t_3$=0.25 s, the series APF is put into the operation. The series APF starts compensating for the voltage harmonics immediately by injecting out of the phase harmonic voltage, making the load voltage distortion-free.

The voltage injected by the series APF is shown in Fig. 6(c). Here, the load voltage THD is improved form 6.27% to 0.53%. The harmonic spectra of the source current and the load voltage in phase "c" with compensation and without compensation are shown in Fig. 7. Owing to the unbalanced load, a current of 18.60 A RMS ($i_{ln}$) flows in the neutral conductor, as shown in Fig. 6(i). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply-neutral current ($i_{sn}$) to zero, as depicted in Fig. 6(h).

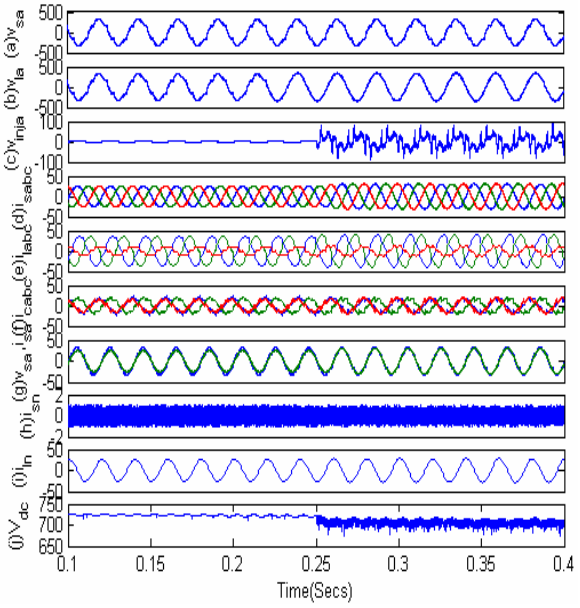


**Fig. 6.** Performance of the UPQC in load balancing, power factor correction, current, and voltage harmonic mitigation

### 4.2 Performance of the UPQC during Sudden Load Change

To show the response of the UPQC during sudden load change, the load across the dc side of the rectifier is increased at t=0.25 s. As shown in Fig. 8(b), in addition to the load balancing, power-factor correction, and current

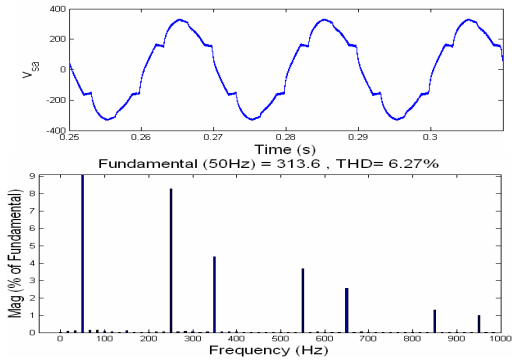


**Fig. 7.** (a) Load voltage and its harmonic spectrum before compensation

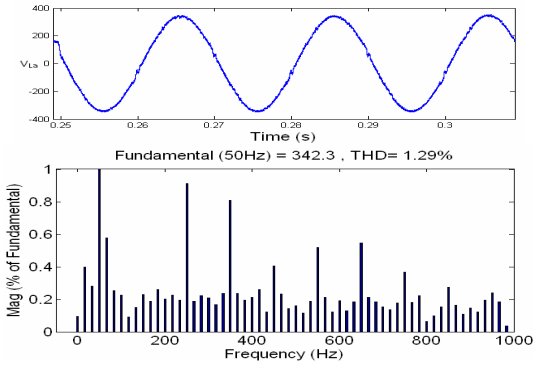


**Fig. 7.** (b) Load voltage and its harmonic spectrum after compensation

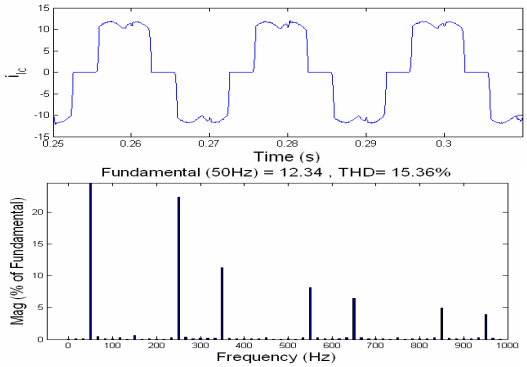


**Fig. 7.** (c) Source current in phase "c" and its harmonic spectrum before compensation

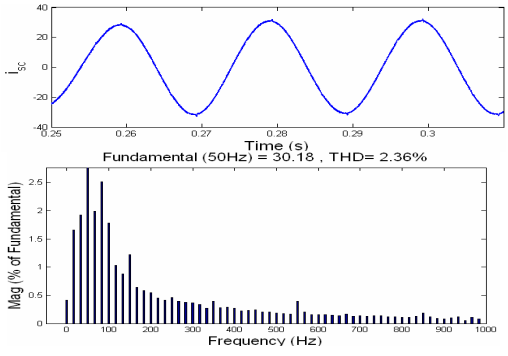


**Fig. 7.** (d) Source current in phase "c" and its harmonic spectrum after compensation

harmonic mitigation, the UPQC controller acts immediately without any delay in the operation and gains a new steady state. Moreover, in Fig. 8(f), a small dip in the dc voltage at t=0.25 s is present, but the dc link is able to regulate the dc voltage to its previous value. Fig. 10(i) shows that a current ($i_{ln}$) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply-neutral current ($i_{sn}$) to zero, as depicted in Fig. 8(h).

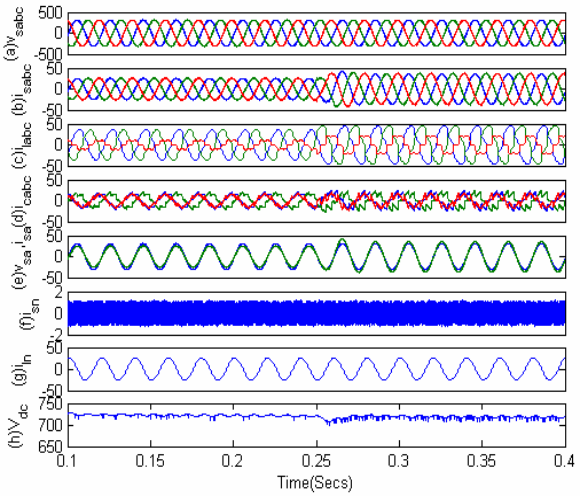


**Fig. 8.** Performance of the UPQC during sudden load change

### 4.3 Comparison with conventional techniques

The conventional techniques reported in literature [13-15] give poor results under distorted and/or unbalanced input/utility voltages, and they involve many calculations. The proposed scheme is a simple scheme for achieving effective compensation for current harmonics, reactive power compensation, load balancing, and voltage harmonic mitigation even under distorted and/or unbalanced input/utility voltages. To compare the results of the proposed scheme with those of the conventional techniques, the simulation results of the UPQC based on SRF theory [15] are presented here. The results obtained with the SRF theory and the proposed scheme is compared in Table 1.

The simulation results using SRF theory are presented in Fig. 9. The shunt APF is switched on at t=0.05 s. The shunt APF compensates for the current harmonics, load balancing, and reactive power, as shown in Fig. 9(f). The source currents are sinusoidal and balanced, as shown in Fig. 9(d), and are in phase with the supply voltage, as shown in Fig. 9(g). The source-neutral current is compensated for, as depicted in Fig. 11(h), and the load-neutral current is shown in Fig. 9(i). The series APF is switched on at t=0.25 s, compensating for the voltage harmonics, as shown in Fig. 9(c). The load voltage THD is reduced from 6.27% to 0.78%, and the source current THD in phase "c" is reduced from 15.36% to 3.31%.

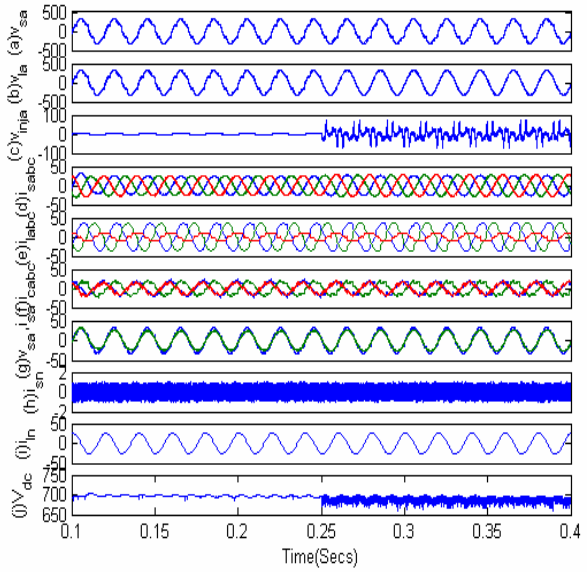


**Fig. 9.** Performance of the UPQC using SRF theory

## 5. Conclusion

The proposed control scheme for three-phase, four-wire UPQC is validated and compared with the SRF theory through the simulation results using MATLAB software, Simulink and SPS toolbox. The performance of the UPQC is satisfactory in various power quality improvements, such as load balancing, neutral source current mitigation, power-factor correction, voltage harmonics mitigation, and current harmonic mitigation. Supply currents and load voltage harmonic levels are maintained below IEEE-519 standards under all conditions. The computational delay is reduced by indirectly controlling the three-phase supply currents/voltages. Moreover, the load and APF neutral currents are not sensed; hence, the number of current sensors is reduced. The comparison of the proposed and the SRF-based control algorithms is presented in Table 1.

**Table 1.** % thd of the supply currents and load voltage

| Supply currents/load voltage | Without UPQC | UPQC with I CosΦ theory | UPQC with SRF theory |
|---|---|---|---|
| %THD in current in Phase "c" | 15.36% | 2.36% | 3.31% |
| %THD in load voltage | 6.27% | 1.29% | 0.78% |

## Appendix

The system parameters used are as follows:
Supply voltage and line impedance: 415 V L-L, f=50 Hz, $R_s$=0.1 ohm, $L_s$=1.5 mH
Filter: R=7 Ω, C=5 μF
DC bus capacitance: $C_{dc}$=3000 μF
Transformer: 250 MVA, 58 kV/12 kV

$V_{dc}$=700 V

$K_p$=$K_i$=2

Loads: Two single-phase linear load of 12 KW, 8 KVar in phase "a" and "b" only and a three-phase rectifier load R=50 ohm on the dc side.

## References


[1] E. W. Gunther and H. Mehta, "A survey of distribution system power quality", IEEE Trans. on Power Delivery, vol.10, No.1, pp.322-329, Jan.1995.

[2] R. C. Dugan, M. F. McGranaghan and H.W. Beaty, Electric Power System Quality, 2nd Edition, McGrawHill, New York, 2006.

[3] Ewald F. Fuchs and Mohammad A. S. Mausoum, "Power Quality in Power Systems and Electrical Machines," Elsevier Academic Press, London, UK, 2008.

[4] IEEE Recommended Practices and Requirments for Harmonics Control in Electric Power Systems, IEEE Std.519, 1992.

[5] B. Singh, AL.K. Haddad and A. Chandra, "A review of active filters for power quality improvement," IEEE Trans. on Ind. Electron, vol.46, pp. 960–971, 1999.

[6] H Akagi, "New trends in active Filters for power conditioning," IEEE Trans. on Ind. Appl., 1996, 32, pp. 1312–1322

[7] B.Singh, V. Verma, A. Chandra and K. Al-Haddad, "Hybrid filters for power quality improvement," Proc. IEE on Generation, Transmission and Distribution, vol.152, pp.365-378, May 2005.

[8] Arindam Ghosh, Gerard Ledwich, "*Power Quality Enhancement Using Custom Power Devices,*" Kulwer International Series in Engineering and Computer Science, 2002.

[9] N. G. Hingorani, "Introducing custom power," Proc. IEEE Spectrum, vol.32, pp.41-48, June1995.

[10] M. Aredes, K. Heumann, and E. H. Walandble, "An universal active power line conditioner," *IEEE Trans. Power Del.*, vol. 13, no. 2, pp. 545–551, Apr. 1998.

[11] H. Fujita and H. Akagi, "The unified power quality conditioner: the integration of series- and shunt-active filters," *IEEE Trans. Power Electron.*, vol. 13, no. 2, pp. 315–322, Mar. 1998.

[12] B. Han, B. Bae, H. Kim, and S. Baek, "Combined operation of unified power-quality conditioner with distributed generation," *IEEE Trans. Power Del.*, vol. 21, no. 1, pp. 330–338, Jan. 2006.

[13] Tan Zhili, Li Xun, Chen Jian, Kang Yong and Duan Shanxu, "A direct control strategy for UPQC in three-phase four-wire system," in *Proc. IEEE Conf. on Power Electron. and Motion Control 2006*, vol.2, pp. 1-5.

[14] V. Khadkikar and A. Chandra, "A Novel Structure for Three-Phase Four-Wire Distribution System Utilizing Unified Power Quality Conditioner (UPQC)," IEEE Trans. Industry Applications, vol. 45, pp.1897-1902, 2009.

[15] Li. Xun, Zhu. Guorong, Duan. Shanxu and Chen Jian Chen, "Control Scheme for Three-Phase Four-Wire UPQC in a Three-Phase Stationary Frame," Procd. IEEE/IECON 2007, pp.1732-1736, 2007.

[16] A. Ghosh, A.K. Jindal and A. Joshi, "A unified power quality conditioner for voltage regulation of critical load bus," in *Proc. IEEE Power Eng. Society General Meeting,* June 2004, vol.1, pp471-476**.**

[17] B.Singh and Venkateswarlu, "A Simplified Control Algorithm for Three-Phase Four-Wire Unified Powe Quality Conditioner", Journal of Power Electronics, vol.10, No.1, January2010.

[18] G. Chen ,Y. Chen and K.M. Smedley, "Three-phase four-leg active power quality conditioner without references calculation ,"in Procd. IEEE APEC '04, vol.1, pp.587-593, 2004.

[19] Vadirajacharya Kumar, P. Agarwal and H. O. Gupta, "A Simple Control Strategy For Unified Power Quality Conditioner Using Current Source Inverter," Procd. IPEC2007, pp.1219-1223.

[20] G. Bhuvaneswari, M. G. Nair and S. Kumar Reddy, "Comparision of Synchronous detection and ICosΦ Shunt Active Filtering Algorithm", Conf. IEEE PEDES'06,Dec.2006,pp.1-5.

[21] G. Bhuvaneswari and M. G. Nair, "Design, Simulation and analog Circuit Implementation of a Three-Phase Shunt Active Filter Using the ICosΦ Algorithm," IEEE Trans. on Power Delivery, vol.23, pp.1222-1235, April2008.


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