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The Approach for the Trade-off Study Between Field-effect Mobility and Current on/off Ratio in P3HT Field-effect Transistors

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Abstract: Presented herein are the results of the study that was conducted on the electrical characteristics of organic field-effect transistors based on poly(3-hexylthiophene), particularly the thickness and annealing temperature of their active layer is varied. The changes in field-effect mobility and current on/off ratio were explored. It was observed that both increasing annealing temperature from 60℃ to 100℃ and various concentrations influence the trade-off relations between the mobility and current on/off ratio. The surface morphology of the 2-μm^2 area with various thicknesses was scanned via atomic-forcemicroscopy(AFM) to verify the relationship between surface morphology, which is related to the thickness of the film, and device performance.

Keywords: Flexible, P3HT, Field effect mobility, Current on/off ratio

1. INTRODUCTION

In that the silicon solutions remain economically out of reach due to their high material and processing costs and their need for a complex fabrication system, the idea of organic electronics has become the subject of considerable interest [1,2]. Therefore, the attempts are being made to overcome the problem that was encountered with organic field effect transistors (OFETs). Through solution processing on plastic substrate, where devices can be fabricated at low temperatures and for a large area and low-cost fabrication points can be achieved using the flexible substrate through the roll to roll or printing process [3,4]. As a solution process enabled organic semiconductor, the P3HT is widely fabricated on the plastic substrate with various materials such as CNT (carbonnanotube) or polymeric dielectric for showing high performance transistors [5-7]. But, still there is a demanding for flexible materials and device configuration with all layers including gate dielectric layer, organic semiconductor layer, electrode and substrate. And the strategy to achieve the high electrical performance of polymer semiconductor while the device is consist of bendable materials needs well-interconnected crystal structures of organic semiconductor layer. The charge transport mechanism is strongly affected by the thermal treatment or optimized thickness because the major carriers are flow through the specific neighbored grain and a few charge transport layer [8,9]. And the field effect mobility and current on/off ratio is important factor to determine the appropriate process conditions, which serves the optimized performance [10,11].

Here, we present the trade-off relations between field effect mobility and current on/off ratio when devices are processed on the plastic substrate. The performance variance by annealing temperature and thickness was elucidated. The applicable experimental conditions for the high-performance and flexible substrate were considered, where the recommendable annealing temperatures of the

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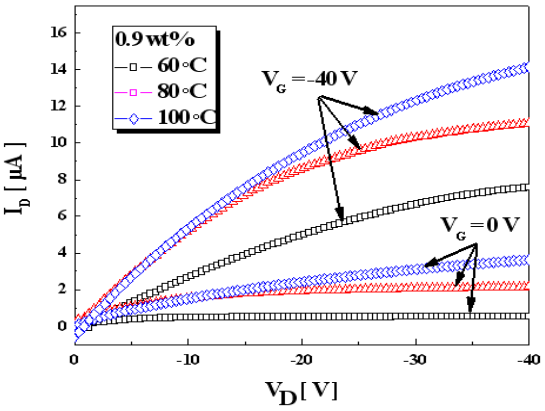

Fig. 1. Output curves of drain current versus drain voltage of RR-P3HT transistors at fixed annealing temperature with 0.3, 0.6, 0.9 wt% of P3HT concentration in chloroform.

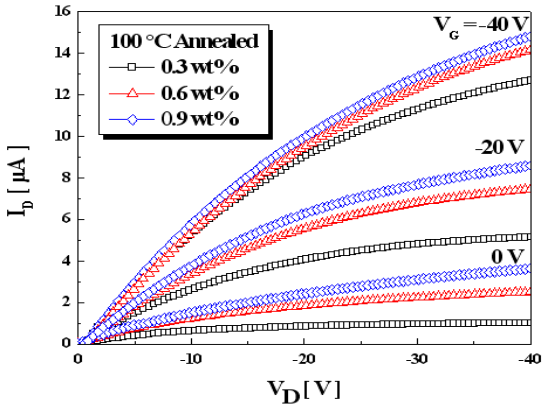

Fig. 2. Output cureves of drain current versus drain voltage at 0.9 wt% of RR-P3HT concentration in chloroform with various annealing temperature.

film must be limited to about its glass temperature. We also introduced organic gate dielectric layer by solution process for better interface effect to organic semiconductor. For the analysis of the origin of the relations between field effect mobility and the current on/off ratio, we measured the surface morphology of the spin-coated films. The electrical characteristics of fabricated devices show apparent tendency according to their thickness and annealing temperature. This fundamental trade-off study of P3HT OTFTs based on plastic substrate is interesting because the P3HT is solution process accessible and has large potential for flexible organic electronics.

2. EXPERIMENTS

We fabricated the thin film transistors on the CNT (carbon nanotube) coated film (TOP NANOSYS, Inc.). The sheet resistance is 400~500 Ω/sq according to the vender's information. The CNT coated polymer substrate is cleaned through continuous wet solutions of IPA (isopropyl alcohol) and de-ionized water in ultra sonic bath for 10 min. The cleaned samples are attached to glass substrate and carried to UV/Ozone treatment for removing organic contaminants. To make the bottom-gate TFTs (thin film transistors), the solution of 15 wt% (cyanoethylpullulan) CyEPL (Shin-Etsu Chemical Co., Ltd.) in the furfuryl alcohol as gate dielectric layer is prepared. To make complete mixture and stabilize the high-density solution, it is synthesized in room temperature for 6 hours. Then, it is spin-coated at 3,000 rpm for 30 sec and annealed at 110℃ for 30 min. The poly(3-hexylthiophene) P3HT (Aldrich Chem. Co.) was used as an active layer, which was dissolved in chloroform. The manipulation for thickness of the film was conducted through the weight concentration of P3HT in the solvent with a constant speed and dwelling time of the spin coater. We dissolved the different P3HT powder in organic solvent to make the 0.3, 0.6, and 0.9 wt% concentrations. And, Their corresponding thickness is 90, 140 and 190 nm, respectively. The annealing temperature range of 60~100℃ is introduced. The annealing treatment of P3HT is low than that of CyEPL to avoid swelling effect or cracking by the high thermal budget. The source and drain electrodes are placed after film formation to make top contact configuration by thermal evaporator. The electrodes were patterned through the open area of the shadow mask in the chamber. The W/L ratio between the source and drain electrodes was 500/100 in the micrometer scale.

The physical estimations of thin film are done using an atomic-force microscope (AFM). The surface of the P3HT film was scanned with an AFM within a 2×2-μ m^2 area. For the investigation of the thermal effects and nominal characteristics of the P3HT organic semiconductor

layer, which has severe sensitivity to the oxygen and moisture in the ambient, the most stable process manual that controls the molecular density and thickness of the channel layer based on the concentration of the organic solvent was considered. The current voltage (I-V) characteristics of field effect transistors are measured by semiconductor parameter analyzer (Keithley 4200 SCS) with the samples kept at room temperature and in a dark, shielded box.

3. RESULTS AND DISCUSSION

To elucidate the principle of current increase upon annealing temperature and current on/off ratio, we focus on the trade-off characteristics of P3HT film that molecular structure can be easily modified by its annealing temperature and film thickness. Because it can be explained by the evident from the assorted mechanisms of molecular-structure formation, which is affected by the thermal budget and the amount of buried solvent when it is cross-linked [12,13].

In Fig. 1. the variance of drain current according to the different thickness of active layer was revealed. To exclude the insufficient cross-linking from low annealing temperature below the boiling temperature of solvent, the annealing condition is fixed to 100℃. The plot of drain current versus drain voltage indicates that the drain current is increased as the thickness is increased. We can know that the interval value in difference of increased current is not linearly modulated to the concentrations of samples. This result means that the amount of accumulated charges at the interface between semiconductor and dielectric have its limitation in conduction depending on its total thickness of film [14]. Thus, it can be expected that the effective current path near the gate dielectric is critical factor in our device structure. In addition, the deficiency at the saturation regime is explained by the punch-through phenomena of conventional principal in (MOSFETs) metal oxide semiconductor field effect transistors [15].

In Fig. 2. the concentration of P3HT in chloroform is fixed at 0.9 wt%. The reason we fixed the thickness of film to 0.9 wt% is that the effect of annealing temperature

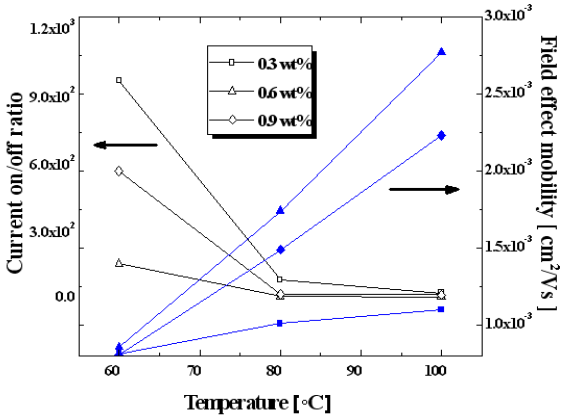

Fig. 3. The plots of current on/offf ratio and field effect mobility depending on annealing temperature with 0.3, 0.6, 0.9 wt% of P3HT in chloroform.

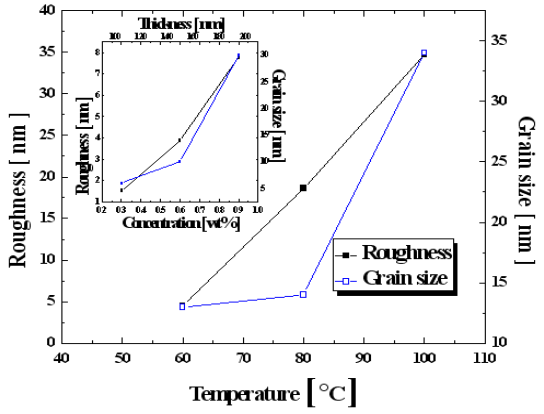

Fig. 4. The plots of roughness and grain size for different annealing temperature at 0.9 wt% of P3HT films. Inset shows the same upon different concentration of P3HT in chloroform at 100℃.

on P3HT organic semiconductor can be dominant in thick film, which needs more thermal budget than thin film. The graph shows the increased drain current as the annealing temperature which implies the thermally activated charge transport contribute to the current increase. This results of effect of annealing temperature on field effect mobility of organic semiconductor is proved through many groups [16,17].

In Fig. 3. the increased thermal budget to film formation takes active part in the increased field effect

mobility. But, the current on/off ratio is decreased despite of the large increase in the field effect mobility at high annealing temperature. This result originated from the fact that the off current or gate leakage has been increased at zero gate voltage. The two of 0.6, 0.9 wt% of P3HT films show steep slope of field effect mobility to annealing temperature than 0.3 wt% of P3HT film. This means the thicker film contains more dense molecular structure and pi-bonding. But the highest weight concentration at 0.9 wt% of P3HT shows decreased field effect mobility due to its over-thickness which needs higher thermal budget to form sufficient cross-linking. Also, the bulk state film over effective channel layer contributes to additional leakage path between source and drain. The degradation is revealed at reduced current on/off ratio. And, the trend of current on/off ratio has the point of inflection at 0.6 wt%.

Figure 4 shows the calculated roughness and thickness from the AFM of samples. As shown in the result from Fig. 4. the increase in thickness of films by weight concentration of P3HT incur the increased roughness as well as the large grain size. This is because of the relatively low centrifugal force when film is deposited by spin coating method at the same revolution speed. The increased grain size along with annealing temperature is the evident of increased field effect mobility. The increased roughness of the above samples implies increased trap charge state at the interface between organic semiconductor layer and gate dielectric layer or top-contact electrodes. Therefore, we can estimate the leakage current from trap charges induce the unwanted off current at negative gate voltage. Then, the trade off relations at thick film and high annealing temperature is attributed to the leakage paths.

4. CONCLUSION

In summary, we fabricated the P3HT based flexible field effect transistor on the CyEPL/CNT coated plastic substrate. Then, the trade off relations between field effect mobility and current on/off ratio under various thicknesses and annealing temperature was discussed. The factor that enhances the field effect mobility was the grain size, which is originated from thermal annealing and thick film. But, the bulk state of the film donates leakage current so that the current on/off ratio was decreased. This result can be proved by the theory of effective channel layer and leakage path problem which generates increased off current. It means that the appropriate conditions for reducing gate leakage upon annealing temperature and film thickness is important to mitigate the trade off relations. From this work, we found the controlling the leakage paths is helpful to optimize the performance on the flexible substrate which needs low-temperature process.

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