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Effects of Post Annealing on the Electrical Properties of ZnO Thin Films Transistors

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This paper reports the effects of post-annealing of ZnO thin films on their microstructure and the device performance of the transistors fabricated from the films. From X-ray diffraction and transmission electron microscopy characterization, we uncovered that the grain size increased with the annealing temperature escalating and that the film stress shifted from compressive to tensile due to the grain size increment. Electrical characterization revealed that the grain size increase damaged the device performance by drastically lifting the off-current level. By annealing the devices in an O_2 ambient (instead of air), we were able to suppress the off-current while improving the electron mobility.

Key Words: ZnO, Thin-film transistor, Grain size, Electron mobility, Thin film stresses

INTRODUCTION

Research interests on ZnO-based thin film transistors (TFTs) are on rise (Bae & Im, 2004; Fortunato et al., 2005; Yao & Li, 2005; Sun & Rogers, 2007). ZnO and its derivatives (InGaZnO, SnZnO, InZnO, etc) offer a unique combination of technologically important features such as a high electron mobility, an excellent transparency, and a stability superior to that of amorphous silicon (Normura et al., 2004). Successfully developing them for transistors could enable some next-generation electronics including transparent electronics and flexible electronics. Vigorous research activities are in progress in harnessing this class of materials as the channel layer of TFTs to achieve a high device performance. In particular, understanding the fundamentals of these materials and its influence on the device performance is an integral part of these research efforts (Bae et al., 2003; Carcia et al., 2003; Hoffman et al., 2003; Norris et al., 2003). For instance, ZnO thin films are typically polycrystalline and the electrical properties of the transistors based on these films are expected intimately related to their microstructural features such as grain boundaries (Hossain et al., 2003). Here, we annealed ZnO films to modulate the microstructure, and examined the effects of the annealing on the microstructure of the ZnO films and the electrical properties of their transistors.

Among various deposition methods, radio frequency (RF) magnetron sputtering technique is widely adopted owing to its process simplicity and wide-area deposition capability (Hwangbo et al., 2008; Kim et al., 2008; Sahu et al., 2008; Venkatachalam et al., 2008). The microstructure of sputtered ZnO films are known very sensitive with the process conditions (such as deposition power, partial oxygen pressure, and post-deposition annealing) and hence the device performance (Levinson et al., 1982). Fortunato et al. (2005) reported the effects of the RF power on the crystallinity and Hall mobility of ZnO films while other studies embarked

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on the effects of the partial oxygen pressure during the deposition and post-annealing in hydrogen environment (Bae et al., 2003; Carcia et al., 2003). In our previous study, we employed different RF powers to generate ZnO films with different grain sizes and demonstrated a sensitive increase of the electron mobility with the grain size (Hwang et al., 2008). Despite the efforts to elucidate the role of the microstructure, the effects of post annealing - the most widely-used way of altering the microstructure of polycrystalline films - on the device performance have not been thoroughly investigated. Here, we annealed ZnO films at various temperatures under different ambients (air and O_2) and delved into how the annealing affected the overall microstructure of the ZnO films and furthermore the electrical properties of the TFTs.

MATERIALS AND METHODS

Fig. 1 shows a schematic diagram of the device structure

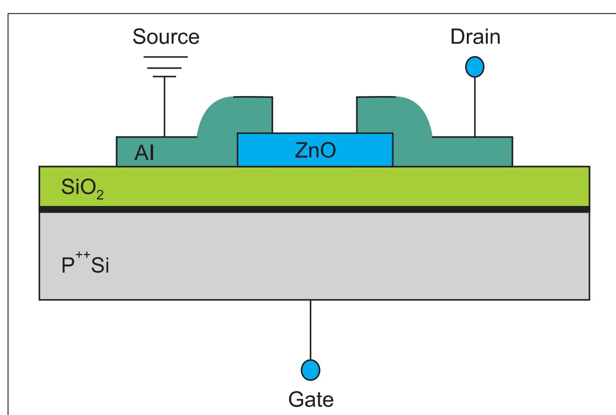


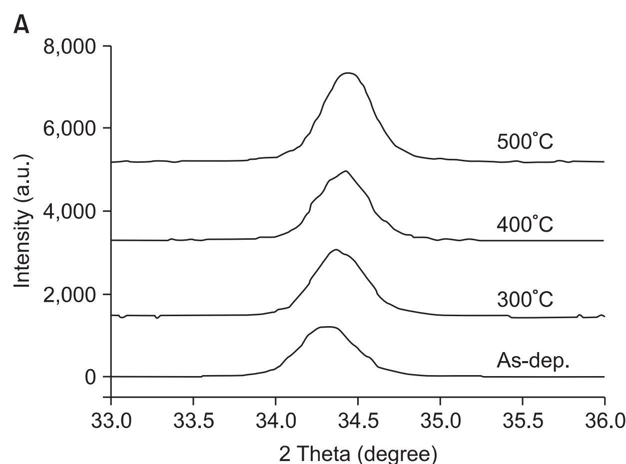
Fig. 1. A schematic diagram of the device structure used in this study.

adopted in this study, which is based on a bottom-gated TFT structure and utilizes a highly doped Si substrate as the gate electrode. First, SiO_2 gate dielectric with the thickness of 100 nm was thermally grown on a highly-doped p-Si (100) wafer (0.001~0.005 Ωcm), followed by deposition of an undoped ZnO active layer in an Ar ambient of 10 mTorr in a RF (13.56 MHz) magnetron sputtering system. The substrate temperature was room temperature and the sputtering power was set to 50 W. The ZnO films were deposited through a shadow mask having a size of 500×1,140 μm to define the active channel regions.

After the deposition of ZnO films, thermal annealing was performed at various temperatures (300°C, 400°C, and 500°C) in different ambients (air and O_2) for 1 hour in a furnace. As the source and drain electrodes of the transistors, Al films were deposited using a thermal evaporation system and patterned using a typical lift-off process. The channel width (W) and length (L) of the fabricated TFTs were 100 μm and 50 μm, respectively. To reduce the contact resistance, rapid thermal annealing was carried out at 200°C for 2 min in N_2 ambient. The electrical characteristics of the transistors were measured using an Hewlett-Packard (HP) semiconductor parameter analyzer (HP4145B). We conducted microstructure analysis on the deposited ZnO films using X-ray diffraction (XRD) and transmission electron microscopy (TEM).

RESULTS AND DISCUSSION

Shown in Fig. 2A are XRD curves obtained from ZnO films, as-deposited and annealed at various temperatures (300°C, 400°C, and 500°C). For all the samples, the XRD curves show the dominant peak around 34.3°, the position of which is coincident with that of the (0002) reflection of the hexagonal ZnO phase. This result represents the presence of a strong



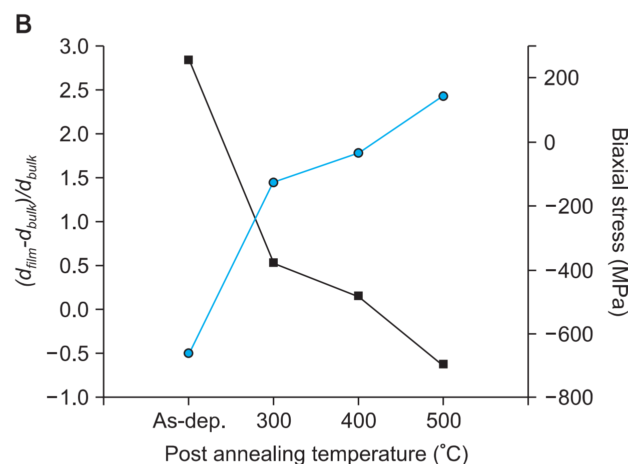


Fig. 2. (A) XRD data obtained from θ~2θ scans for ZnO films, as-deposited and annealed at various temperatures (300~500°C), and (B) a graph of $(d_{film}-d_{bulk})/d_{bulk}$ and biaxial stresses for the as-deposited and annealed samples. XRD, X-ray diffraction.

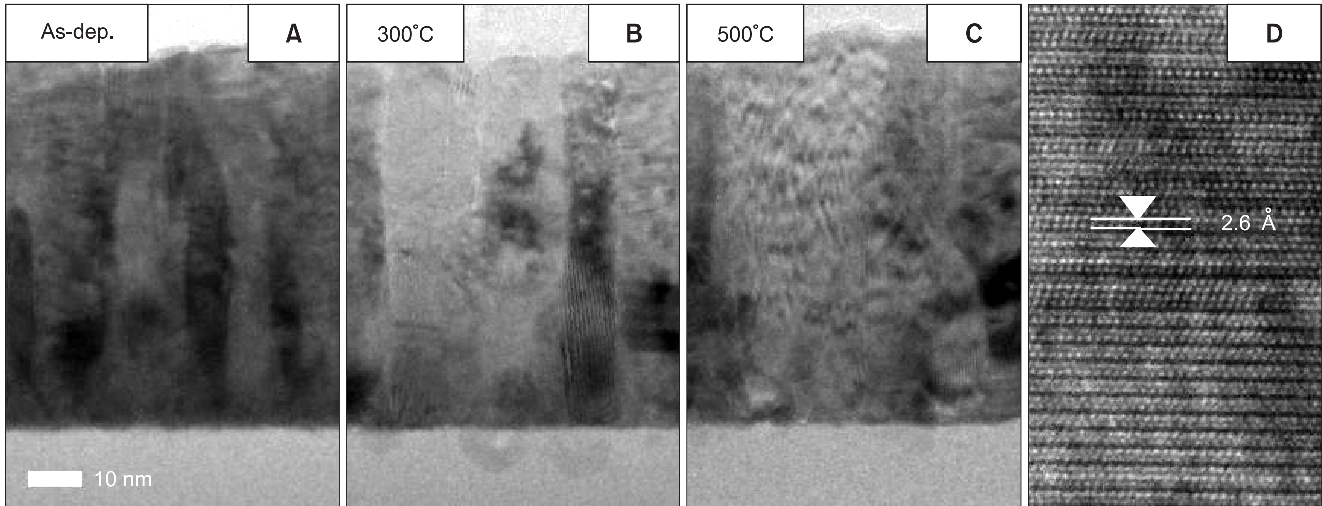


Fig. 3. Bright-field TEM images of ZnO films. (A) As-deposited, (B) annealed at 300°C, and (C) annealed at 500°C. The high resolution image shown in (D) was taken from the sample annealed at 300°C. TEM, transmission electron microscopy.

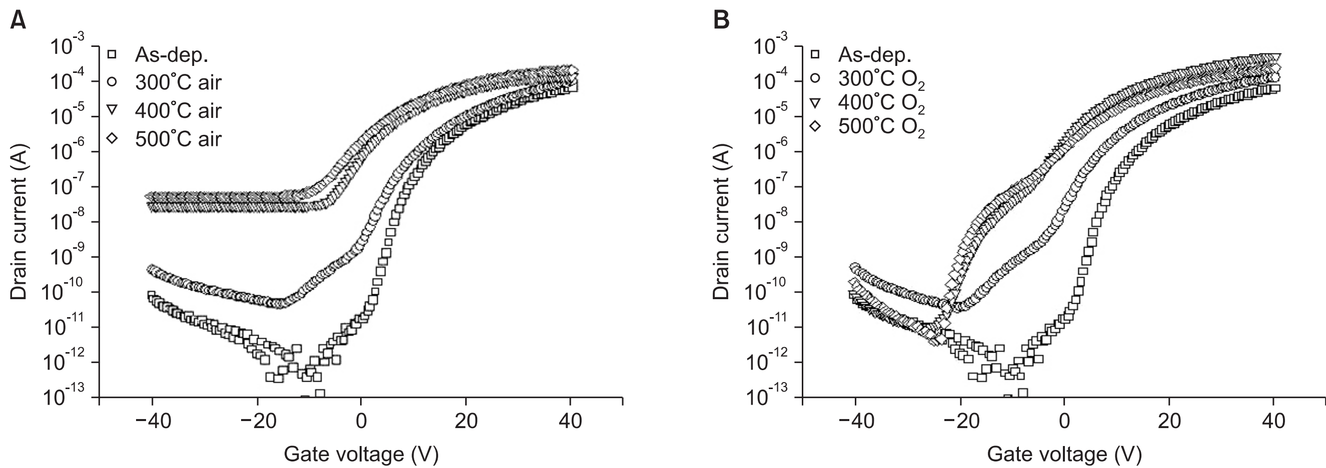


Fig. 4. Transfer curves of TFTs fabricated from the as-deposited and annealed ZnO films in an ambient of (A) air and (B) O_2. Note: the drain voltage was set to 10 V. TFTs, thin film transistors.

(0002) texture in the films. The intensity of the peak escalates with the annealing temperature increasing, signaling an improvement in the crystallinity of the films (that is, the increment of the grain size).

Another noticeable feature observed in the graph is a systematic shift in the peak position for the samples annealed at elevated temperature. In the XRD curves of thin films, the shift of a peak position usually arises from bi-axial stresses present in the films (Venkatachalam et al., 2008). Fig. 2B shows the strain of the films in the film-normal direction [$\varepsilon=(d_{film}-d_{bulk})/d_{bulk}$] measured from the shifts of the (0002) peak position. From this measurement, we could estimate biaxial stresses in the films using the following relationship (Sahu et al., 2008).

$$\sigma_{film}=\frac{2c_{13}^2-c_{33}(c_{11}+c_{12})}{2c_{13}}\cdot\varepsilon$$

For the elastic constants c_{ij}, the data obtained from single crystalline ZnO could be used: c_{11}=208.8, c_{33}=213.8, c_{12}=119.7, c_{13}=104.2 *GPa* (Cebulla et al., 1998). From this calculation, we determined the biaxial stresses of our samples, as shown in Fig. 2B. The as-deposited film was found in a compressive stress (~700 MPa), consistent with other studies on ZnO thin films, which report a film stress of 200~600 MPa and attribute the origin of the stress to atomic peening occurring during sputtering (Cebulla et al., 1998; Zhang et al., 2004; Li et al., 2007). The graph also displays a stress relaxation after annealing. The compressive stress continues to decline with

the annealing temperature increasing until the stress becomes tensile upon annealing at 500°C. This shift of the stress state, from compressive to tensile with the temperature rising, could be explained in connection with the grain size increase confirmed earlier from the peak intensity increase, since a grain size increase means a reduction in the grain boundary area, which would entail the development of a tensile stress in the film.

TEM characterization revealed the details of the microstructure of the ZnO films, which closely parallel with the XRD results, as shown in the bright field images of Fig. 3A-C. The image taken from the as-deposited sample displays a typical columnar structure, in which the grains were grown vertically with a width of around 8 nm. The images also disclose that the columns of the grains became wider upon annealing at 300°C and the grains grew further for the sample annealed at a higher temperature (500°C), which agrees well with the XRD results. In high resolution imaging, the grains dominantly display the lattice images of (0002) planes, as shown in Fig. 3D, which affirms the strong (0002) texture of our films observed in the XRD curves.

Next, we characterized the electrical properties of the transistors fabricated from the as-deposited and annealed ZnO films, as shown in the transfer curves of Fig. 4. The drastic change of the shapes of the curves shown in the graph marks a strong influence of the annealing. Raising the annealing temperature did not only increase the on-current but also the off-current level drastically from 10^{-11} A to 10^{-7} A. The rise of the on-current contributed to the increase of the mobility for the samples annealed at higher temperatures, which was largely shadowed by the concurrent drop of the

Table 1. The summary of the electrical properties of the TFTs

	Mobility (cm^2/V·s)	Threshold voltage (V)	On/off ratio current	Subthreshold slope (V/dec.)
As-dep.	2.3	11.7	~10^7	1.5
300°C	3.4	10.57	10^6	2.1
400°C	3.8	–0.38	$10^{4.5}$	2.5
500°C	4.9	–2.08	$10^{3.5}$	2.7

TFTs, thin film transistors.

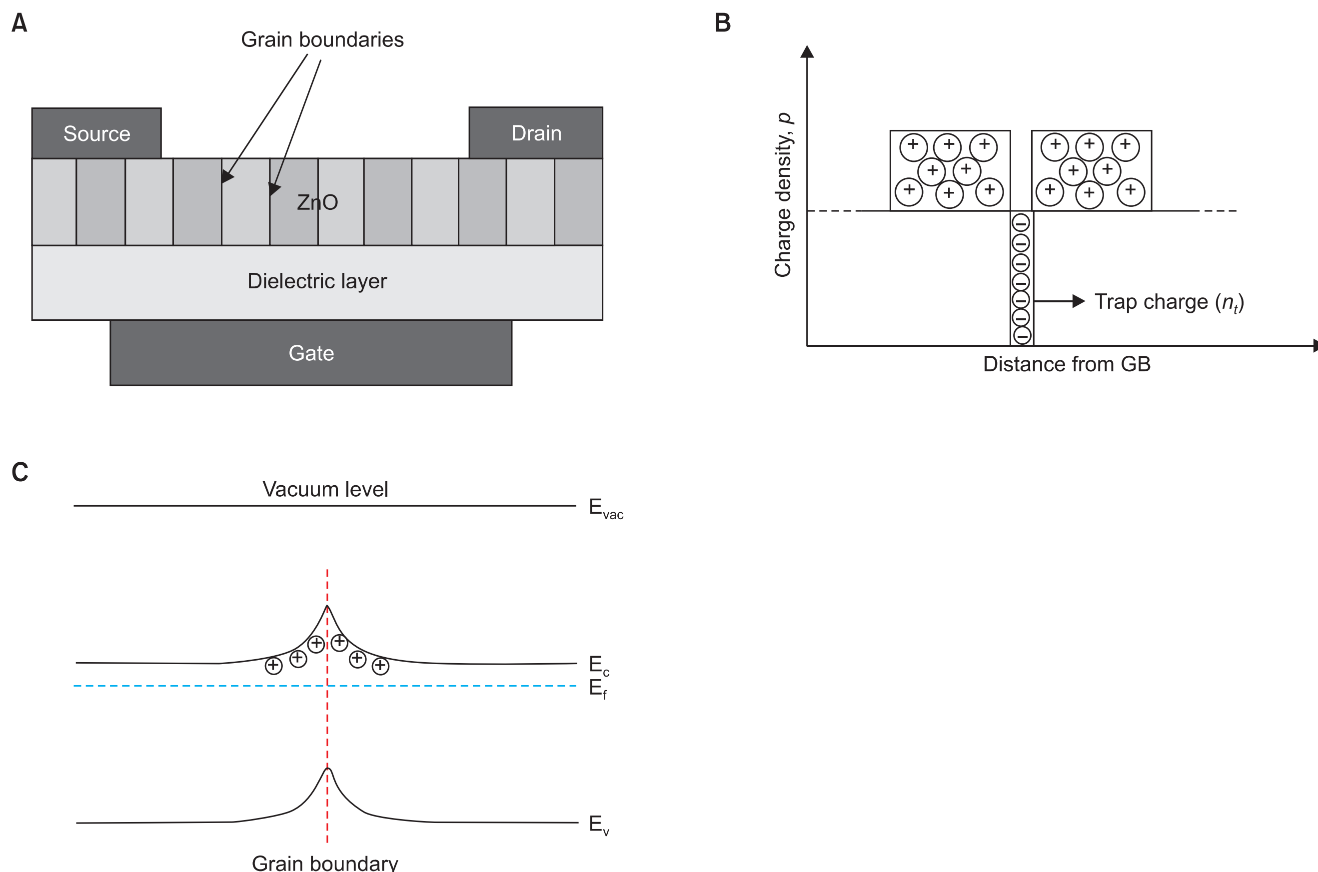


Fig. 5. (A) A schematic diagram of TFT with a ZnO channel layer populated with vertical grain boundaries, (B) the distribution of charges in the vicinity of a grain boundary, and (C) an energy band diagram that shows the formation of a double Schottky barrier around a grain boundary (redrawn from Hossain et al., 2003). TFT, thin film transistor; GB, grain boundary.

on/off-current ratio due to the off-current surge (see Table 1 for the details of the device performance).

Such a drastic rise of the off-current level generally means a significant increase in the background carrier concentration in the ZnO films. In the framework proposed in a study on modeling of polycrystalline ZnO-based TFTs, this behavior could be connected to the grain size increase caused by the annealing (Singh et al., 2007). In this model, as schematically illustrated in Fig. 5, grain boundaries - treated as a thin layer full of trap sites - capture charge carriers in the vicinity, which leads to the formation of depletion regions and double Schottky barriers in the energy band diagram, as illustrated in Fig. 5C. As such, the reduction of grain boundary areas would result in a drop in the trapped charge density and hence an increase in the free charge carrier concentration. Thus, while the increment of the grain size could improve the electron mobility by reducing the number of potential barriers, it could also critically damage the device performance by raising the background carrier concentration and thus increasing the off-current level.

Next, we annealed some samples in O_2 ambient in an attempt to suppress the off-current rise by infusing oxygen into the films during annealing and thereby reducing the concentration of oxygen vacancies, the major source for charge carriers. Shown in Fig. 4B are transfer curves obtained from the samples. The curves are in a sharp display of the effects of the O_2 annealing: As the annealing temperature increases, the off-current rises only slightly while the on-current increases substantially. The electron mobility also improved significantly from 2.3 $cm^2/V \cdot s$ for the as-deposited samples to 5.0 $cm^2/V \cdot s$ for the 500°C annealed samples. One unusual feature of the curves obtained from the samples annealed at high temperatures (300°C-, 400°C-, 500°C-annealed samples in O_2 ambient, and 200°C -annealed samples in air) is the presence of a small shoulder peak around the turn-on voltage. We suggest that such shoulder peaks might arise from two possibilities, gate leakage and the presence of a parasitic channel layer. Further investigation is in progress to acquire full understanding of this behavior and to improve the device performance.

SUMMARY

In this study, we investigated the effects of post-annealing of ZnO thin films on their microstructure and the device performance of the transistors fabricated from the films. From XRD and TEM characterization, we uncovered that the grain size increases with the annealing temperature escalating and that the film stress shifts from compressive to tensile because of the grain size increment. From electrical characterization of the devices, we found that although the grain size increase raised the on-current by reducing the number of potential barriers, it also critically damaged the device performance by raising the background carrier concentration and thus increasing the off-current level. We also confirmed that annealing the devices in an O_2 ambient (instead of air) suppressed such off-current rise by infusing oxygen into the films while improving the electron mobility.

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