A Low Power Dual CDS for a Column-Parallel CMOS Image Sensor

Kyuik Cho, Daeyun Kim, and Minkyu Song

Abstract—**In this paper, a 320 × 240 pixel, 80 frame/s CMOS image sensor with a low power dual correlated double sampling (CDS) scheme is presented. A novel 8-bit hold-and-go counter in each column is proposed to obtain 10-bit resolution. Furthermore, dual CDS and a configurable counter scheme are also discussed to realize efficient power reduction. With these techniques, the digital counter consumes at least 43% and at most 61% less power compared with the column-counters type, and the frame rate is approximately 40% faster than the double memory type due to a partial pipeline structure without additional memories. The prototype sensor was fabricated in a Samsung 0.13 μm 1P4M CMOS process and used a 4T APS with a pixel pitch of 2.25 μm. The measured column fixed pattern noise (FPN) is 0.10 LSB.**

Index Terms—**CMOS image sensor, correlated double sampling, digital CDS, dual CDS**

I. INTRODUCTION

CMOS image sensors have been widely used in various applications such as digital cameras, digital camcorders, CCTV, car security cameras, medical equipment, and so on. Because of the characteristics of the products, research with the aim of achieving a low level of noise in order to improve the image quality has become a major concern. In particular, fixed pattern noise (FPN) generated by non-uniformity of pixels and readout circuits including analog to digital converters (ADC) is a major factor causing noise in a column-parallel CMOS image sensor [1-11].

In general, correlated double sampling (CDS) scheme has been used to eliminate the FPN by subtracting signal voltage (V_{SIG}) – which contains the photoinduced signal and offset of circuits – from reset voltage (V_{RST}) – which contains only offset of circuits – at the pixel output (V_{PIX}). There are two methods to implement CDS: analog CDS [8-16] and digital CDS [1-3].

The analog CDS finishes the CDS before A/D conversion by using capacitors and switches, as shown in Fig. 1(a). Although the analog CDS circuit has been widely used because it is easy to design and operate, it is difficult to improve the accuracy [5] when using this circuit because of a capacitance mismatch, a clock feed-through error at the switch, and so on.

On the contrary, the digital CDS performs the subtraction during double period of A/D conversion by

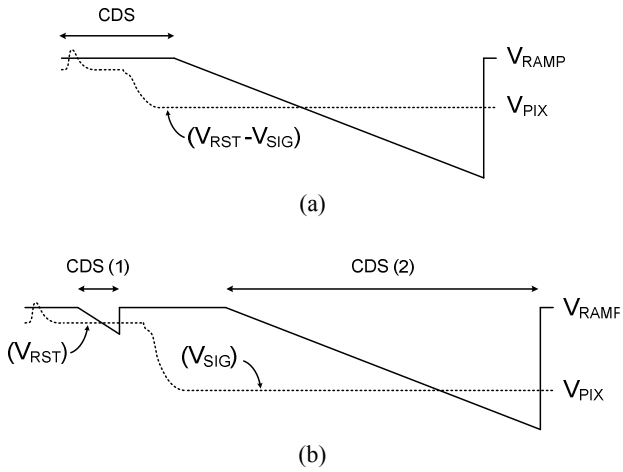

Fig. 1. Correlated double sampling (a) Analog CDS, (b) Digital CDS.

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using digital circuits, as shown in Fig. 1(b). The two ways of conventional digital CDS – one is double memory type [1] and the other is column-counters type [2-7] – are shown in Fig. 2.

The simple principle of the double memory type is as follows. First, the column-ADCs perform the A/D conversion for the V_{RST} and store in the first memory. After that, V_{SIG} is converted and stored to the second memory in the same way. Finally, the digital codes of the effective signal voltage (V_{eff_SIG}) are taken by subtractor connected to two memories at the end of the readout circuit.

The basic principle of the column-counters type is shown in Fig. 3 where the comp out is the output of the comparator and the CDS clock is an essential clock for the digital CDS. First, the column-counters (up/down counters) down count and take the difference between top voltage (V_{TOP}) and V_{RST} during the first period of A/D conversion. At this time, the first conversion time is suppressed to 256 counts because the V_{RST} variation is much smaller than the V_{SIG} variation. After that, the

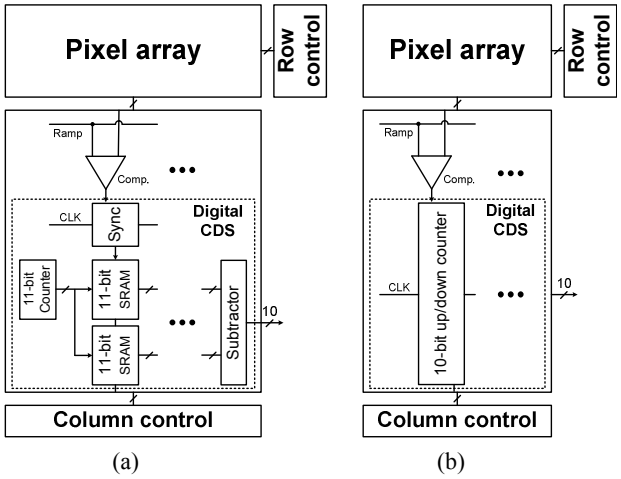

Fig. 2. Conventional digital CDS (a) Double memory type, (b) Column-counters type.

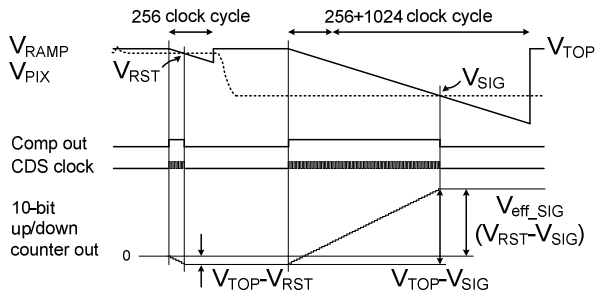

Fig. 3. Timing diagram of digital CDS with column-counters.

up/down counters up count until the V_{SIG} is equivalent to the ramp signal (V_{RAMP}) during the second period of A/D conversion and the difference between V_{TOP} and V_{SIG} is taken. As a result, the up/down counters stored digital codes of V_{eff_SIG} because of subtracting V_{TOP} - V_{RST} from V_{TOP} - V_{SIG}.

The digital CDS or dual CDS [4-7] which uses both analog CDS and digital CDS enables the resolution of CDS to improve beyond 10-bit. Nevertheless, they also have drawbacks. Fundamentally, they have a low conversion speed because of digital double sampling for comparison of the reset and the signal [1-7]. Furthermore, the double memory type consumes a greater area and more power because the architecture needs an 11-bit global counter and two 11-bit memories in every column to achieve 10-bit resolution, and four 11-bit memories are required for the pipeline structure to realize a high frame rate. Although high speed CMOS image sensors based on a column-counters have been recently reported in [2-7], they use a complex design and their power consumption and chip area are unacceptably large for applications that require low power and a small pixel pitch.

In this paper, a CMOS image sensor with a column-parallel single-slope ADC (SS-ADC) and a dual CDS which consists of an analog CDS circuit and a digital CDS circuit is described. To realize low power consumption and low digital switching-noise without decreasing the speed which is generated by the digital double sampling, a new and simple digital counting algorithm with an 8-bit counter – a hold-and-go counter – which has a satisfactory resolution of 10-bit or beyond is presented. Furthermore, in order to improve energy efficiency, we also propose a configurable counter scheme which selects the bit number of the digital counter according to the changed analog gain.

This paper is organized as follows. Section II describes the architecture of the proposed CMOS image sensor. Section III shows the circuit description of the image sensor. Section IV presents the measurement results. Finally, the conclusion and directions for future work are provided in Section V.

II. ARCHITECTURE

Fig. 4 shows the block diagram of conventional CMOS image sensor based on a column-parallel SS-

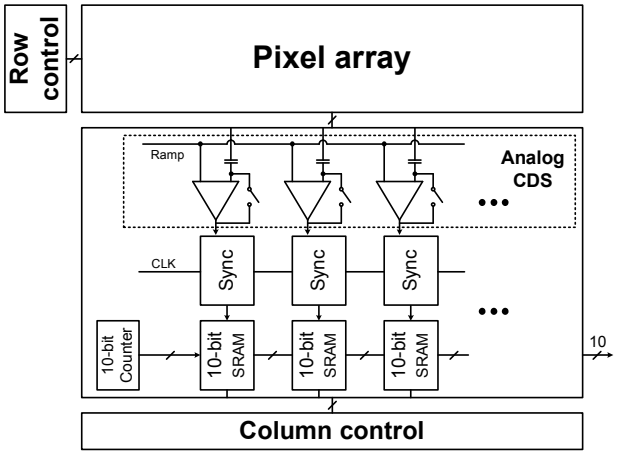

Fig. 4. Block diagram of conventional CMOS image sensor.

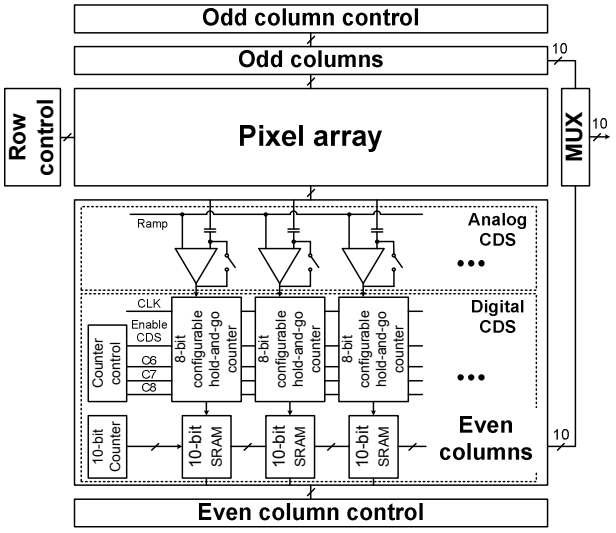

Fig. 5. Block diagram of the proposed CMOS image sensor.

ADC. A conventional image sensor [11] and the proposed image sensor with the dual CDS have almost same architecture except for the sync block. The block diagram of the proposed image sensor is shown in Fig. 5. The image sensor is composed of a pixel array, two side column parallel readout circuits, and digital control blocks. The pixel array is based on the 4T two-shared pinned-photodiode [11, 14] with a pixel pitch of 2.25 μm. The readout circuits consist of the analog CDS circuits, SS-ADCs, 8-bit configurable hold-and-go counters for digital CDS, 10-bit SRAMs, a global 10-bit counter and a configurable counter control block. A row control block, a column control block, and a multiplexer (MUX) are included in the digital control block. The two side column structure – with odd columns and even columns – expands the column pitch from 2.25 μm to 4.5 μm, thereby preventing errors generated by small column pitch [3].

Pixel and analog CDS circuit is shown in Fig. 6 and Fig. 7 shows the block diagram of the proposed 8-bit configurable hold-and-go counter. The counter plays the role of digital CDS circuit and sync block at the same time.

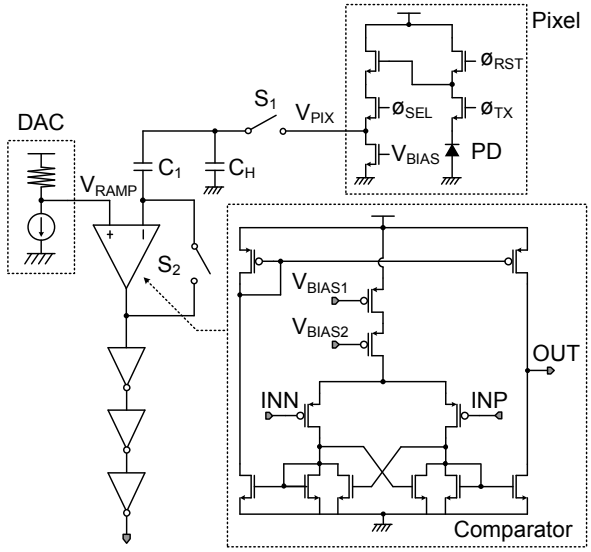

Fig. 6. Pixel and analog CDS circuit.

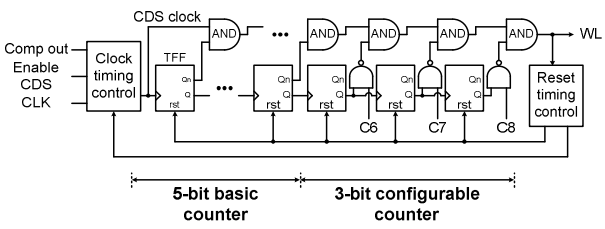

Fig. 7. Block diagram of the proposed 8-bit configurable hold-and-go counter.

III. CIRCUIT DESCRIPTION

1. Dual CDS with Hold-and-Go Counter

Fig. 8 shows the timing diagram of the dual CDS using an 8-bit hold-and-go counter for the 10-bit resolution CMOS image sensor compared with the previous digital CDSs [2-6]. In the previous digital CDSs – of column-counters type –, the output signals are obtained from the difference between the V_{RST} and the V_{SIG} while all 10-bit column-counters are operating. Therefore, a maximum 256 clock cycle is needed at the first period of A/D conversion [T2 + T3], and a maximum 256 + 1024 clock cycle is needed at the second period of A/D conversion

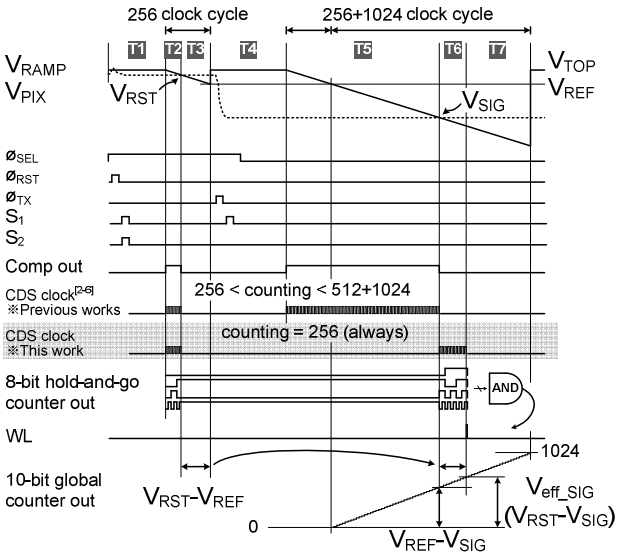

Fig. 8. Timing diagram of the dual CDS with the hold-and-go counter.

[T5 + T6 + T7]. Although this type of CDS realizes high speed because a global counter is unnecessary, their power consumption and chip area are unacceptably large for applications which require low power and small pixel pitch.

From the Fig. 8, the simple explanation of the proposed dual CDS with the 8-bit hold-and-go counter is as follows. 1) The V_{RST} is appeared by resetting all the pixels of a row (controlled by $ø_{RST}$). After that, switches connected to the pixel output (S_1) are closed to charge holding capacitors (C_H) with the V_{RST}, and simultaneously the other switches connecting input and output of the comparators (S_2) are closed to eliminate the offset of circuits [T1]. 2) When the ramp signal starts for the first comparison, all the 8-bit counters in every column also start working [T2]. 3) When the ramp signal is equivalent to the V_{RST}, the counters stop and hold the digital codes [T3]. 4) The V_{SIG} is appeared (controlled by $ø_{TX}$) and the S_1 is closed again to drive the V_{SIG} [T4]. 5) The second ramp signal starts to capture the V_{SIG} and after 256 clock cycle, a global 10-bit counter starts working [T5]. We don't need to count 256 for the 2nd ramp using another counter, because the operation of global counter is always the same. 6) When the ramp signal is equivalent to the V_{SIG}, the 8-bit counters begin working again – thus we call the counter "hold-and-go" – and at this time, the 10-bit global counter output is the digital codes of V_{REF} - V_{SIG}. After that, when all the output codes of the 8-bit hold-and-go counter are high through AND gates, the digital codes of the global 10-bit counter are stored at the column memories [T6]. The stored data is the corrected digital signal (V_{eff_SIG}) because the period of T3 is equal to T6 and the sum of the V_{REF} - V_{SIG} and the V_{RST} - V_{REF} is the V_{eff_SIG} (V_{RST} - V_{SIG}) where the V_{REF} is defined as V_{TOP} - 256 V_{LSB}. 7) The 8-bit hold-and-go counter is stopped and reset to zero by both the clock timing control block and the reset timing control block [T7].

In this algorithm, the hold-and-go counters just control the timing when the memories store the digital codes generated by a global 10-bit counter. We can reduce the power consumption and the switching noise compared with the column-counters type because the 8-bit hold-and-go counter is sufficient to satisfy the 10-bit resolution requirement, and this means that a clock cycle of only 256 is enough to realize the desired 10-bit resolution. Furthermore, because the subtraction is completed in the columns, the conversion error is reduced and an extra subtractor is unnecessary, in contrast to double memory type sampling.

2. Partial Pipeline Structure

Generally, additional memories are utilized to pipeline the A/D conversion of the Nth row and the horizontal data transfer of the N-1th row to give a high frame rate despite the large area of occupancy [3, 5, 10, 12]. A column SS-ADC with digital CDS, in particular, needs a pipeline structure because it suffers from low conversion speed owing to the digital double sampling. On the other hand, the proposed digital CDS pipelines the partial period of A/D conversion of the Nth row and the horizontal data transfer of the N-1th row without using any more memories. Fig. 9 shows the horizontal readout sequence. This solves the problem of decreasing speed due to digital double sampling, thereby increasing the frame rate by approximately 40% with a relatively low power and small area.

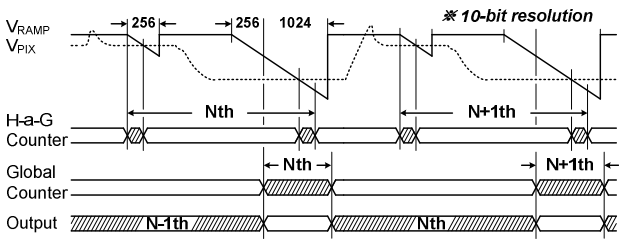

Fig. 9. Horizontal readout sequence.

3. Dual CDS and Configurable Counter Scheme

A dual CDS architecture employing an analog CDS as well as a digital CDS is implemented to reduce noise, improve conversion speed, and decrease power consumption. An advantage of the dual CDS is that it has a high noise suppression capability because FPN cancellation is performed in both the analog domain and the digital domain [5]. Additionally, in this paper, the analog CDS, which reduces the period of A/D conversion for the reset voltage by eliminating the analog offset of the pixel and the comparator output, enables high speed conversion and low power consumption because the 5-bit (32 clock cycle) hold-and-go counter in each column is sufficient to provide the desired 10-bit resolution, as shown in Fig. 10.

Although the period of A/D conversion for the reset voltage is reduced by using analog CDS in the dual CDS architecture, the required bit number of the hold-and-go counter is increased when the slope of the ramp signal is decreased for high analog gain. The high analog gain changes the total level of light into bright level and makes it easy to distinguish the light level, despite reducing treatable range of light input. For example, when the analog gain is changed from 1× to 8×, the bit number of the counter should be changed from 5-bit to 8-bit (256 clock cycle) again, as shown in Fig. 11.

The configurable counter scheme using this principle is applied to the hold-and-go counter in order to reduce the power consumption efficiently. Fig. 12 shows the

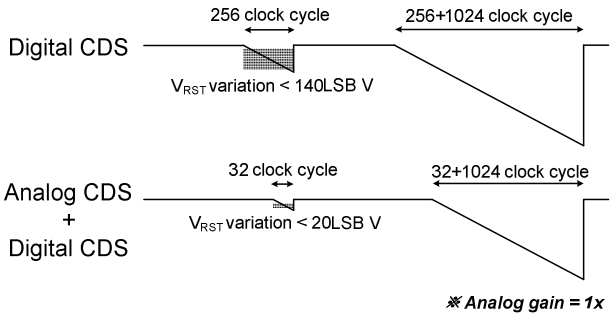

Fig. 10. The effect of dual CDS.

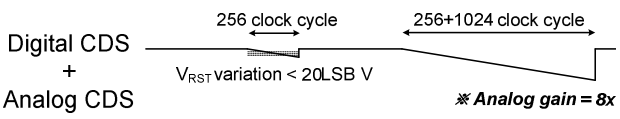

Fig. 11. Analog gain and dual CDS.

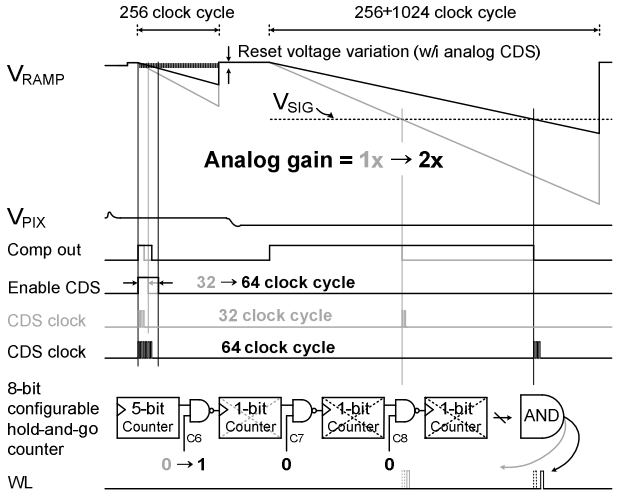

Fig. 12. Processing of the configurable hold-and-go counter according to the changed analog gain.

processing of the configurable hold-and-go counter. The counter is composed of a 5-bit basic counter and a 3-bit configurable counter. When the analog gain is changed from 1× to 2×, the bit number of the counter is also changed from 5-bit to 6-bit. In the same way, bit numbers of 7-bit and 8-bit are selected when the analog gain is 4× and 8×, respectively. The bit number is controlled by the signal of Enable CDS and NAND inputs. Therefore, we can reduce the power consumption and switching noise efficiently.

IV. MEASUREMENT RESULTS

The prototype CMOS image sensor was fabricated by a 0.13 μm 1P4M CMOS process. A chip microphotograph is shown in Fig. 13. A pixel array of 320 × 240 was implemented with 2.25 μm pixel pitch. The column pitch is 4.5 μm by using a two side column structure. Although the effective chip area is 1.5 mm × 2.2 mm, the total chip area including bond pads is 5 mm × 5 mm due to the number of pads being increased for verification of the test block and some nodes. The silicon area of a digital CDS circuit is only 4.5 μm × 190 μm.

We employ an off-chip field programmable gate array (FPGA) to generate the various clock signals controlling the image sensor, and change the signals flexibly. To generate the clock signals, we transfer the Verilog code from the computer to the FPGA through a USB interface. After that, the FPGA transfers the clock signals to the image sensor, receives data outputs from the image

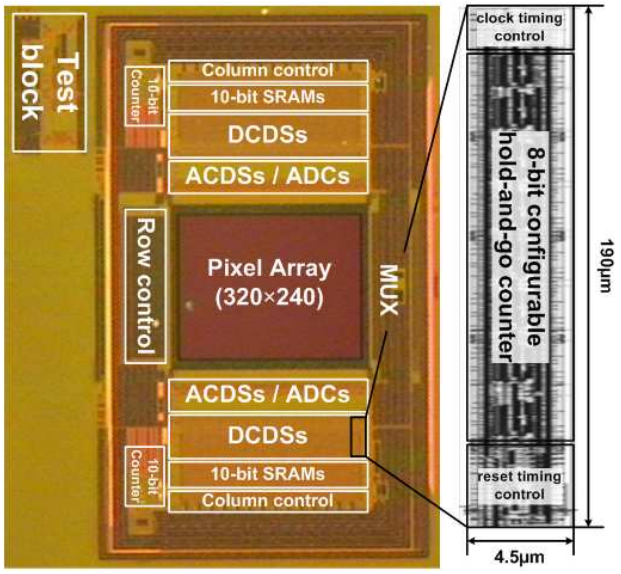

Fig. 13. Chip microphotograph.

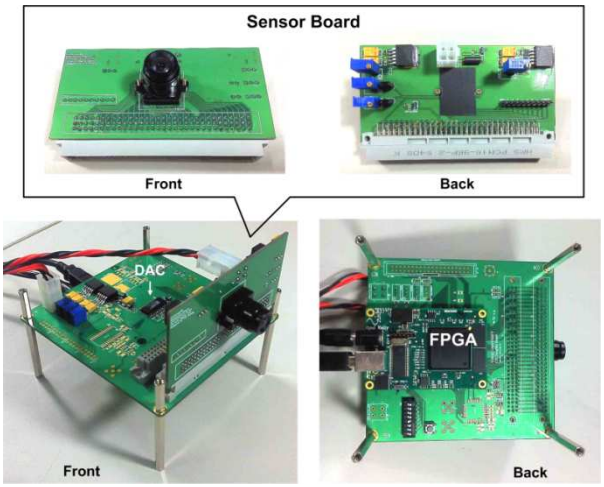

Fig. 14. Test board.

sensor, and transfers the outputs to the computer, simultaneously.

The test board consisting of a sensor-board and a main-board for measurement is shown in Fig. 14. The sensor-board is composed of variable resistors, regulators, and the image sensor chip with a lens. The FPGA and a DAC generating the ramp signal are included in the main-board. We use the external DAC to change the ramp signal freely and reduce the number of pad of the chip.

Fig. 15 and Table 1 compare the power consumption with the results of previous work using an up/down counter [4, 5]. The average power of the digital blocks is measured by SPICE simulation results during 1

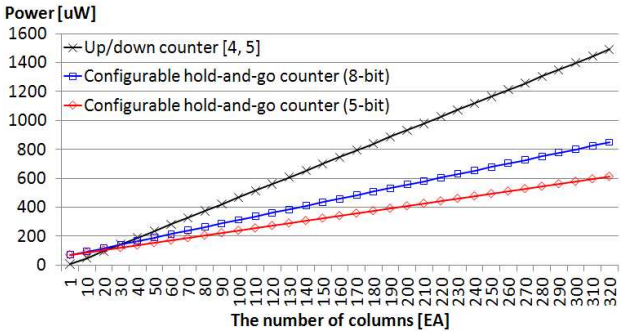

Fig. 15. Comparison of the power consumption in the digital CDS.

Table 1. Comparison of the power consumption in the digital CDS

※	Digital CDS					
	Up/down counter [4, 5] (Only 10-bit up/down counters)		**Configurable hold-and-go counter** (Configurable counters+10-bit SRAMs+one global 10-bit counter)			
			8-bit (8×)		**5-bit (1×)**	
1EA column	7.74μW	**+4.65μW /column**	71.01μW	**+2.44μW /column**	70.26μW	**+1.7μW /column**
2EA columns	12.39μW		73.45μW		71.96μW	
320EA columns	1491.09μW **(100%)**		849.37μW **(56.96%)**		612.56μW **(41.08%)**	

* Average power consumption excluding the reading-time

horizontal time period excluding the reading-time. The x-axis is the number of columns and the y-axis is the power consumption in Fig. 15. The up/down counter, the proposed 8-bit counter (analog gain=8×), and the proposed 5-bit counter (analog gain=1×) consume 4.65 μW per column, 2.44 μW per column, and 1.7 μW per column, respectively, where the resolution of the image sensor is 10-bit. When we use 320 columns for QVGA resolution with the 8-bit hold-and-go counter, the power consumption is reduced by 43% in comparison with the previous digital CDS circuits. In the case of the 5-bit counter, the power consumption is reduced by 59%. If the number of columns is increased further, the power consumption can be drastically reduced.

The measured column FPN is about 0.1 LSB at dark. To take the column FPN, we captured 30 images at dark and analysis the data by using the program with calculations of temporal average, spatial average, and deviation.

Fig. 16 shows the measured results of sample images. The left side is the measured result without CDS, and the right side is the measured result with the proposed dual

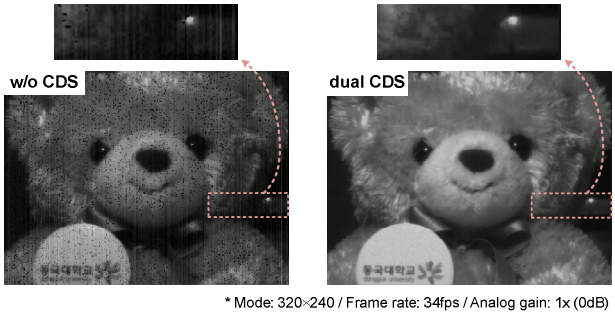

Fig. 16. Measured sample images.

Table 2. Specification of the designed CMOS image sensor

Process	0.13 μm 1P4M CMOS process
Chip size	5 mm × 5 mm
Effective chip size	1.5 mm × 2.2 mm
Resolution	320 × 240
Pixel type	2-shared 4T (pinned-photodiode)
Pixel size	2.25 μm × 2.25 μm
Supply voltage	2.8 V (analog), 1.5 V (digital)
Frame rate	80 frame/s
ADC resolution	10-bit
Column FPN	0.1 LSB (with dual CDS)
Power consumption (average-power of the digital block excluding the reading-time)	1.70 μW/column (analog gain=1×) 1.81 μW/column (analog gain=2×) 2.02 μW/column (analog gain=4×) 2.44 μW/column (analog gain=8×)

CDS. The upper image is the magnified photo for the measured image. The chip performance is summarized in Table 2.

V. CONCLUSIONS

This paper has presented a dual CDS with an 8-bit configurable hold-and-go counter for a 10-bit 320 × 240 pixel, 80 frame/s CMOS image sensor. As well as a new 8-bit hold-and-go counter in each column performed a role to obtain an equivalent 10-bit resolution, the dual CDS and a configurable counter scheme reduced the power consumption drastically. With those techniques, the digital counter consumed at least 43% and at most 61% less power compared with the column-counters type, and the frame rate was approximately 40% faster than the double memory type due to a partial pipeline structure without additional memories.

In summary, there are three main advantages of this dual CDS technique: (1) simple architecture, (2) high energy efficiency, and (3) applicability of the techniques. First, the proposed CMOS image sensor and conventional one are based on the column-parallel SS-ADC with almost the same architecture. Thus, we realize a low noise image sensor by minimally changing the design of a conventional image sensor. Secondly, the hold-and-go algorithm enables the frame rate to increase with relatively low power and small area, and the configurable counter scheme enhances energy efficiency more. Thirdly, it is possible that the techniques could be applied to other digital CDSs, even in high speed digital CDSs such as [2-7].

On the other hand, the major drawback of the proposed architecture is that it is still using a global counter. Although the proposed image sensor realizes a high frame rate with a relatively small area, the maximum speed is restricted by using the global counter. Therefore, it is the next step to study an effective method using these schemes without the global counter.

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