Millimeter-Wave High-Linear CMOS Low-Noise Amplifier Using Multiple-Gate Transistors

Jihoon Kim, Wooyeol Choi, Abdus Samad Quraishi, and Youngwoo Kwon

A millimeter-wave (mm-wave) high-linear low-noise amplifier (LNA) is presented using a 0.18 μm standard CMOS process. To improve the linearity of mm-wave LNAs, we adopted the multiple-gate transistor (MGTR) topology used in the low frequency range. By using an MGTR having a different gate-source bias at the last stage of LNAs, third-order input intercept point (IIP3) and 1-dB gain compression point (P_{1dB}) increase by 4.85 dBm and 4 dBm, respectively, without noise figure (NF) degradation. At 33 GHz, the proposed LNAs represent 9.5 dB gain, 7.13 dB NF, and 6.25 dBm IIP3.

Keywords: Millimeter-wave, low-noise amplifier, MGTR, linearity, 0.18 μm CMOS.

I. Introduction

In recent years, the development of CMOS RF circuit design including RF CMOS modeling, low-loss passive element structure, and layout optimization has resulted in millimeter-wave (mm-wave) ICs implemented by using 0.18 μm standard CMOS technology [1]. It has not only brought about various mm-wave applications using standard CMOS process but also accelerated the development of RF transceiver MMICs operating at beyond 20 GHz frequency using only low-cost 0.18 μm standard CMOS foundry [2], [3]. Thus, RF CMOS IC components operating in the frequency range above 20 GHz have also become necessary to meet the specifications of modern communication systems. The linearity is the essential requirement in recent receiver front-ends that require a large dynamic range. Until now, many studies about high linear receivers or low-noise amplifiers (LNAs) have been accomplished in the microwave range under 5 GHz [4], [5]. In continuation of these previous works, this work is an attempt to improve the linearity of LNAs available in the mm-wave range using a low-cost 0.18 μm standard CMOS process.

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II. Millimeter-Wave Designs for Higher Linearity

Figure 1 shows the circuit schematic of LNAs developed in this work. To improve the linearity, we adopted the multiple-gate transistor (MGTR) topology, which has been used in the microwave range. MGTR topology helps us in controlling the second derivative of transconductance, g_m'', and the second harmonic conductance, $g(2\omega)$, which are important factors to the third-order input intercept point (IIP3), by tuning its gate-source voltages apart from that of a common source stage [4]. For higher linearity, g_m'' should be near to zero and $g(2\omega)$ should be as large as possible [4]. As the operating frequency increases, the nonlinear C_{gs} plays important role in determining the second harmonic conductance as can be seen from

$$g(2\omega) \approx g_m \times \frac{1+2j\omega C_{gs}Z_1 + 2j\omega C_{gd}Z_2}{1+\omega_T C_{gd} Z_2}, \qquad \omega_T = \frac{g_m}{C_{gs}}, \tag{1}$$

where g_m is the transconductance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, Z_1 is the input impedance, and Z_2 is the output impedance. In addition to reducing g_m'' by supplying proper gate-source bias, MGTR increases $g(2\omega)$ by increasing C_{gs} without any DC power consumption and serious gain drop. Thus, it can contribute in improving the linearity at high frequency. Previously proposed

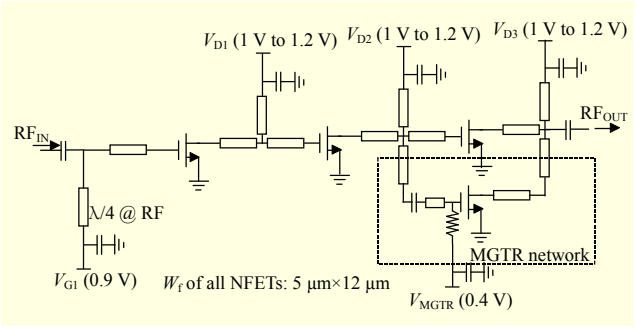

Fig. 1. Schematic of proposed mm-wave MGTR LNA.

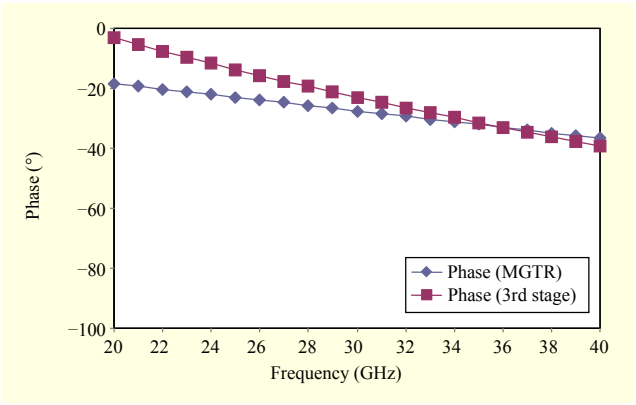

Fig. 2. Phase difference between two paths at third stage of LNA.

high-linear LNAs using this method were mainly designed as a single common source stage or a single cascode [4], [5]. However, as the operating frequency increases above 20 GHz, a single stage LNA cannot provide enough gain. Moreover, by inserting the MGTR, additional parasitic parameters can seriously degrade the noise figure (NF) in the mm-wave range. This LNA is designed to have three common source stages with the MGTR inserted at the last stage. By attaching the MGTR at the last stage, it has a minor effect on NF degradation. In addition, more improved linearity can be expected because according to theory, the last stage generally has a dominant influence on overall IIP3 [6]. Additional interconnect lines for inserting the MGTR are carefully designed because they can result in un-negligible phase difference between the MGTR network and the original third stage of LNA in the output matching network. Although transmission lines of equal lengths are basically tried in the two paths, the phase difference due to unequal transmission lines is about 11° at 30 GHz due to the inevitable connection of the MGTR network to the third stage of LNA. However, the small capacitance (≈0.2 pF) reduces the phase difference by 6.4° at 30 GHz. The small capacitance acts not only as a DC block but also as a phase compensator. Figure 2 represents the simulation result of the phase difference between the two paths in the third stage.

III. Measurements

The proposed circuit is fabricated using 0.18 μm standard CMOS technology with 1 poly and 6 metals. Figure 3 represents a photograph of the implemented circuit. To compensate the loss from resistive silicon substrates and thin metals, grounded coplanar waveguide using multiple metal lines and transistors of F_{MAX}-optimized size found in our previous paper are applied [1]. On-wafer measured *S*-parameter, IIP3, gain, third-order output intercept point (OIP3), and NF are shown in Figs. 4(a) and (b). Under an optimized

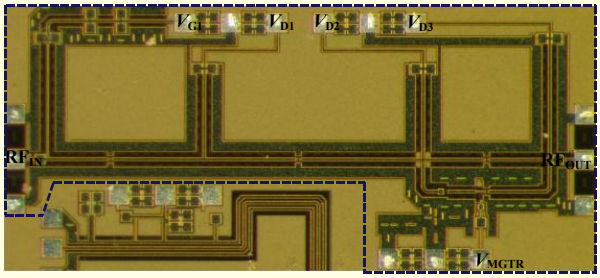

Fig. 3. Photograph of mm-wave MGTR LNA (1.92 mm × 0.85 mm).

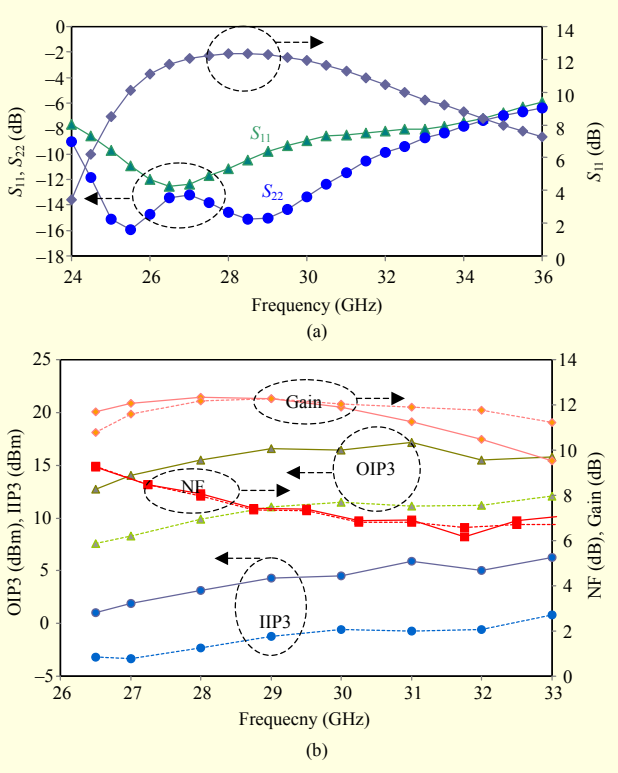

Fig. 4. (a) Measured *S*-parameter of the proposed LNA and (b) measured IIP3, gain, OIP3, and NF of the proposed LNA with MGTR (solid line) and LNA without MGTR (dashed line). V_{G1}=0.9 V, V_{D1}=V_{D2}=V_{D3}=1.2 V, V_{MGTR} = 0.4 V, total current = 44 mA.

MGTR bias where the gate-source voltage of the MGTR (V_{MGTR}) is 0.4 V, peak gain is 12.35 dB at 28 GHz, and 3-dB gain bandwidth is 7.5 GHz (25.5 GHz through 33 GHz). In Fig. 4(b), IIP3, gain, and OIP3 of the proposed LNA are compared with those of the LNAs without an MGTR. We compared the linearity between the LNA with an MGTR and the LNA without an MGTR under the same bias condition where V_{G1} is 0.9 V, $V_{D1\ to\ D3}$ is 1.2 V, and I_{ds} is 44 mA. Because MGTR topology uses the secondary transistor under or near threshold voltage V_{TH}, there is no additional current consumption. The LNA without an MGTR is completely equal to LNA with an MGTR except for the MGTR network. Within the 3-dB gain bandwidth, the measured IIP3, OIP3, and NF of the LNA with an MGTR are 1.0 dBm through 6.25 dBm, 12.7 dBm through 16.57 dBm, and 6.2 dB through 9.2 dB, respectively. From these results, we clarify that LNAs with an MGTR do not suffer from serious gain degradation when it is compared with LNAs without an MGTR. However, additional transmission lines, a capacitor, and a capacitive MGTR in the third stage of the LNA have an effect on gain degradation below 1.7 dB in the high-end frequency range of 31 GHz through 33 GHz. To test the effect of adopted MGTR topology on IIP3 and P_{1dB} in the mm-wave range, the MGTR bias is measured at 30 GHz as shown in Fig. 5. As proposed, when the MGTR bias is 0.4 V, the improved IIP3 and P_{1dB} can be obtained which are 2.5 dBm through 3.4 dBm and 1.0 dBm through 3.0 dBm higher than the other biases.

In comparison with the same LNAs without an MGTR network, the proposed LNA also shows an improvement of 4.85 dBm in IIP3 and 4 dBm in P_{1dB}. In addition, the effect on NF and gain characteristics according to the MGTR bias is investigated at 30 GHz as shown in Fig. 6. Although the MGTR bias is changed by 0 V through 0.6 V, gain variation is below 1.7 dB, and NF variation is only 0.09 dB. The proposed LNA with an MGTR network shows negligible gain and noise

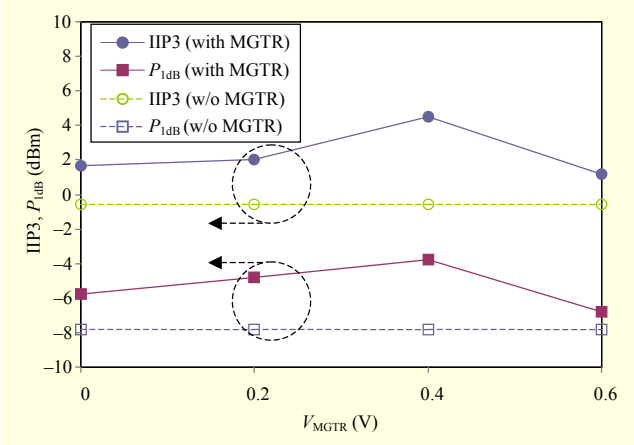

Fig. 5. Measured IIP3 and P_{1dB} versus V_{MGTR} at 30 GHz

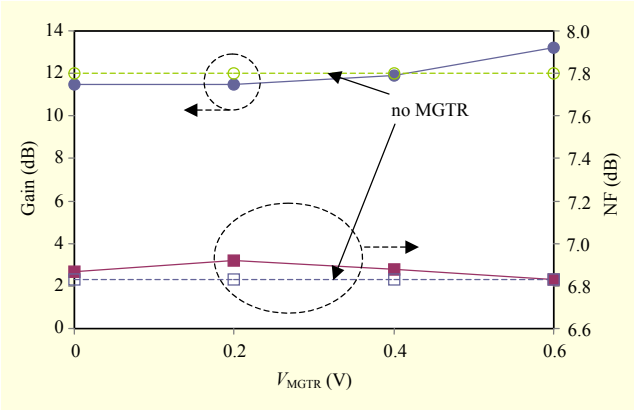

Fig. 6. Measured gain and NF versus V_{MGTR} at 30 GHz.

Table 1. Comparison of reported 20 GHz to 40 GHz LNAs using 0.18 μm CMOS technology.

	Freq. range (GHz)	NF (dB)	Gain (dB)	IIP3 (dB)	P_{1dB} (dBm)	P_{DC} (mW)
[2]	22 to 29	4.5 to 6	18	-	-	15
[7]	21 to 27	4.9 to 6.1	9	–4	-	27
[8]	21 to 27	5.6 to 9.1	12.86	2.04	–11.1	54
[9]	21 to 27	3.9 to 6.7	13.1	0.54	–12.2	54
[10]	38 to 42	7.5	15	–8	–16	36
This work (low P_{DC})	25.5 to 33	6.2 to 9.2	11.5	4.2	–5.8	31
This work (high P_{DC})	25.5 to 33	6.2 to 9.2	12.3	6.25	–3.8	53

degradation as compared to the LNA without an MGTR network. Although a related figure is not shown, a similar tendency is also observed in the lower DC power mode where IIP3 somewhat decreases. Through above measurements, we can extract that the proposed mm-wave LNA has better IIP3 performance without NF degradation. Table 1 compares the performance of the reported 20 GHz to 40 GHz LNAs using 0.18 μm CMOS technology. To show that the improved linearity is the direct result of MGTR topology regardless of P_{DC}, we compared the proposed LNA under both low P_{DC} and high P_{DC} condition with other reported LNAs. From Table 1, we can confirm that under not only high P_{DC} but also low P_{DC} conditions, MGTR LNAs show the best IIP3 and P_{1dB} performance. To the best of the authors' knowledge, this is the best linearity performance of CMOS LNAs operating at greater than 30 GHz.

IV. Conclusion

High-linear LNAs have been demonstrated over 30 GHz

using a low-cost standard 0.18 μm CMOS process. In order to improve the linearity without NF degradation in the mm-wave, an MGTR network is successfully inserted into the last stage of a 3-stage LNA. Particularly, in a high frequency range of more than 20 GHz, an MGTR can improve not only g_m'' that is critical for IIP3 in the low frequency range but also second harmonic termination that imposes more critical effects on IIP3 in the higher frequency range by changing gate bias. As a result, optimum MGTR gate bias accomplishes the best IIP3 performance among the reported LNAs over 20 GHz. This also inherits advantages of previous microwave MGTR LNAs that do not require additional DC power consumption to enhance IIP3 and almost keep the same gain as LNAs without MGTR.

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