

Low-Power, All Digital Phase-Locked Loop with a Wide-Range, High Resolution TDC

YoungGun Pu, AnSoo Park, Joon-Sung Park, and Kang-Yoon Lee

In this paper, we propose a low-power all-digital phase-locked loop (ADPLL) with a wide input range and a high resolution time-to-digital converter (TDC). The resolution of the proposed TDC is improved by using a phase-interpolator and the time amplifier. The phase noise of the proposed ADPLL is improved by using a fine resolution digitally controlled oscillator (DCO) with an active inductor. In order to control the frequency of the DCO, the transconductance of the active inductor is tuned digitally. The die area of the ADPLL is 0.8 mm² using 0.13 μm CMOS technology. The frequency resolution of the TDC is 1 ps. The DCO tuning range is 58% at 2.4 GHz and the effective DCO frequency resolution is 0.14 kHz. The phase noise of the ADPLL output at 2.4 GHz is -120.5 dBc/Hz with a 1 MHz offset. The total power consumption of the ADPLL is 12 mW from a 1.2 V supply voltage.

Keywords: All-digital phase-locked loop (ADPLL), time-to-digital converter (TDC), phase-interpolator, time amplifier, wide tuning range frequency, active inductor, fine-resolution, digitally controlled oscillator (DCO).

I. Introduction

In submicron technology, digital radio frequency (RF) architectures will have to be adopted in order to reduce the cost, the power consumption, and the required area of the system. As the minimum feature size decreases, the supply voltage will also decrease. While an analog phase-locked loop (PLL) needs to be redesigned as the process is changed, a digital PLL can be easily translated into a new process. A digital PLL can be integrated into a digital RF transceiver.

All-digital phase-locked loop (ADPLL) architectures for digital RF transceivers are becoming attractive in submicron technology. To improve the frequency resolution and tuning range performance of the ADPLL, the performance of the time-to-digital converter (TDC) and the digitally controlled oscillator (DCO) is most important. A conventional analog PLL uses a charge-pump circuit. However, an analog PLL gets worse in jitter performance because of the charge-pump feed-through and mismatches. Therefore, a digital PLL uses a TDC instead of a charge-pump. The use of the TDC eliminates the current sources and the RC filter found in analog PLLs. The TDC is used to compare the DCO output frequency to a reference frequency. It needs to have a high resolution in order to improve the phase noise of the digital PLL [1]. The resolution of the TDC is very important to the performance of the ADPLL because it has an effect in causing in-band phase noise [2]. Typically, a TDC is designed with an inverter delay chain. Therefore, the TDC has a problem in that it cannot be implemented at a high resolution due to a less than inverter delay time. In this case, the TDC is designed with a delay time that is less than that of the inverter by using a phase-interpolator [3]. However, it is sensitive to process variation. To compensate for this, the TDC resolution is improved by using a time

Manuscript received May 22, 2010; revised July 16, 2010; accepted Aug. 2, 2010.

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology(2010-0013369). Also, this work was sponsored by Samsung Electronics. Co., Ltd, Rep. of Korea.

YoungGun Pu (phone: +82 2 452 6229, email: hara1015@konkuk.ac.kr), AnSoo Park (email: anssown@konkuk.ac.kr), Joon-Sung Park (email: pjs83@konkuk.ac.kr), and Kang-Yoon Lee (corresponding author, email: kylee@konkuk.ac.kr) are with the Department of Electronic Engineering, Konkuk University, Seoul, Rep. of Korea.

doi:10.4218/etrij.11.0110.0295

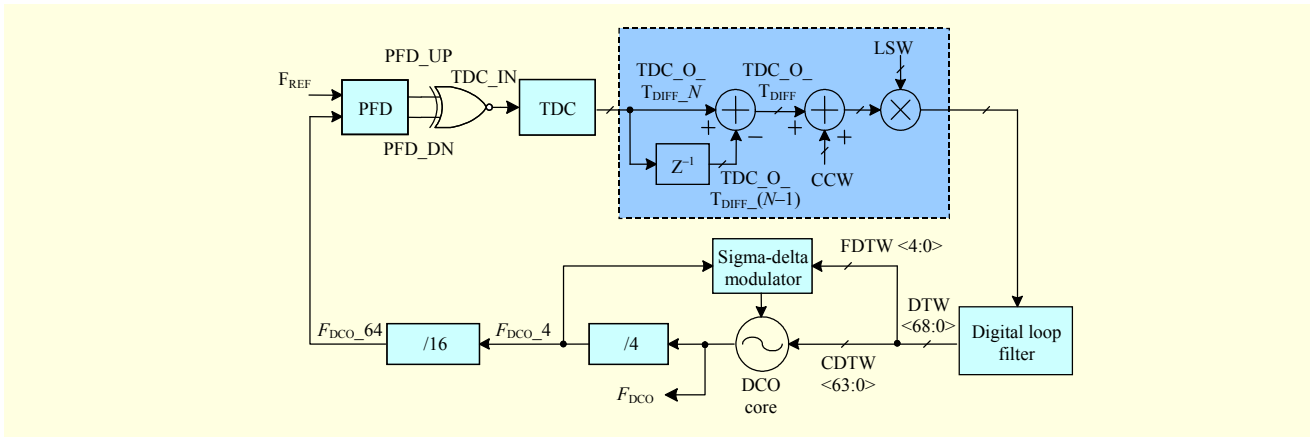


Fig. 1. Block diagram of proposed ADPLL.

amplifier (TA) that amplifies the inverter delay time [4]. However, the TA cannot be implemented with a high gain at a high frequency. In addition, in order to have a wide tuning range in the digital PLL, the input range of the TDC must have a wider input range. So, we have developed a three-step coarse-tuning TDC which resolves the problems of the frequency resolution and the input range.

In digital PLLs, the DCO corresponds to the voltage controlled oscillator (VCO) of the analog PLL. Typically, the frequency of the DCO is tuned with a varactor. There is, however, a physical limitation to the varactor size (\sim aF). To overcome this limitation, a sigma-delta modulator is used to provide the fine capacitance needed [5]. Nevertheless there is still a limitation in the frequency resolution, due to a physical limitation in the varactor size. In this case, the dithering bits of the sigma-delta modulator need to be increased in order to provide a fine resolution. Unfortunately, this requires an increase in the area and power consumption. In this paper, an active inductor is used for the frequency control, overcoming the minimum frequency resolution problem.

Conventionally, several techniques are used to cover the wide frequency range using a single LC-oscillator [6]. However, if the tuning range is too wide, the area and power consumption are increased. Thus, the DCO architecture and automatic coarse tuning scheme needs to be optimized for a wide tuning range. To improve the frequency resolution and tuning range performance of DCO, the active-inductor DCO with an automatic three-step coarse tuning loop is used [7].

This paper presents a fractional-ADPLL with a three-step TDC and an active-inductor DCO. The three-step TDC is used for a wide input range and a frequency resolution that is less than the inverter delay. An active-inductor DCO is used for a wide tuning range and fine resolution.

Section II shows the architecture and operation of the ADPLL with the proposed the three-step TDC and the active-

inductor DCO. Section III explains the proposed TDC, and section IV shows the measurement results of the proposed ADPLL. Section V concludes this work.

II. All-Digital PLL Architecture

Figure 1 shows the block diagram of the proposed ADPLL. It consists of a conventional phase and frequency detector (PFD), three-step TDC, digital loop filter, 3rd-order sigma delta modulator (3rd-order SDM), coarse tuning controller, 16-divider, and 4-divider. The PFD is used to compare the arrival times of the reference clock and the divided clock edges. The resulting PFD_UP/PFD_DN information is processed through an XOR [8]. The difference between the rising edge and the falling edge of the XOR output is measured by the three-step TDC. The output of the three-step TDC for the phase error between F_{REF} and F_{DCO_64} is $TDC_O_T_{DIFF}$. It is calculated by using the difference in the digital codes between $TDC_O_T_{DIFF_N}$, which is delayed ($N-1$)th output of the three-step TDC, and $TDC_O_T_{DIFF_N}$, which is the N -th output of the three-step TDC.

The channel control word (CCW) is added to $TDC_O_T_{DIFF}$ for the channel switching of ADPLL. And then, it is multiplied by the level scale word (LSW) to fit the input dynamic range the DCO.

The digital loop filter is a 1st-order digital filter and controls the DCO core with a 69 bit digital-tuning word (DTW) [9]. The DTW is divided into CDTW<63:0>, which is sent directly to the DCO core, and the FDTW<4:0>, which is sent to the 3rd-order SDM and are used to enhance the frequency resolution of the DCO. The DCO output is divided by the 4-divider and the 16-divider. The output of 4-divider is used as the sampling clock for the 3rd-order SDM.

Figure 2 shows the timing diagram of the proposed ADPLL. The PFD is used to compare the time interval T_{DIFF} between

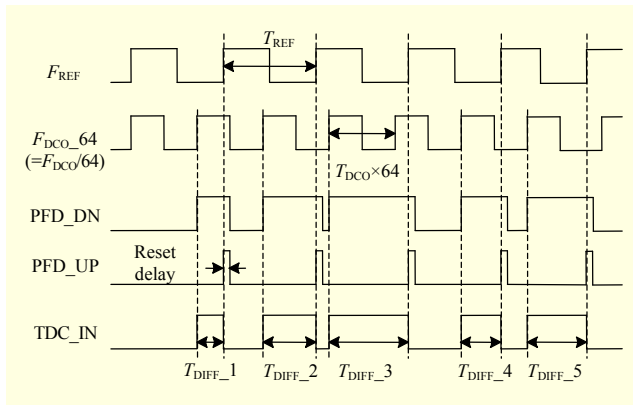


Fig. 2. Timing diagram of proposed ADPLL.

F_{REF} and F_{DCO_64} . The PFD always generates PFD_DN because F_{DCO_64} is much faster than F_{REF} in spite of the DCO tuning range variation. The outputs of the PFD always contain a reset delay. The reset delay can be removed by using an XOR gate, and TDC_IN is used to exactly detect the time interval between F_{REF} and F_{DCO_64} .

In Fig. 2, we assume that the first period pulse width, the second period pulse width and the third period pulse width in TDC_IN are T_{DIFF_1} , T_{DIFF_2} , and T_{DIFF_3} , respectively, when the rising edge of the F_{REF} and F_{DCO_64} signals are equal.

The T_{DIFF} , time interval between F_{REF} and F_{DCO_64} , is calculated by

$$T_{DIFF} = \frac{1}{F_{REF}} - \frac{1}{F_{DCO_64}} = T_{DIFF_1} = (T_{DIFF_3}) - (T_{DIFF_2}), \quad (1)$$

where T_{DIFF} and T_{DIFF_1} are the same when the rising edge of the F_{REF} and F_{DCO_64} signals are equal. In other cases, T_{DIFF} is calculated by using time difference between T_{DIFF_2} and T_{DIFF_3} . Thus, to calculate the T_{DIFF} , which is the time interval between F_{REF} and F_{DCO_64} , the difference of the digital bits between the TDC output for T_{DIFF_3} and the delayed TDC output for T_{DIFF_2} is used.

The proposed ADPLL consists of the three-step TDC detecting period difference between F_{REF} and the divided F_{DCO} . Thus, the proposed three-step TDC can cover the output frequency range of the ADPLL by the DCO tuning-range.

If the tuning range of the proposed DCO is from 2.1 GHz to 3.5 GHz, T_{DIFF_TUNE} , which is the period difference between F_{REF} and the divided F_{DCO} , is from 7.99 ns to 20.18 ns as determined by (1). The proposed three-step TDC has an input range of 25 ns to compensate for the PVT variation.

The time difference of the divided F_{DCO} done by the channel switching of the ADPLL be determined by

$$T_{DIFF_CH} = \frac{1}{F_{DCO_64}} - \frac{1}{F_{DCO_64} + (F_{CH_min}/64)}, \quad (2)$$

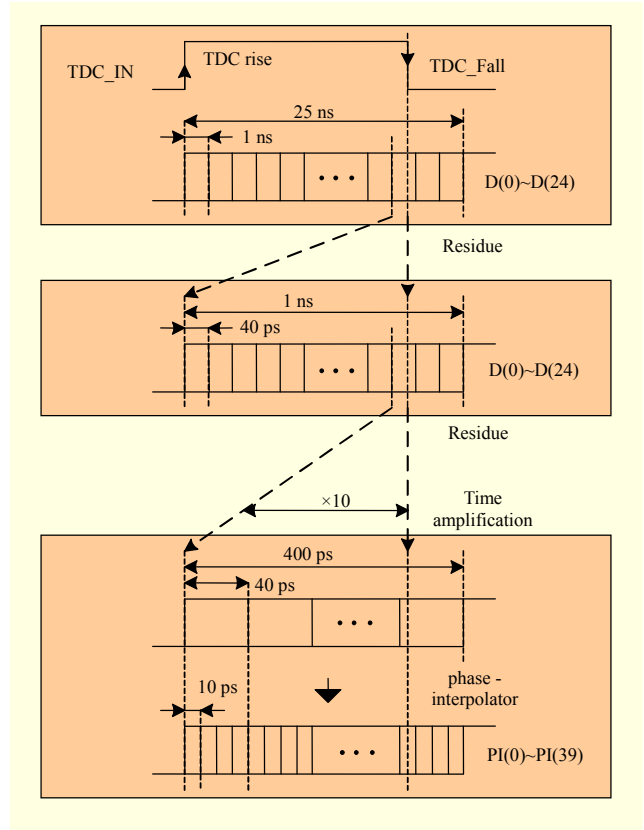


Fig. 3. Conceptual diagram of the proposed three-step TDC.

where F_{CH_min} is the minimum channel spacing. For example, in the Long Term Evolution (LTE) application, F_{CH_min} is 1.4 MHz [10] and T_{DIFF_CH} is 15.5 ps. Thus, resolution of the TDC must be less than 15.5 ps for channel switching of the ADPLL. The resolution of the proposed three-step TDC is 1 ps, considering the channel switching and the phase noise of the proposed ADPLL.

III. Three-Step TDC with a Phase-Interpolator and Time Amplifier

A buffer delay chain is widely used in TDC design. In the delay chain, the rising edge of the F_{DCO} signal propagates through the chain of inverters. When the rising edge of the F_{REF} signal arrives, a flip-flop (F/F) samples the output of each inverter and produces a thermometer code that locates the relative time interval. However, this sampling scheme cannot resolve the time interval better than a single inverter delay [11].

The conceptual diagram of the proposed three-step TDC architecture is shown in Fig. 3. It is composed of the 1st coarse TDC, the 2nd coarse TDC, and the fine TDC with a phase-interpolator and a TA. The time difference between the edge of each output of delay line $D(n)$, and the edge of TDC_Fall,

generates every possible time residue. The edge detector in the 1st coarse TDC and the 2nd coarse TDC determines which edge of $D(n)$ is closest to the TDC_Fall. The multiplexer (MUX) then passes that residue to the fine TDC through the TA. The three-step TDC improves the resolution by amplifying the residue between the input and closest coarse level, then quantizing the amplified residue again with the same coarse resolution. Both the 1st coarse TDC, the 2nd coarse TDC, and the fine TDC use thermometer-to-binary (T2B), resolving 5, 5, and 6 bits, respectively.

The ΔT_{RES} , which is the time resolution of the proposed three-step TDC, is 1 ps. The quantization noise due to the finite resolution of the TDC, ΔT_{RES} , affects the in-band phase noise of the ADPLL of Fig. 1. Therefore, the in-band phase-noise L at the output of the ADPLL due to the TDC timing quantization can be calculated as

$$L = 10 \log \left[\frac{(2\pi)^2}{12} \left(\frac{\Delta T_{RES}}{T_V} \right)^2 \cdot \frac{1}{F_{REF}} \right], \quad (3)$$

where T_V is the DCO clock period and F_{REF} is the reference of the sampling frequency [2]. Substituting $\Delta T_{RES} = 1$ ps, $F_{REF} = 26$ MHz, $F_{DCO} = 2.4$ GHz, and $T_V = 417$ ps, we obtain $L = -121.37$ dBc/Hz. Equation (3) was validated experimentally within 1 dB of measurement error for ΔT_{RES} spanning 0.89 to 1.12 ps through varying the TDC supply voltage. The next generations of deep-submicron CMOS processes can only bring reductions in ΔT_{RES} , so the phase noise performance will be further improved.

Figure 4 shows the block diagram of the proposed three-step TDC. The 1st coarse TDC in Fig. 4(a) is composed of a delay cell that consists of two cascaded inverters, a phase-interpolator with a resistor automatic-tuning circuit, a F/F, an edge detector, and a multiplexer (MUX). The 2nd coarse TDC is similar to the 1st coarse TDC in Fig. 4(b). The fine TDC in Fig. 4(c) is composed of a delay cell that consists of two cascaded inverters, a phase-interpolator with a resistor automatic-tuning circuit, and a F/F. The F/F is used as a comparator whose output determines the thermometer codes of the TDC. By locating the transition from 1 to 0, the edge detector logic identifies the critical residue to be sent to the TA and the fine TDC for fine conversion.

Figure 5 shows the block diagram of the proposed resistor automatic-tuning and phase-interpolator that is composed of resistor tuning arrays (RTA) using passive resistors. The passive resistors usually vary by about 15% due to process variations. The variation of passive resistors in the phase-interpolator can be compensated by adjusting component values for regular time intervals. The $RTA(i)$ in the phase-interpolator is controlled by the resistor automatic-tuning circuit to achieve regular time intervals. Assume there are two

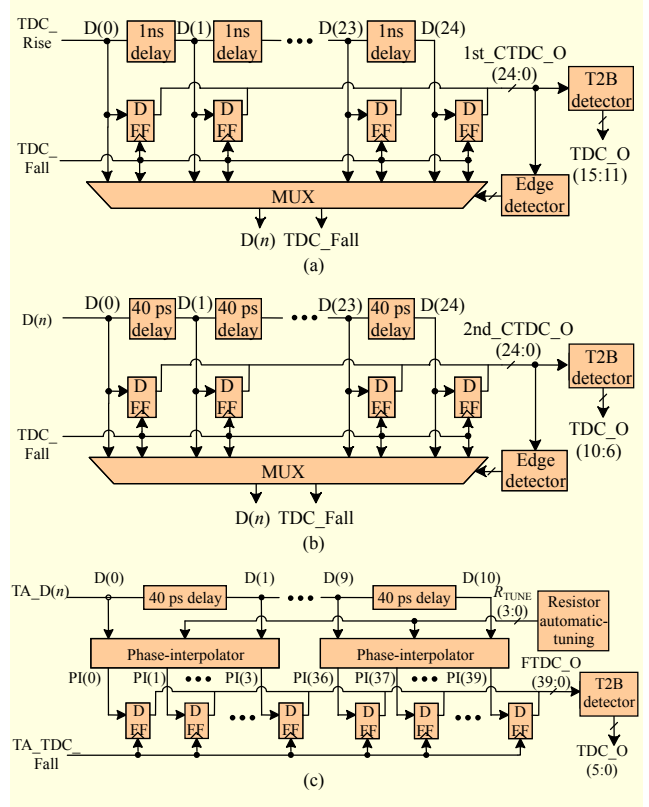


Fig. 4. Block diagram of proposed three-step TDC: (a) 1st coarse TDC, (b) 2nd coarse TDC, and (c) fine TDC.

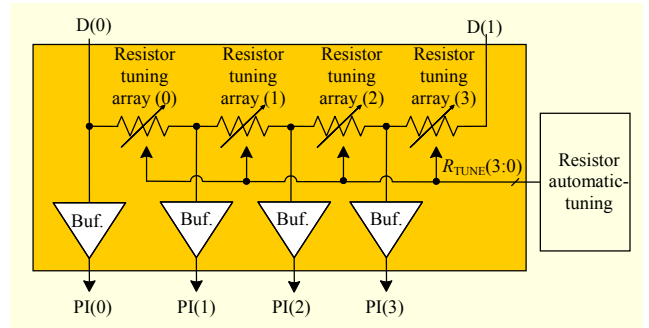


Fig. 5. Block diagram of proposed resistor automatic-tuning and phase-interpolator.

rising signal transitions with two inverter delay T_{DS} . A new signal $PI(i)$, defined by

$$PI(i) = D(0) + a_i \cdot \{D(0) - D(1)\}, \quad 0 < a_i < 1, \quad (4)$$

is found between the two generating signals $D(0)$ and $D(1)$ in the transition region [3]. Together with a comparator latch that detects the mid-level crossing, the new signal can be used to quantize the time interval between $D(0)$ and $D(1)$. A passive voltage divider, as shown in Fig. 5, is connected between $D(0)$ and $D(1)$ and is used to generate the interpolated signals defined by (4).

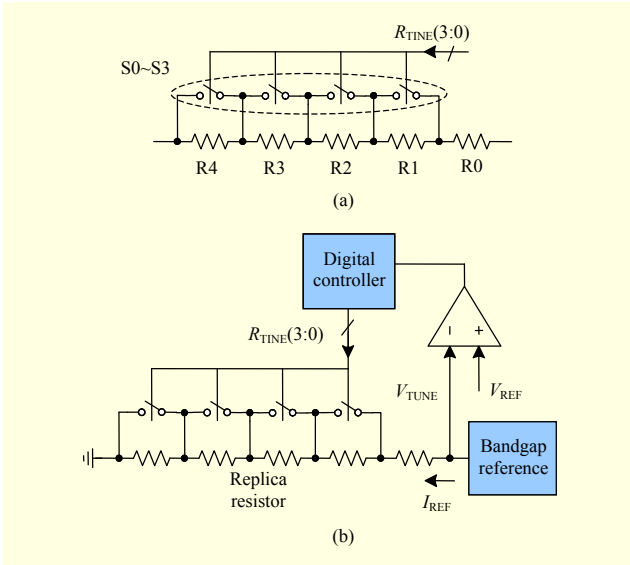


Fig. 6. Schematic of proposed (a) RTA and (b) resistor automatic-tuning circuit of phase-interpolator.

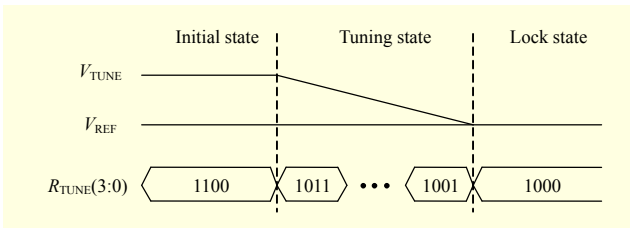


Fig. 7. Timing diagram of proposed resistor automatic-tuning method.

Figure 6(a) shows the RTA which is composed of a main resistor (R0) and subresistors (R1 through R4). It is controlled by the $R_{TUNE}(3:0)$ signal from the resistor automatic-tuning circuit shown in Fig. 6(b). In Fig. 6(b), V_{TUNE} is generated by I_{REF} and the replica resistor of R0 through R4. It is then compared with the reference voltage, V_{REF} . $R_{TUNE}(3:0)$ is then controlled based on the result from the digital controller. When the resistor is changed due to process variation, it is restored by the negative feedback of the resistor automatic-tuning circuit.

Figure 7 shows the timing diagram of the proposed resistor automatic-tuning method. If the resistor of the phase-interpolator is increased by process variation, the V_{TUNE} is higher than the V_{REF} . In this case, the switch control bits $R_{TUNE}(3:0)$ are decreased. The resistor tuning is completed when the V_{TUNE} crosses the V_{REF} .

Figure 8 shows the schematic of the proposed time amplifier. It is composed of a latch with a large output capacitance and delay cells with separate delay times (T_{off} , $T_{off} + \alpha$). The TA will amplify the time interval between the rising edge of $PI(n)$ and TDC_Fall . The small-signal gain of the TA is expressed by

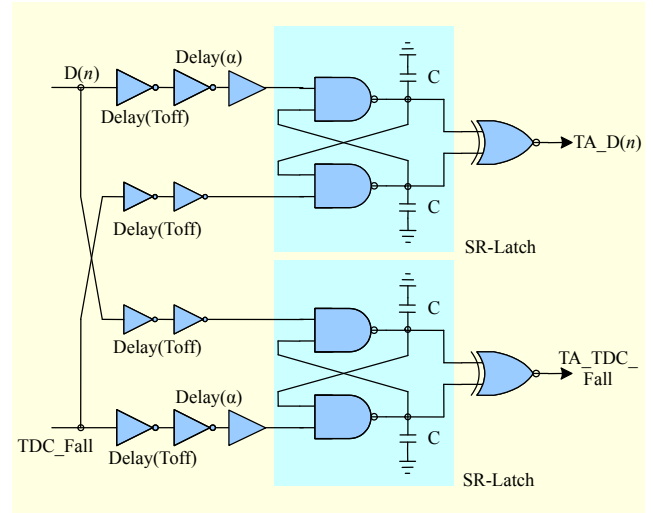


Fig. 8. Schematic of proposed time amplifier.

$$\text{Small-Signal Gain of the TA} = \frac{2C}{g_m \times \alpha}, \quad (5)$$

where g_m is the transconductance of the NAND and C is the capacitance at its output [4]. It should be noted that both the gain and linear range can be controlled by the time offset α . The TA uses a low value of C and α to let it cover the high gain and high frequency. The conventional TA is designed with two latches and delays with opposite inputs. Therefore, it has a problem in that it cannot implement a high gain due to having a delay time larger than the inverter delay time. The proposed TA is improved by using a fractional delay time α that is less than that of the inverter; this is the difference between two delay cells with separate delay times (T_{off} , $T_{off} + \alpha$).

IV. Experimental Results

The chip was fabricated using the 0.13 μm technology CMOS process with a single poly layer, six layers of metal, MIM capacitors, and high sheet resistance poly resistors. The total area of the ADPLL with TDC, DCO, SDM, and digital blocks is 0.8 mm^2 .

Figure 9 shows the measured results of the time amplifier. The relationship between the regeneration time and the initial time difference is a linear function. The gain and linear range of the TA are 10 and 100 ps, respectively.

Figure 10 shows the measured characteristic of the three-step TDC. The decimal number output of the three-step TDC when the time interval swept over TDC_IN is presented. The resolution and input range of the proposed three-step TDC are 1 ps and 25 ns, respectively.

To measure the linearity, two inputs with a 1 Hz difference at the reference frequency of 26 MHz are applied to generate a

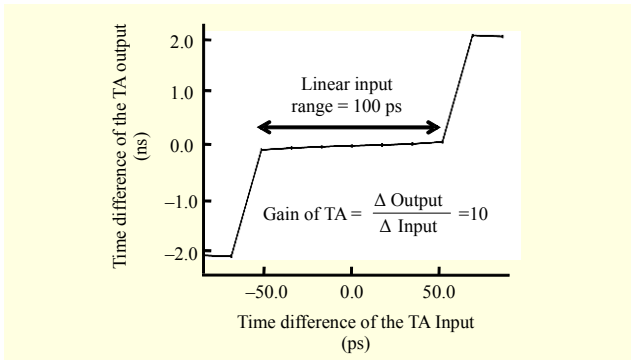


Fig. 9. Measurement results of time amplifier difference characteristic.

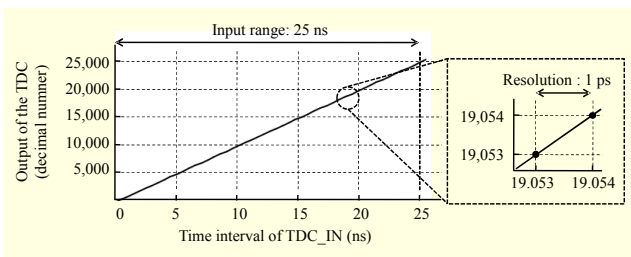


Fig. 10. Measured characteristics of the three-step TDC.

ramp input. The differential non-linearity (DNL) and the integral non-linearity (INL) of the three-step TDC are calculated, sweeping the value of the difference in the frequency, and then performing a code density statistic. The maximum DNL is ± 0.6 LSB, while the maximum INL is ± 1.9 LSB.

The frequency tuning range that can be achieved with the planar passive inductor and capacitance tuning is 0.9 GHz. On the other hand, when the three-step coarse tuning scheme is used, the tuning range can be widened by 0.5 GHz with the same capacitance value.

As a result, the overall frequency tuning range that can be covered with the 1st coarse tuning is 1.4 GHz.

The measured DCO gain is 0.14 kHz/LSB by the gain tuning scheme used for each frequency curve. The frequency resolution for the 1-LSB of the CDTW<63:0> is 4.6 kHz. Thus, the effective time-averaged frequency resolution $\Delta f^{\Delta\Sigma}$ done by the 5-bit SDM can be calculated as

$$\Delta f^{\Delta\Sigma} = 4.6 \text{ kHz} / 2^5 = 0.14 \text{ kHz}. \quad (6)$$

From (6), the K_{DCO} is about 0.14 kHz/LSB because the frequency resolution for the 1-LSB of the DTW<68:0> is 0.14 kHz.

The measured phase noise of the DCO output is -120.5 dBc/Hz at 1 MHz offset. The in-band phase noise is dominated by the resolution of TDC and the out-band phase noise depends on the Q factor and resolution of the DCO. Thus, in

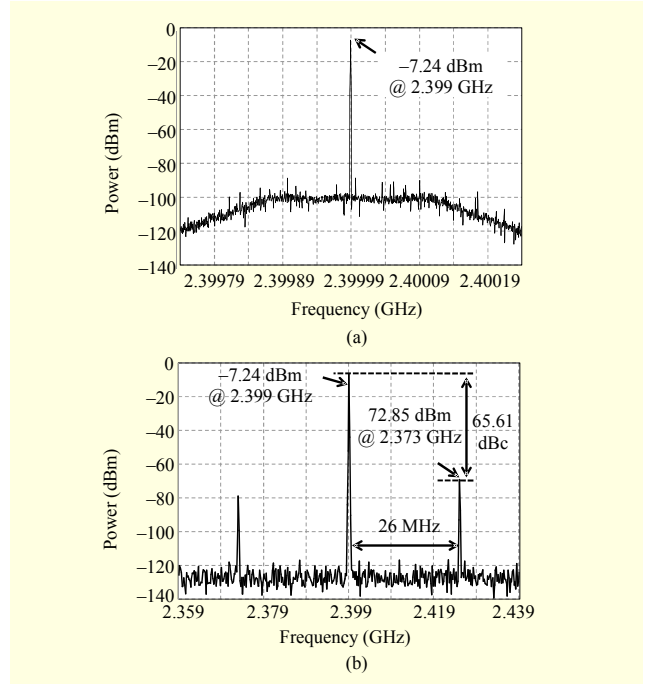


Fig. 11. Measured (a) narrow-span and (b) wide-span spectrum of ADPLL.

order to improve the out-band phase noise, the Q factor of the active inductor used in the DCO can be increased by adjusting the ratio of the passive inductor to active inductor.

For example, when the inductance of the active inductor is increased and the inductance of passive inductor is decreased in the DCO, the out-band phase noise performance would be improved at the sacrifice of the tuning range [7].

The power level of the spurious tone at 26 MHz offset is 65.61 dB lower than that of the carrier signal at 2.4 GHz, as shown in Fig. 11.

The performance of the proposed ADPLL is summarized in Table 1. The figure of merit with the frequency tuning range (FOM_T) for the ADPLL can be calculated using

$$FOM_T = PN(f_{\text{offset}}) - 20 \log \left(\frac{f_o}{f_{\text{offset}}} \right) + 10 \log \left(\frac{P_{\text{DC}}}{1 \text{ mW}} \right) - 20 \log \left(\frac{FDR}{10} \right), \quad (7)$$

where f_{offset} is the offset frequency, f_o is the oscillation frequency, $PN(f_{\text{offset}})$ is the phase noise found in the f_{offset} , P_{DC} is the DC power consumption of the ADPLL, and the FDR is the frequency tuning range in a percentage.

Table 1 shows the comparison of the proposed ADPLL with other recently published ones. The phase noise performance of this work is better than those of [1], [12], [13]. In addition, the resolution of the TDC is the smallest except [13], and the frequency resolution of the DCO is the smallest of all. Also, the proposed ADPLL has the smallest area and power consumption

Table 1. Summary of measured performance.

Reference	[1]	[12]	[13]	Proposed work	
Technology	90 nm CMOS	0.13 μ m CMOS	90 nm CMOS	0.13 μ m CMOS	
Output frequency	2.4 GHz	3.67 GHz	1.2 GHz	2.4 GHz	
Phase noise (@ offset frequency)	-110 dBc/Hz (500 kHz)	-108 dBc/Hz (400 kHz)	-97 dBc/Hz (1 MHz)	-120.5 dBc/Hz (1 MHz)	
TDC resolution	25 ps	6 ps	0.7 ps	1 ps	
DCO resolution (without SDM)	23 kHz	7.32 kHz	250 kHz	4.6 kHz	
Frequency range	17 %	27 %	83 %	58 %	
Total power consumption	25 mW	46.7 mW	17 mW	DCO	6.6 mW
				TDC	3.5 mW
				Others	1.9 mW
				Total	12 mW
Total area	N/A	0.95 mm ²	0.6 mm ²	0.8 mm ²	
FOM _T	-174.25 dBc/Hz	-179.19 dBc/Hz	-164.66 dBc/Hz	-192.58 dBc/Hz	

in the same process. From the measured phase noise and frequency tuning range, FOM_T is calculated as -192.58 dBc/Hz.

V. Conclusion

We have presented a novel architecture for a low-power ADPLL. It employs a three-step TDC and an active inductor DCO to achieve the low power ADPLL. The resolution of the proposed TDC is improved by using a phase-interpolator and a time amplifier for the improvement of the in-band phase noise of the ADPLL. To control the frequency of the DCO, the transconductance of the active inductor is tuned digitally. To cover the wide tuning range, a three-step coarse tuning scheme is used. The presented techniques and principles are extendible to other standards and modulation schemes.

The input range of the TDC is 25 ns, and the frequency resolution of the TDC is 1 ps. The DCO tuning range is 58% at 2.4 GHz, and the effective DCO frequency resolution is 0.14 kHz. The phase noise of the DCO output at 2.4 GHz is -120.5 dBc/Hz at a 1 MHz offset. The total power consumption of the ADPLL is 12 mW from a 1.2 V supply voltage. The die area of the ADPLL is 0.8 mm² using 0.13 μ m CMOS technology.

References

- [1] R.B. Staszewski et al., "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, Dec. 2005, pp. 2278-2291.
- [2] R.B. Staszewski, "TDC-Based Frequency Synthesizer for Wireless Applications," *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2004, pp. 215-218.
- [3] S. Henzler et al., "A Local Passive Time Interpolation Concept for Variation-Tolerant High-Resolution Time-to-Digital Conversion," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, July 2008, pp. 1666-1676.
- [4] Minjae Lee and A.A. Abidi, "A 9 b, 1.25 ps Resolution Coarse-Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies a Time Residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, Apr. 2008, pp. 769-777.
- [5] R.B. Staszewski et al., "Digitally Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in a Deep-Submicrometer CMOS Process," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 11, Nov. 2003, pp. 815-828.
- [6] D. Leenaerts et al., "A SiGe BiCMOS 1 ns Fast Hopping Frequency Synthesizer for UWB Radio," *Proc. IEEE Int. Solid-State Circuits Conf. Dig.*, vol. 1, Feb. 2005, pp. 202-593.
- [7] YoungGun Pu et al., "Wide-Band Fine-Resolution DCO with an Active Inductor and Three-Step Coarse Tuning Loop," *ETRI J.*, vol. 33, no. 2, Apr. 2011, pp. 201-209.
- [8] V. Kratyuk et al., "A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy," *IEEE Trans. Circ. Syst. II*, vol. 54, no. 3, Mar. 2007, pp. 247-251.
- [9] S.K. Mitra, *Digital Signal Processing: A Computer-Based Approach*, New York: McGraw-Hill, 2001.
- [10] Third Generation Partnership Project, "Technical Specification Group Radio Access Network," User Equipment Radio Transmission and Reception (Rel. 8), 3GPP TS 36.101 V8.5.1.
- [11] P. Dudek, S. Szczepanski, and J.V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, Feb. 2000, pp. 240-247.
- [12] C.-M. Hsu, M.Z. Straayer, and M.H. Perrott, "A Low-Noise, Wide-BW 3.6-GHz Digital $\Delta\Sigma$ Fractional-N Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, Dec. 2008, pp. 2776-2786.
- [13] V. Kratyuk et al., "A Digital PLL with a Stochastic Time-to-Digital Converter," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 8, Aug. 2009, pp. 1612-1621.



YoungGun Pu received his BS and MS from the Department of Electronic Engineering at Konkuk University, Seoul, Korea, in 2006 and 2008, respectively, where he is currently working toward a PhD in electronic engineering. His research interest is focused on CMOS fully integrated frequency synthesizers and oscillators

and on transceivers for low-power mobile communication.



AnSoo Park received the BS from the Department of Electronic Engineering at Konkuk University, Seoul, Korea, in 2009, where he is currently working toward his MS in electronic engineering. His research interests are in CMOS RF design, high-speed analog integrated circuit design, frequency synthesizers,

and other techniques of analog signal processing.



Joon-Sung Park received his BS from the Department of Electronic Engineering at Konkuk University, Seoul, Korea, in 2008, where he is currently working toward his MS in electronic engineering. His research interest is focused on CMOS RF/analog integrated circuit design for wireless application.



Kang-Yoon Lee received his BS, MS, and PhD from the School of Electrical Engineering at Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively. From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, where he was a manager of the Analog Division and worked on the design of

the CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. Since 2005, he has been with the Department of Electronics Engineering, Konkuk University, Seoul, where he is currently an assistant professor. His research interests include implementation of the CMOS RF transceiver, analog integrated circuits, and the analog/digital mixed-mode VLSI system design.