Wideband Low-Reflection Transmission Lines for Bare Chip on Multilayer PCB

Rashad Ramzan, Jonas Fritzin, Jerzy Dabrowski, and Christer Svensson

The pad pitch of modern radio frequency integrated circuits is in the order of few tens of micrometers. Connecting a large number of high-speed I/Os to the outside world with good signal fidelity at low cost is an extremely challenging task. To cope with this requirement, we need reflection-free transmission lines from an on-chip pad to on-board SMA connectors. Such a transmission line is very hard to design due to the difference in on-chip and on-board feature size and the requirement for extremely large bandwidth. In this paper, we propose the use of narrow tracks close to chip and wide tracks away from the chip. This narrow-to-wide transition in width results in impedance discontinuity. A step change in substrate thickness is utilized to cancel the effect of the width discontinuity, thus achieving a reflection-free microstrip. To verify the concept, several microstrips were designed on multilayer FR4 PCB without any additional manufacturing steps. The TDR measurements reveal that the impedance variation is less than 3 Ω for a 50 Ω microstrip and *S*11 better than –9 dB for the frequency range 1 GHz to 6 GHz when the width changes from 165 μm to 940 μm, and substrate thickness changes from 100 μm to 500 μm.

Keywords: Bare chip mounting, RF testing, microstrip discontinuities, microstrip transitions.

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I. Introduction

Connecting high-frequency signals from a printed circuit board (PCB) to an integrated circuit often requires careful analysis and design of the chip package and a circuit board close to the package. Still, it may be very difficult to keep good signal transmission over a wide frequency range. One way to simplify the task is to utilize bare chip mounting, thus avoiding the analysis and design of a package. However, because of the very small geometry of modern integrated circuits as compared to the width of standard 50 Ω PCB track, it is not simple to layout a wideband track from an SMA connector down to the chip. This becomes even more challenging, especially when many high-speed I/Os and radio frequency (RF) pads are present on a chip.

Quite often specialized technologies like ceramic boards are used for high-frequency systems using bare chips. The obvious benefit is the possibility to choose thin dielectrics with high-dielectric constant and low-dielectric loss. Still, it is highly desirable to use the widely available, and therefore low cost, standard PCB technology based on FR4 laminates. FR4 is in fact quite sufficient for signal transmission up to at least 10 GHz [1].

The main difficulty stems from the fact that due to lower dielectric constant, the 50 Ω transmission line (TL) on a standard 1.6 mm FR4 PCB is an order of magnitude wider compared to the pitch of the chip bonding pads. For example, the ΣΔ RF front-end chip shown in Fig. 1 has twelve high-speed (2.4 Gbps) I/Os. The RF front-end chip manufactured in 90 nm CMOS has the dimensions of 1 mm×1 mm and a pad pitch of 65 μm. For standard 1.6 mm thick FR4 ($\varepsilon_r = 4.2$) board with 1/2-oz copper, the 50 Ω microstrip requires a conductor width of approximately 3 mm, which reduces to

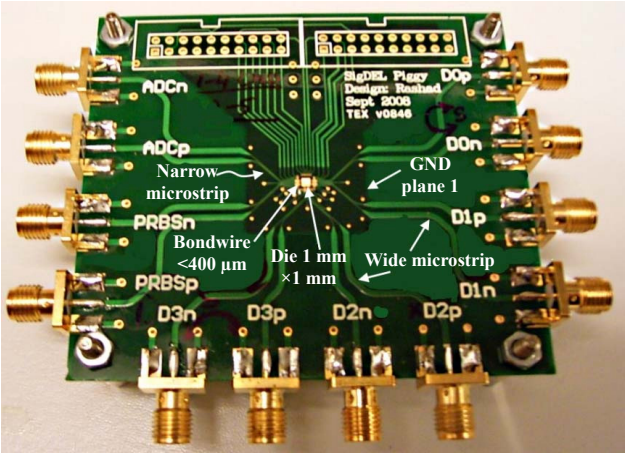

Fig. 1. 1 mm×1 mm ΣΔ RF front-end chip mounted in cavity with twelve 2.4 Gbps I/Os connected using 50 Ω reflection-free microstrips with bondwires shorter than 400 µm.

1.5 mm for a dielectric thickness of 0.8 mm [2]. The use of wide microstrips inhibits a dense layout close to the bare chip, which results in excessively long bondwires, thus severely limiting the bandwidth of the PCB track. On the other hand, the use of narrow track (with thin dielectric) from the chip all the way down to the SMA launch is not viable due to excessive attenuation and the fact that track width must be large (or equal) compared to the diameter of SMA connector pin for continuous 50 Ω impedance.

In this paper, we propose the use of a very thin dielectric in an area close to the chip, thus allowing narrow TLs which result in dense layout. Away from the chip, we have to use ordinary (wide) PCB TLs to reduce the track losses and allow the SMA connector pin soldering without large impedance discontinuities [3], [8]. A key issue is to design a reflection-free transition between the two TLs of different widths. To eliminate the effect of width discontinuity, we propose the use of two different substrate thicknesses: a narrow TL section with a thin substrate and wide TL section with a thick substrate underneath. This can be easily achieved using standard multilayer FR4 manufacturing process without any additional manufacturing steps. The difference in the substrate thickness is proportional to the difference of the width of TL. In this way, the width and substrate thickness discontinuities act in opposite direction canceling each other. Ideally, this results in a microstrip without any impedance discontinuity.

The paper is arranged as follows. In section II, the basic principle of reflection-free transmission of signal between two tracks of different width is elaborated. In section III, we present the design of different types of microstrips used in measurements to evaluate the combined effect of width and substrate thickness discontinuities. Details of simulation and measurement results are described in section IV. Section V concludes the paper with a short summary and some possible applications.

II. Basic Principle of Reflection-Free Transmission

The step change in the width of microstrip results in impedance discontinuity and is commonly used in microwave filter design. This type of discontinuity is thoroughly analyzed in literature [2]-[4]. As shown in Fig. 2(a), the wide side of microstrip (port 1) has 50 Ω impedance, while the narrow side (port 2) has impedance larger than 50 Ω. Since the substrate thickness is uniform, the impedance mismatch is directly proportional to the ratio of $W1$ and $W2$.

Another type of impedance discontinuity is encountered in microstrips when there is step change in substrate thickness as shown in Fig. 2(b). The microstrip with thick substrate (port 1) has 50 Ω impedance while the thin side (port 2) has impedance smaller than 50 Ω. Since the microstrip width is uniform, the impedance mismatch is directly proportional to the ratio of $H1$ and $H2$ [5], [6].

The difference between two discontinuities is the step change when the width transforms the 50 Ω impedance into higher

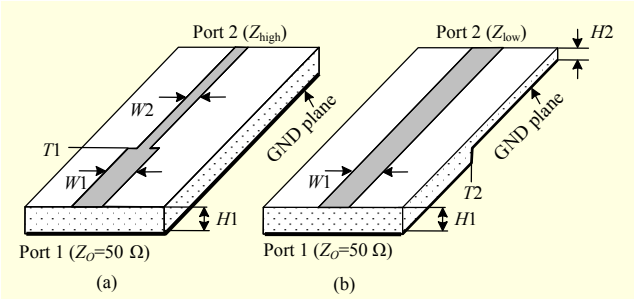

Fig. 2. (a) Microstrip step change in width and (b) microstrip step change in substrate thickness.

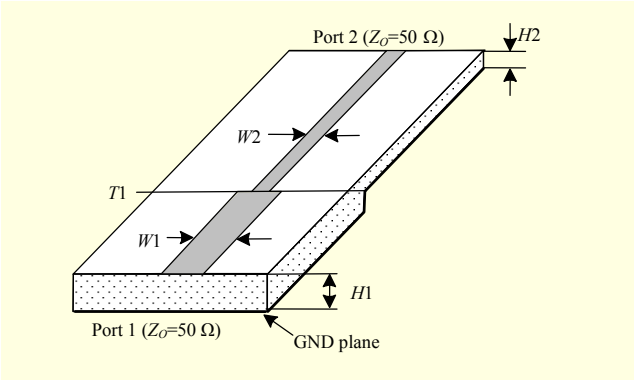

Fig. 3. Microstrip step change in width and step change in substrate thickness at same physical location cancelling the effect of each other.

value, while the step in substrate thickness transforms 50 Ω impedance into lower impedance. When these two discontinuities are designed to occur at same physical point in the microstrip, their effects cancel each other. Therefore, theoretically reflection-free transmission is possible despite the difference in the width as shown in Fig. 3. This is also obvious from the first-order approximate formula of microstrip impedance in (1) that keeping the *W/H* ratio fixed keeps the impedances Z_O constant [2]. In this case, W is the width of the microstrip and H is the height of the microstrip from GND plane or thickness of the substrate; in other words, while ε_e is the dielectric constant of the substrate.

$$Z_O = \frac{120\pi}{\varepsilon_e \left[W/H + 1.393 + 0.667 \ln(W/H + 1.444) \right]}. \quad (1)$$

III. Design of Microstrips

Momentum, a planar (2.5D) electromagnetic simulation tool from ADS, is used for the design, optimization, and simulation of microstrip lines.

The step change in substrate thickness can be conveniently realized using standard multilayer PCB. For example, in a four layer PCB stack, the two layers in the center can be used as ground plane. As shown in Fig. 4, the upper ground layer GND1 is present under the microstrip where a thin dielectric is needed while GND0 is present under a complete PCB.

Note that the two-ground planes under the microstrip do not provide a continuous path for return current. Therefore, the return current path will be determined by the frequency of the signal and location of the nearest connection between the two ground planes GND0 and GND1. The large numbers of fat vias are placed to connect the GND1 and GND2 as shown in Fig. 5. These vias play an important role to keep both the ground planes at same potential and provide the bounce free ground. To provide the deterministic path for the return ground

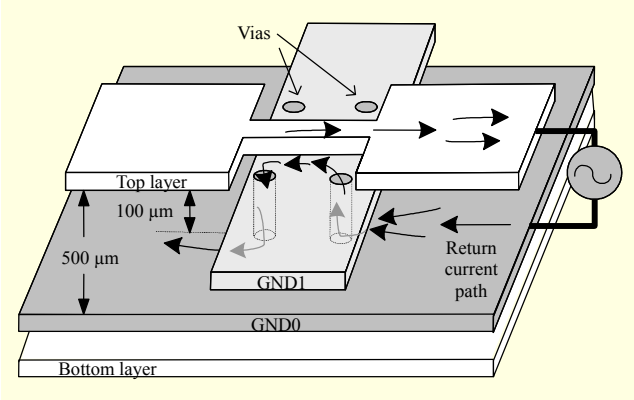

Fig. 4. Four layer standard FR4 PCB stack.

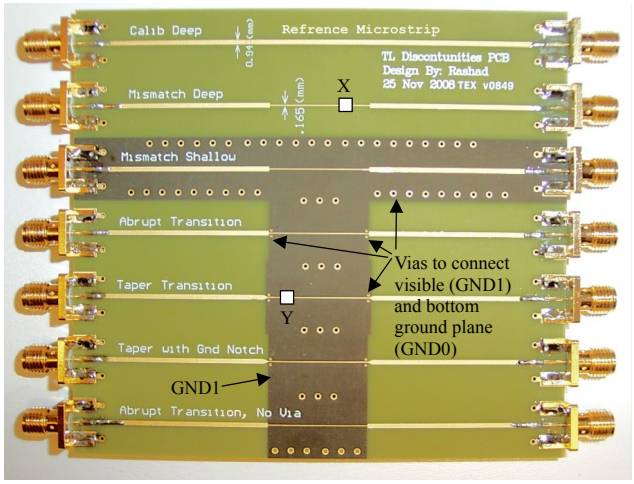

Fig. 5. Test PCB to characterize microstrip discontinuity due to step change in width and substrate thickness.

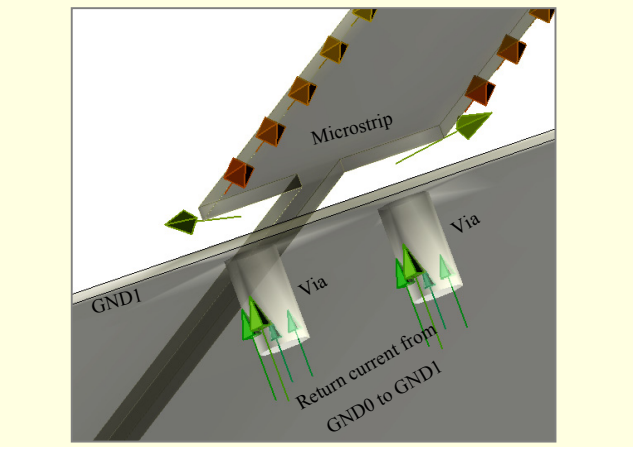

Fig. 6. Simulated 3D plot of ground return current.

currents, we have placed thin vias between the two ground planes close (100 µm as allowed by PCB manufacturing rules) to the width discontinuity as shown in Figs. 4 and 6. These vias carry the major portion of return RF current. An extremely small portion of RF current returns through remote fat vias and common SMA connector ground connections. This fact is confirmed by a simulation performed at 2.4 GHz. A 3D view of the RF current flow is shown in Fig. 6. The arrows show the magnitude and direction of current.

To characterize and understand the different aspects of reflection-free microstrips, we have simulated and manufactured seven variants of microstrips as shown in Figs. 7 and 8.

The microstrip parameters are derived from the real world needs to measure a wideband (1 GHz to 6 GHz) ΣΔ RF front-end with twelve high-speed I/Os (Fig. 1). A typical FR4 PCB manufacturer can manufacture a minimum line width of 100 µm ±10% (≈4 mil) with 100 µm ±10% spacing. The

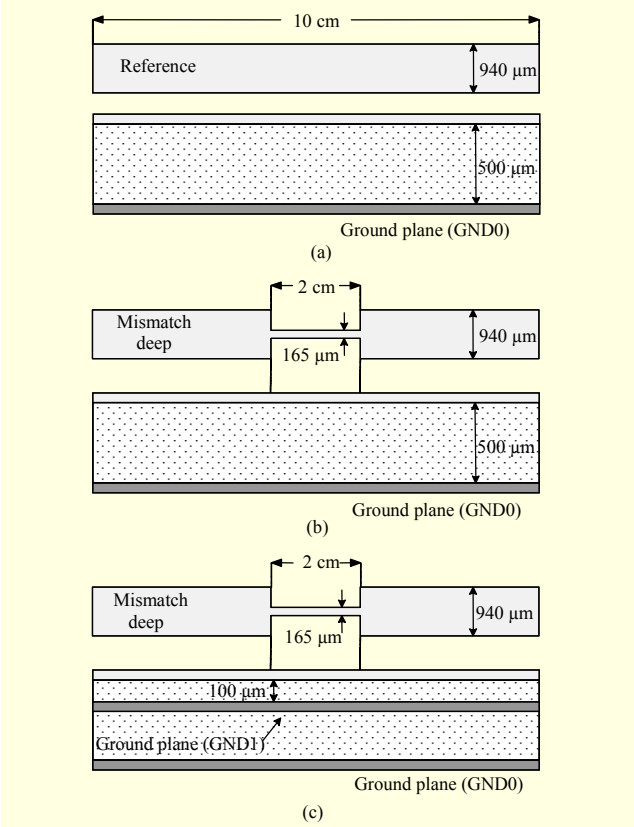

Fig. 7. (a) Reference microstrip with 500 µm dielectric, (b) mismatched microstrip with 500 µm dielectric, and (c) mismatched microstrip with 100 µm dielectric.

commercial off-the-shelf FR4 laminate and prepreg is available in a variety of thickness starting from 50 µm to a few millimeters. Therefore, any substrate thickness in multiples of 50 µm can easily be manufactured.

The chip size is 1 mm×1 mm, and we decided to use three edges of the chip to layout the twelve microstrips. A 165 µm wide track with 100 µm thick substrate constitutes the 50 Ω TL. Four microstrips can easily be laid out extremely close to the chip pads using 100 µm line spacing as shown in Fig. 1.

The other side of the TL has to be connected with the SMA connector. The solder pin diameter of typical low cost DC to an 18 GHz SMA connector is 800 µm ±5%. To minimize the reflection from an SMA connector to a microstrip transition, we decided to use a line width of 1,000 µm. Simulation results show that a 940 µm wide track makes a 50 Ω TL on a 500 µm thick FR4 substrate. This width is enough for an SMA connector pin landing pad and soldering with minimum outward bulging, thus resulting in minimum reflections [3], [8]. Based upon these real world specifications, we have designed the two PCBs. The first PCB shown in Fig. 5 is one of the sample test boards to verify the concept of low-reflection TLs. Eight sample PCBs, manufactured from a commercial PCB

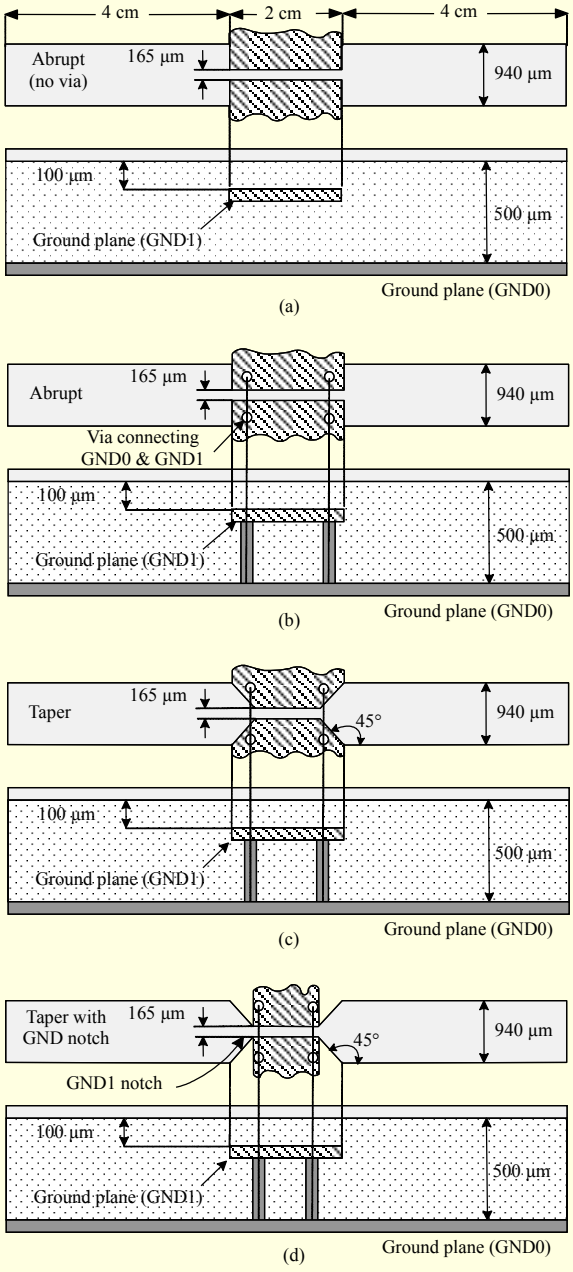

Fig. 8. (a) Microstrip with abrupt change in width with no vias, (b) abrupt change in width, (c) tapered change in width, and (d) tapered change in width and ground notch under tapered portion.

manufacturing facility in Stockholm, were capable of the placement of 100 µm tracks with 100 µm spacing with ±10% tolerance. The same tolerance in substrate thickness was guaranteed by the manufacturer. Physical measurement of the reference track on all eight PCBs showed that all sample PCBs meet the specified tolerance limits both in track width and substrate thickness. The physical measurement of a sample PCB is shown in Fig. 9. An *S*-parameter and TDR

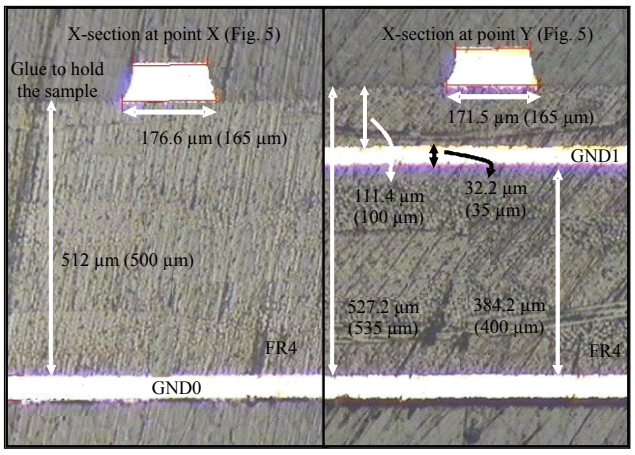

Fig. 9. Cross-section showing manufactured substrate dimensions of test PCB at point X and Y in Fig. 5. The target dimensions are shown in parentheses.

measurement included in this paper belong to the PCB shown in Figs. 5 and 9. Based on these measurements, we can safely assume that the proposed technique works satisfactorily for the manufacturing tolerances well within the capability of today's commercial PCB manufacturers without any special precision enhancement procedures.

The second PCB shown in Fig. 1 uses the proposed low-reflection TLs for the successful measurement of wideband RF front-end.

Figure 7(a) shows the 10 cm long 50 Ω microstrip without any discontinuity that serves as the reference or benchmark for the other measurements. The two cases of microstrip with step discontinuity in width are shown in Figs. 7(b) and (c). In the first case (mismatch deep), the wide portion of the microstrip is designed for 50 Ω, while the center part has higher impedance. The second case (mismatch shallow) is just opposite of above, where the center part has 50 Ω impedance, while the right and left parts have considerably lower impedance. These two cases are a measure of the step discontinuity in width with uniform substrate thickness.

The microstrips shown in Fig. 8 are designed to evaluate the collective impedance variation caused by the simultaneous change in width and substrate thickness.

The microstrip in Fig. 8(a) includes an abrupt transition from one width to another width without any nearby vias connecting the GND planes. The two ground planes are connected together mainly at the SMA connectors and a number of vias far from the microstrip.

The microstrip in Fig. 8(b) is same as in Fig. 8(a) but with four vias connecting the two ground planes in close proximity to the width discontinuity.

The microstrip in Fig. 8(c) shows a tapered transition. Tapering is a well-known technique for smooth width transitions to reduce reflections. The microstrip in Fig. 8(c) is tapered at 45° with four vias connecting the two ground planes. Moreover, the GND1 layer extends under the complete tapered portion of the microstrip.

As shown in Fig. 8(d), the tapered portion is not completely covered from the ground (GND1) plane underneath. Only approximately 5% of the taper area has a GND1 layer underneath in the form of triangular notch.

All of the microstrips shown in Figs. 7 and 8 are manufactured on a FR4 test PCB shown in Fig. 5. The T-shaped dark area visible from the top is GND1, and it provides a substrate thickness of 100 µm to the narrow part of lower four microstrips. The GND0 plane completely covers the test PCB. All the planar metal structures on this PCB are composed of 1/2-oz copper with gold plating on the top surface of microstrips.

IV. Simulation and Measurement Results

To evaluate the cumulative impedance discontinuity, *S*-parameters were measured using the Rhodes & Schwarz ZVM

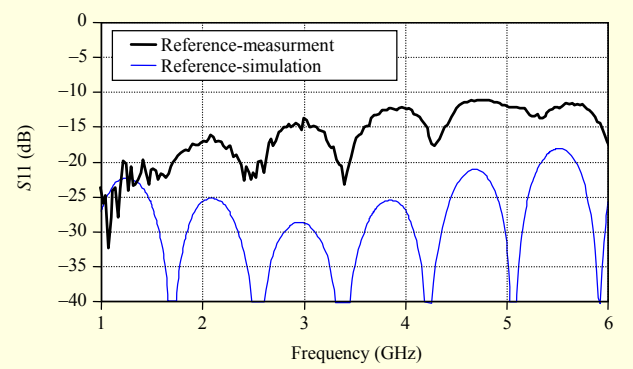

Fig. 10. Measured and simulated input reflection coefficient (*S*11) for reference microstrip.

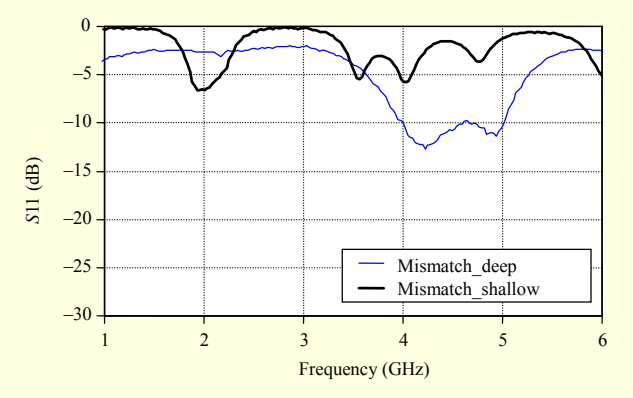

Fig. 11. Measured input reflection coefficient (*S*11) for microstrip with step change in width (Fig. 7(b)).

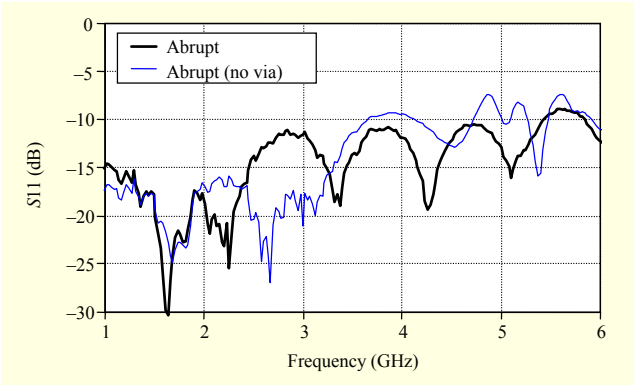

Fig. 12. Measured input reflection coefficient (*S*11) for microstrip with abrupt change in width with and without vias.

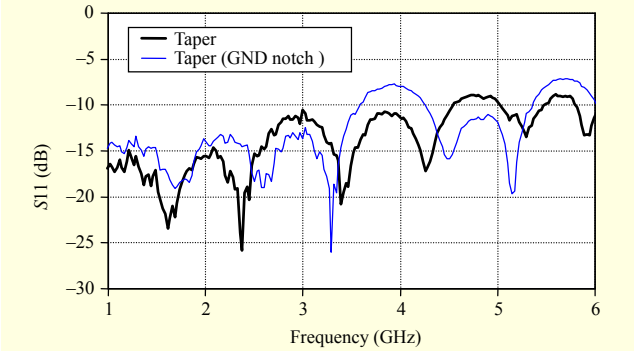

Fig. 13. Measured input reflection coefficient (*S*11) for tapered and GND notch microstrip.

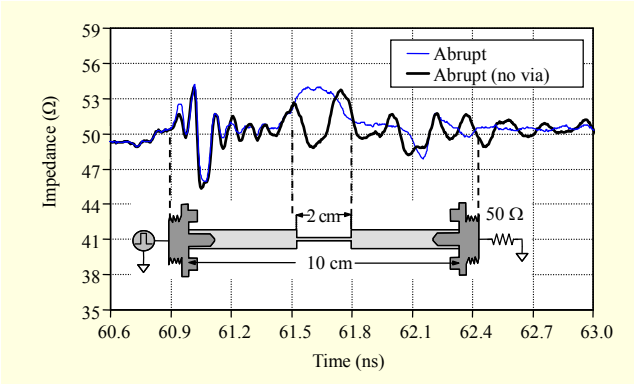

Fig. 14. TDR measurements for microstrip with abrupt change in width (with and without vias).

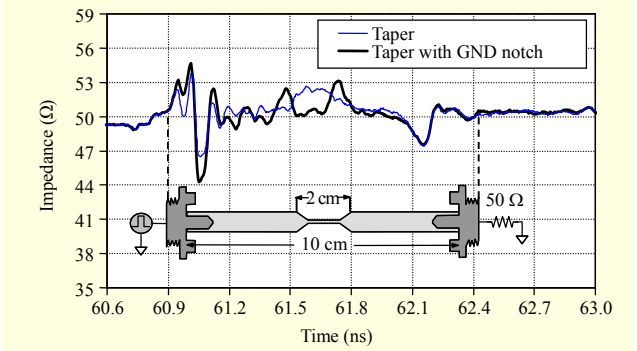

Fig. 15. TDR measurements for microstrip with tapering and with GND notch.

Vector Network Analyzer. To trace the location and magnitude of impedance discontinuities, TDR measurements were performed using an Agilent 54754 TDR module on test PCB (Fig. 5) using a 35 ps pulse width [7].

The *S*-parameter simulation and measurement results are plotted in Figs. 10 to 13. The measured reflection coefficient for the reference microstrip is better than –10 dB for the frequency range 1 GHz to 6 GHz. The reflection coefficient for an uncompensated microstrip with a step change in width is extremely poor with a value of only –2d B for the frequency ranges 1 GHz to 3 GHz and 5.5 GHz to 6 GHz (Fig. 11). Both the abrupt and taper microstrips (Figs. 12 and 13) have a frequency response close to –10 dB with minor differences for the entire frequency range 1 GHz to 6 GHz. This value is very close to the performance of the reference microstrip.

The abrupt microstrip with nearby vias for ground current has better response compared to its counterpart without nearby vias (Fig. 12) for the frequencies greater than 3.5 GHz. The TDR measurements of the same microstrips (Fig. 14) show that the abrupt microstrip with a via has stable 53 Ω impedance, while the version without a via has poor impedance control. The probable reason is the larger and indistinct inductance loop formed by the return current in absence of vias; hence, the poor impedance control. However, this is not true for all frequencies as the displacement current in the cavity is critical as return current; thus, the indistinct inductance loop becomes highly frequency-dependent, and we see different behavior at low and high frequencies.

In Fig. 13, the behavior of two taper microstrips is plotted. In this case, both the tapered microstrips have nearby GND vias. The difference is the GND notch in one microstrip as shown in Fig. 8(d). The frequency domain measurements show that the *S*11 response of the microstrip with the GND notch is better in frequency range 2.4 GHz to 3.4 GHz and 4.3 GHz to 5.3 GHz. The TDR measurements of the same microstrips (Fig. 15) show that the SMA discontinuity of the microstrip with a GND notch is higher than its counterpart. Since the frequency domain results represent the amalgamated picture of SMA and microstrip discontinuities, TDR measurements show that there is no significant difference between the behavior of the two tapered microstrips with or without a GND notch. The length of tapered section is approximately 800 μm, which is more than thirty times smaller than the minimum wavelength of interest (≈2.5 cm at 6 GHz in copper microstrip). Therefore, the

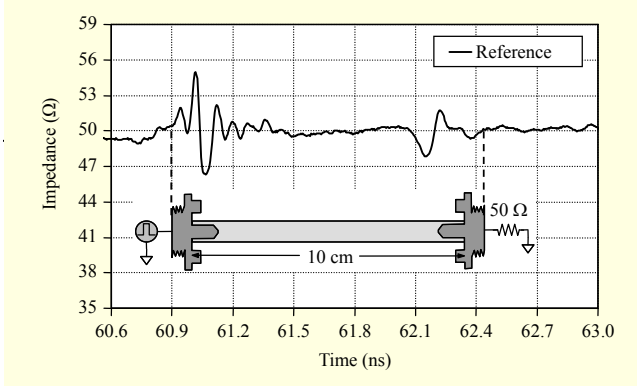

Fig. 16. TDR measurement for reference microstrip.

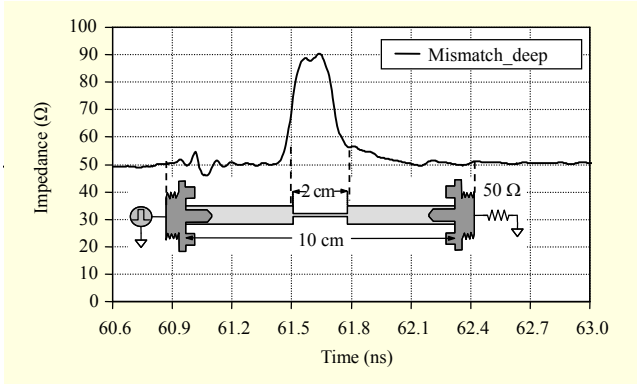

Fig. 17. TDR measurement for microstrip with step change in width.

ground plane (GND1) covering the complete tapered portion gives similar results compared to the ground notch option. The ground notch can be better in a case where the taper geometry becomes comparable to the wavelength.

There is a discrepancy between the simulation and measurement results (Fig. 10) for the reference microstrip. The major cause of this difference is the fact that SMA connectors are not modeled and included in the schematic level simulation of reference microstrip since the model of the hand soldered SMA changes notably from microstrip-to-microstrip even on the same PCB. The differences in the SMA-to-microstrip discontinuity is manifested in TDR measurements in Figs. 14 to 17. Another reason is the divergence in dimensions of the designed and the manufactured microstrips. The physical dimensions of the microstrip structures on eight manufactured PCBs reveal that the 940 μm and 165 μm tracks have width errors of 1.5% and 8.5%, respectively. Similar variations are observed in the thicknesses of the FR4 dielectrics. The cross-section of the test PCB taken at location X and Y (Fig. 5) is shown in Fig. 9. The thin dielectric geometries are prone to higher manufacturing tolerances. For example, the 100 μm thick FR4 layer is found to be 111.4 μm after manufacturing.

Another probable cause of this difference is the hand soldering of the SMA connector with 1.4 mm wide cut in mounting flanges on the test PCB which is 0.6 mm thick. This means that the SMA pin has to be manually centered and leveled on a 50 Ω PCB track. Therefore, lack of mounting precision causes the additional mismatch. This mismatch between coaxial SMA connector and the planar microstrip [3], [8] is very clearly visible in TDR measurement. This mismatch is very pronounced in all the TDR plots shown in Figs. 14 to 17 with numerical values close to 6 Ω, whereas the cumulative mismatch due to step changes in width and step change in substrate is close to 3 Ω. This can be compared to the unmatched case where there is a difference of 40 Ω, as observed in Fig. 17. The time domain TDR measurements comply with frequency domain *S*-parameter measurements for all microstrips.

As the time and frequency domain performance of abrupt and tapered microstrips are very close to the reference microstrip, these microstrips are suitable for any practical application. In real world applications, the response will be even better as there will be one width discontinuity as shown in Fig. 1 compared to two width discontinuities present on the test PCB in Fig. 5.

V. Conclusion

In this paper, a practical low-cost solution was presented to mount and test bare chips having multiple high-speed I/Os. To meet the physical area constraints, narrow 50 Ω microstrips are laid close to the chip. These microstrips change their width when they move away from the chip. The impedance discontinuity due to change in the width of the microstrip is neutralized using a change in substrate thickness.

Both frequency and time domain measurements show acceptable response, that is, *S*11 better than –9 dB in the range of 1 GHz to 6 GHz for two width discontinuities in a single microstrip without precision manufacturing. The comparison

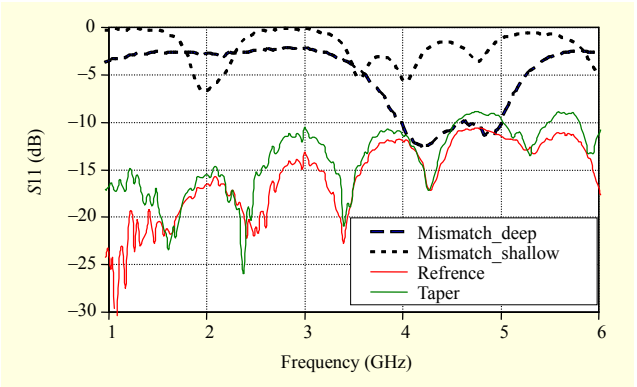

Fig. 18. Comparison of reference microstrip with mismatched and compensated taper microstrip.

between the reference, mismatched deep, mismatched shallow, and compensated tapered microstrip has been drawn in Fig. 18. It is evident that the response of the compensated taper (and also the abrupt) microstrip is very close to the reference microstrip. This clearly shows the effectiveness of the proposed technique to cancel out the mismatches due to microstrip width discontinuity. The further improvement in the reflection coefficient is possible with low tolerance microstrip manufacturing and precision mounting of SMA connectors.

This technique is successfully applied to measure a 1 mm× 1 mm ΣΔ RF front-end with sixteen high-speed I/Os using an ordinary multilayer FR4 PCB. This technique is equally applicable to other types of multilayer PCBs with the possibility that controlled impedance microstrips and striplines can be designed on any PCB layer. Even the transition from one PCB layer to another is possible when a controlled impedance via structure is used [9], [10]. Another possible application is in high-density hybrid designs where multiple bare chips are mounted very close to each other.

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