Sampling Jitter Effect on a Reconfigurable Digital IF Transceiver to WiMAX and HSDPA

Bong-Guk Yu, Jaekwon Lee, JinUp Kim, and Kyutae Lim

This paper outlines the time jitter effect of a sampling clock on a software-defined radio technology-based digital intermediate frequency (IF) transceiver for a mobile communication base station. The implemented digital IF transceiver is reconfigurable to high-speed data packet access (HSDPA) and three bandwidth profiles: 1.75 MHz, 3.5 MHz, and 7 MHz, each incorporating the IEEE 802.16d worldwide interoperability for microwave access (WiMAX) standard. This paper examines the relationship between the signal-to-noise ratio (SNR) characteristics of a digital IF transceiver with an under-sampling scheme and the sampling jitter effect on a multichannel orthogonal frequency-division multiplexing (OFDM) signal. The simulation and experimental results show that the SNR of the OFDM system with narrower band profiles is more susceptible to sampling clock jitter than systems with relatively wider band profiles. Further, for systems with a comparable bandwidth, HSDPA outperforms WiMAX, for example, a 5 dB error vector magnitude improvement at 15 picoseconds time jitter for a bandwidth of WiMAX 3.5 MHz profile.

Keywords: Software defined radio (SDR), time jitter, digital IF, mobile communication.

Manuscript received June 9, 2010; revised Aug. 25, 2010; accepted Sept. 10. 2010.

Bong-Guk Yu (phone: +82 42 860 1755, email: bgyu2@etri.re.kr) was with the Georgia Electronic Design Center, Georgia Institute of Technology, Atlanta, Georgia, USA, and is now with the Internet Research Laboratory, ETRI, Daejeon, Rep. of Korea.

Jaekwon Lee (email: breeze@kbs.co.kr) is with the Technical Research Institute, Korea Broadcasting System, Seoul, Rep. of Korea.

JinUp Kim (email: jukim@etri.re.kr) is with the Internet Research Laboratory, ETRI, Daejeon, Rep. of Korea.

Kyutae Lim (email: ktlim@ece.gatech.edu) is with the Georgia Electronic Design Center, Georgia Institute of Technology, Atlanta, Georgia, USA.

doi:10.4218/etrij.11.0110.0339

I. Introduction

Software-defined radio (SDR) technology is a promising feature that makes it possible to accommodate several standards through software changes on a single hardware platform for next-generation mobile communication systems. Mobile network operators can rapidly provide state-of-the-art services to their customers with a low cost of deployment and maintenance if SDR technology is applied to their mobile communication base stations.

These advantages have led many research institutes to proceed with worldwide commercialization of software radio technology. This paper presents an SDR-technology-based digital intermediate frequency (IF) transceiver for a mobile communication base station that is reconfigurable to three bandwidth profiles: 1.75 MHz, 3.5 MHz, and 7 MHz, each incorporating the IEEE 802.16d worldwide interoperability for microwave access (WiMAX) standard based on orthogonal frequency-division multiplexing (OFDM) technology [1].

It is also reconfigurable to the high-speed download packet access (HSDPA) standard based on wideband code-division multiple-access (WCDMA) technology [2], [3]. This reconfigurable mobile base station, which incorporates heterodyne architecture, uses SDR technology in which modems and other functional blocks can be reconfigured easily by software downloaded onto identical hardware platforms [4].

The presented transceiver manages the digital IF function in the base station and can be reconfigured to other standard profiles through software downloaded onto identical hardware platforms, without changing any components or parts on the board. The main functions of the digital IF transceiver include the frequency up-conversion of a baseband signal from a modem to an analog IF signal and the frequency down-

conversion of an analog IF signal from a radio frequency (RF) transceiver to a digital baseband signal.

The designed digital IF transceiver adopted a bandpass sampling scheme, also known as under-sampling, in which sampling clock purity is very important [5], [6]. Because the under-sampling process requires replacement of the RF or IF signal onto the baseband signal in recovering the original signal, signal-to-noise ratio (SNR) degradation by folding, sampling jitter, and analog to digital converter (ADC) quantization noise cannot be avoided [7].

It is well known that the performance of an OFDM system is highly dependent on the frequency offset error and phase noise at the receiver side compared to a code-division multiple-access (CDMA) system [8]. Aperture jitter can introduce phase noise in the bandpass sampling process and result in an instantaneous randomly varying frequency offset. The frequency offset results in inter-carrier interference (ICI) and a loss of orthogonality between the subcarriers in an OFDM system [9]. This paper presents the simulation and experimental results that demonstrate the SNR performance of the designed digital IF transceiver operated on hardware that is identical to the hardware of an OFDM system and a CDMA system using an under-sampling scheme, which is closely related to sampling clock jitter characteristics.

This paper is organized as follows. In section II, a theoretical background of jitter effect on system performance and the simulation results will be discussed. In section III, we present the overall designed digital IF transceiver architecture and implemented printed circuit board assembly module. In addition, we propose a time jitter generation module. Here, the experimental results presented show the error vector magnitude (EVM) performance to the sampling time jitter of the designed reconfigurable digital IF transceiver for various design systems. Finally, concluding remarks are presented in section IV.

II. Simulation Results

The main contributing factor affecting an analog-to-digital converter (ADC) sampling clock jitter is white noise, phase noise, and spurious components. These components are all merged and emerge as the total amount of jitter. If we assume the input signal as a sinusoidal in ADC processing, then

$$v(t) = A\sin(2\pi ft). \tag{1}$$

Here, A is the amplitude and f is the frequency of the input signal. Time derivative of the signal follows (2) and (3).

$$\frac{dv(t)}{dt} = 2\pi fA\cos(2\pi ft), \tag{2}$$

$$\frac{\Delta v_{\text{i\_RMS}}}{\Delta t_{\text{j\_RMS}}} = 2\pi fA\sqrt{\int_{-0.5f}^{0.5f}\cos^2(2\pi ft)dt} = \sqrt{2}\pi fA, \tag{3}$$

where $\Delta v_{\text{j\_RMS}}$ represents the amount of root-mean-square (RMS) jitter noise and $\Delta t_{\text{j\_RMS}}$ means the amount of time jitter. If the jitter has a normal distribution with an average 0 and variance $\sigma_{\text{j}}^2 = \Delta t_{\text{j\_RMS}}^2$, then the RMS noise voltage is

$$\Delta v_{\text{j\_RMS}} = \sqrt{2}\pi fA\sigma_j. \tag{4}$$

Therefore, the SNR can be represented by

$$\begin{aligned} SNR_{\text{jitter}} &= 20\log\left(\frac{A/\sqrt{2}}{\Delta v_{\text{j\_RMS}}}\right) \\ &= 20\log\left(\frac{1}{2\pi f\cdot\Delta t_{\text{j\_RMS}}}\right) \\ &= 20\log\left(\frac{1}{2\pi f\cdot\sigma_{\text{j\_RMS}}}\right). \end{aligned} \tag{5}$$

In (5), f is the input signal frequency at which the sampling occurs and $\sigma_{\text{j\_RMS}}$ is the RMS aperture jitter. As can be seen in (5), the SNR decreases as the input IF and the amount of aperture jitter increase. An alternative SNR expression resulting from a flat wideband signal results in (6) [6].

$$SNR_{\text{sig}} = \frac{1}{4\pi^2\sigma_t^2\left(f_0^2 + \frac{BW^2}{12}\right)}. \tag{6}$$

Here, σ_t is the phase jitter in RMS seconds, f_0 is the signal frequency, and BW represents the signal bandwidth. When the 10*log is taken to the right side of (6), nearly identical results are found regardless of the bandwidth as long as the condition $f_0 > 10$ BW is satisfied.

We show the simulation results to identify the sampling clock jitter effects on the performance of CDMA and OFDM systems. Figure 1 shows a block diagram of the jitter effect simulation for an HSDPA system.

The input sequences are generated by a random generator and are symbol-mapped in the transmitter. This signal is widely spread and interleaved to be the final HSDPA signal. Then, the baseband signal is upsampled by a factor of 4 and upconverted to an intermediate carrier frequency. The signal is then transmitted through the additive white Gaussian noise channel. At the receiver, the IF band signal is added with the jitter signal while analog-to-digital conversion is processed. Figure 2 shows a block diagram for a WiMAX system simulation. The binary phase shift keying (BPSK) symbol-mapped signals are processed by a typical OFDM system in the transmitter. As the signal bandwidths and digital sample rates differ for each of the

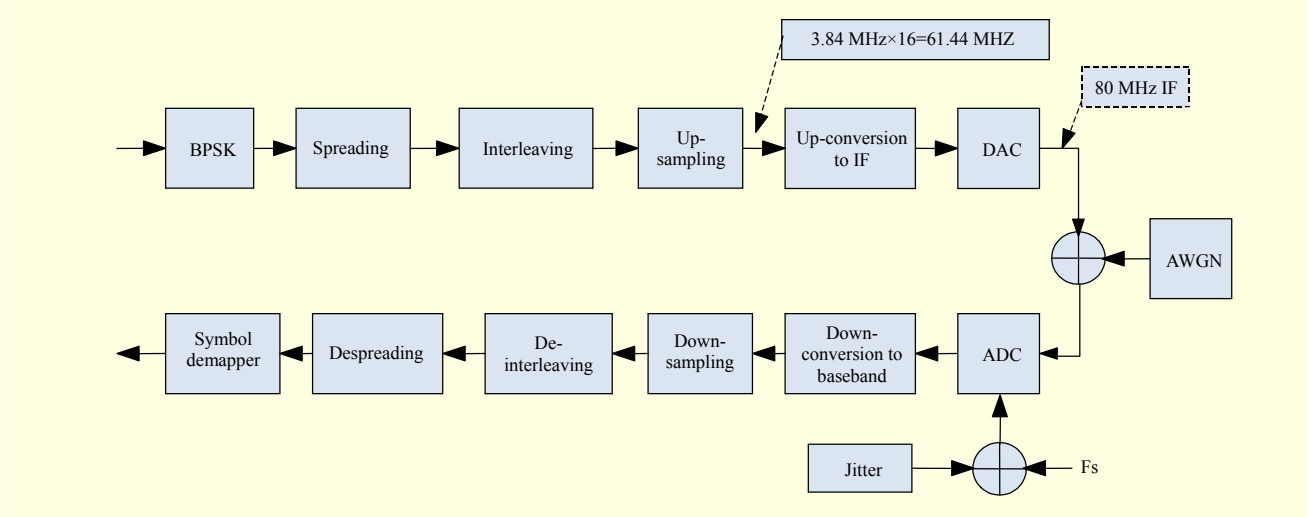

Fig. 1. Jitter effect simulation model for HSDPA.

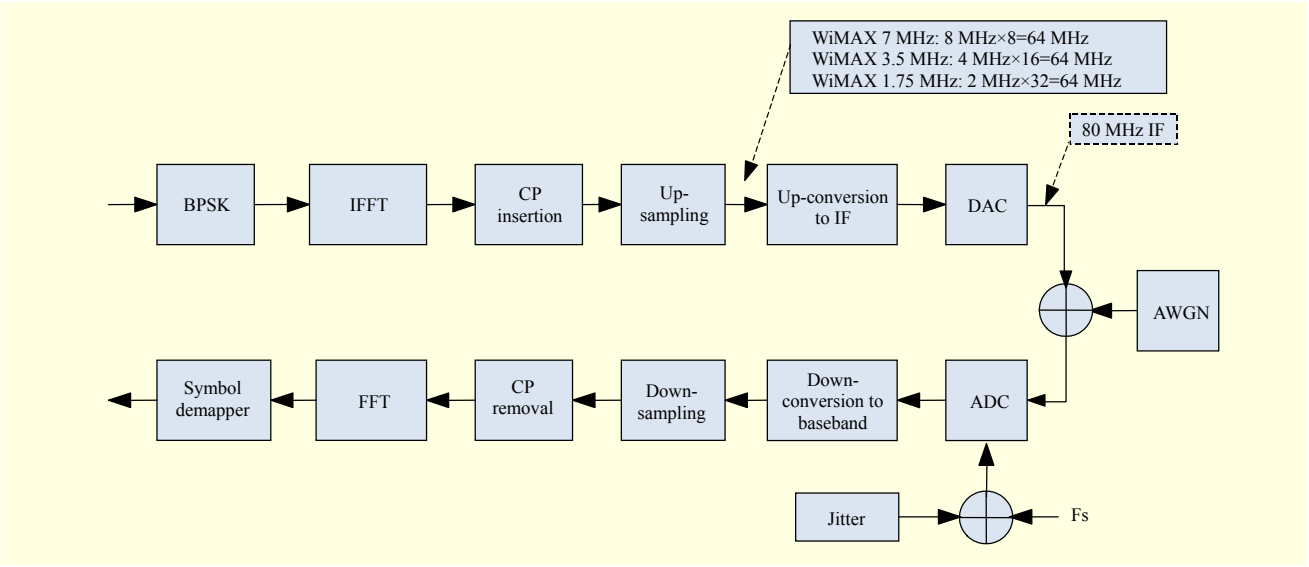

Fig. 2. Jitter effect simulation model for WiMAX.

OFDM system profiles, the filters should be designed individually to accommodate 3 WiMAX profiles: 1.75 MHz, 3.5 MHz, and 7 MHz.

The designed digital finite impulse response (FIR) filter specifications for interpolation and decimation are shown in Table 1 according to the HSDPA system and three WiMAX profiles. The same filter coefficient set was used on the down-conversion side for the receiver in simulation and hardware implementation.

The simulation parameters in Table 2 show the uplink input signal parameters of each system to verify the SNR degradation according to the amount of time jitter. Each profile of the WiMAX system has the same FFT size but a different subcarrier spacing due to the different signal bandwidth of each profile. All input signals were BPSK modulated. We used the same input parameter for the experimental test in section III.

Figure 3 shows the SNR performance degradation due to time jitter for the various system profiles with the same simulation condition. The theoretical curve in Fig. 3 was achieved using (6).

As can be seen in Fig. 3, each system including the three WiMAX profiles shows a different SNR performance. In the case of the WiMAX profiles, the SNR values with narrower signal bandwidth profiles are more severely decreased as the amount of jitter is increased. When comparing the HSDPA system to WiMAX 3.75 MHz with similar signal bandwidths, the SNR performance curve shows that the HSDPA system has better performance than the WiMAX system due to specific jitter. Figures 4 and 5 represent the simulation results about the bit error rate (BER) performance due to RMS time jitter when

Table 1. FIR filter specifications.

Profile	HSDPA	WiMAX 1.75 MHz	WiMAX 3.5 MHz	WiMAX 7 MHz
FIR type	Raised cosine	Raised cosine	Raised cosine	Raised cosine
Window	Hamming	Hamming	Hamming	Hamming
Interpolation rate	4	4	8	16
Decimation rate	2	4	8	16
Rolloff	0.22	0.115/0.115	0.115	0.115
Number of taps	129	129/129	129	129
Sampling freq. (MHz)	61.44	64/8	64	64
Cutoff freq. (MHz)	2.8	2/1.2	2	3.5
Coefficient resolution (bits)	16	16/16	16	16

Table 2. Input signal parameters.

Profile	HSDPA	WiMAX 1.75 MHz	WiMAX 3.5 MHz	WiMAX 7 MHz
Duplex	FDD	FDD	FDD	FDD
Modulation and coding	BPSK	BPSK RS-CC 1/2	BPSK RS-CC 1/2	BPSK RS-CC 1/2
Data rate (kbps)	3,840	694.44	1388.9	2,777.8
Frame duration (ms)	2	8	5	5
Cyclic prefix	-	1/8	1/8	1/8
Number of FFT	-	256	256	256
Number of used subcarrier	-	200	200	200
Subcarrier spacing (kHz)	-	7.8125	15.625	31.25

the jitter equals 20 picoseconds (ps) and 60 ps, respectively. The theoretical result curve in the figure means a theoretical BER curve of the BPSK signal and showed as performance criteria.

In the case of Fig. 4, the RMS jitter is introduced to the simulation process with the relatively small amount of 20 ps. Therefore, all the systems against the jitter effect are similar to the theoretical results. Whereas, when the amount of RMS jitter is increased to 60 ns as shown in Fig. 5, the performance of the WiMAX 1.75 MHz profile, which has the narrowest signal bandwidth among the three WiMAX profiles, shows the worst performance. In addition, the HSDPA system shows a better performance than the WiMAX 3.75 MHz profile, which has a similar signal bandwidth.

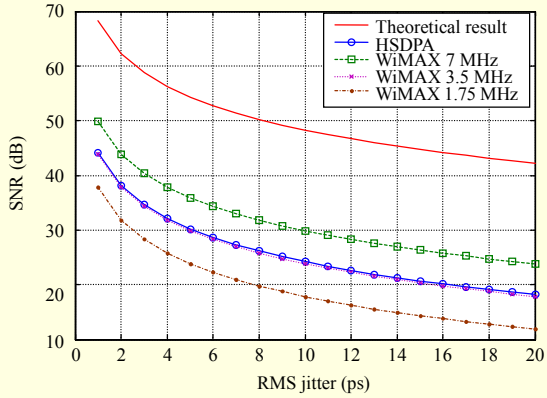

Fig. 3. SNR performance degradation.

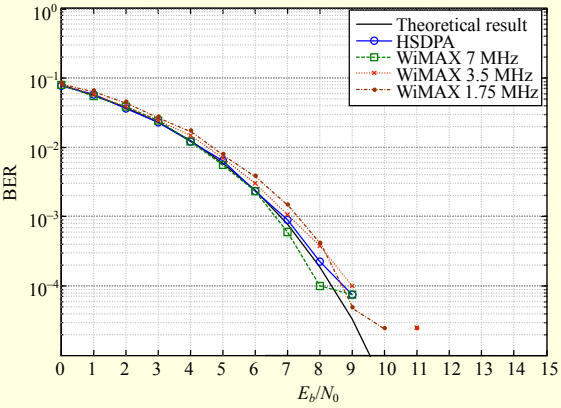

Fig. 4. BER performance when RMS jitter = 20 ps.

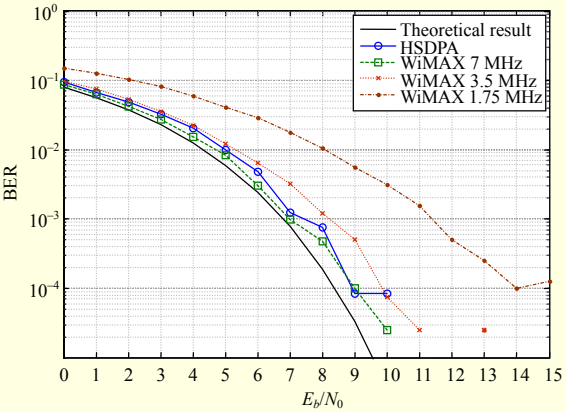

Fig. 5. BER performance when RMS jitter = 60 ps.

III. Experimental Results

1. Implementation of Digital IF Transceiver

The transmitter architecture of the transceiver for a HSDPA base station supporting two frequency assignments (FAs) is

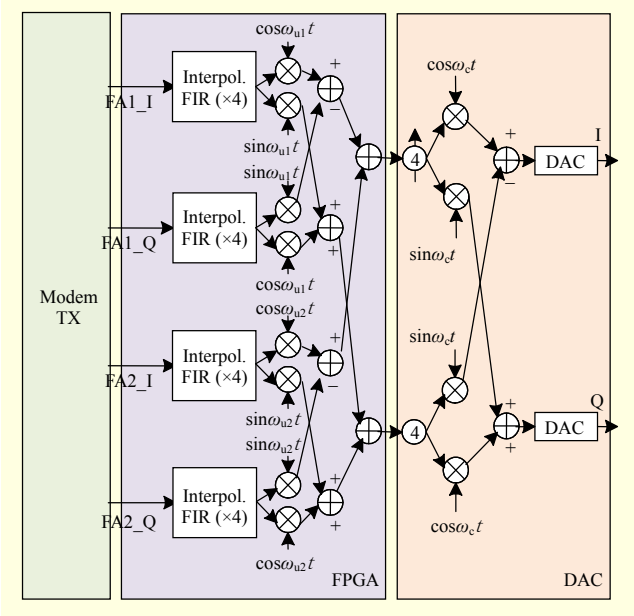

Fig. 6. Digital IF up-conversion block diagram of HSDPA.

shown in Fig. 6. It requires a functional block for frequency up-conversion and digital combining of two FA signals for the downlink direction. The digital I/Q baseband signals received from a modem corresponding to each FA are sent to the digital IF transmitter at a rate of four oversamples of the fundamental frequency of the HSDPA system.

Each digital signal is interpolated to a higher sample rate signal by passing through the ×4 interpolation FIR filters. In Fig. 6, each signal is a digital complex quadrature modulated to a higher frequency using a numerically controlled oscillator (NCO) to remove the image signals. After this modulation, the two FA signals are digitally combined to each inphase and quadphase signal entering the commercial DAC chip. Here, ω_{u1} is 16.16 MHz, ω_{u2} is 20.96 MHz, and ω_c is 61.44 MHz for the HSDPA system.

The DAC operates at a data rate of 61.44 MHz and uses two halfband filters to achieve ×4 interpolation function internally. Finally, it outputs an IF analog signal of 80 MHz after being upconverted by 61.44 MHz via a digital complex quadrature modulation. Table 3 summarizes the main specifications of the digital IF transceiver for the downlink direction of each system.

Figure 7 shows the architecture of the receiver side for the uplink direction. The receiver side has two main functions, frequency down-conversion and channelization, that split one ADC output signal into two paths. The input of this receiver is an analog IF signal from an RF transceiver. Here, the RF transceiver down-converts the RF signal from a receiver antenna to an analog IF signal.

The analog IF signal entering the digital IF receiver part is oversampled by an ADC operating with a 61.44 MHz

Table 3. Transmitter specifications.

Profile	HSDPA	WiMAX 1.75 MHz	WiMAX 3.5 MHz	WiMAX 7 MHz
Output center freq. (MHz)	80	80	80	80
Number of FA	2	2	2	2
FA center freq. (MHz)	77.6/82.4	76/84	76/84	76/84
FA separation (MHz)	5	8	8	8
IF bandwidth (MHz)	10	9.75	11.75	15
FA bandwidth (MHz)	5	1.75	3.5	7
Output power (dBm)	–13	–13	–13	–13
Sample rate (MHz)	245.76	256	256	256
Digital data resolution (bits)	16	16	16	16
Impedance (Ω)	50	50	50	50
Modem interface	61.44 MHz LVDS	64 MHz LVDS	64 MHz LVDS	64 MHz LVDS

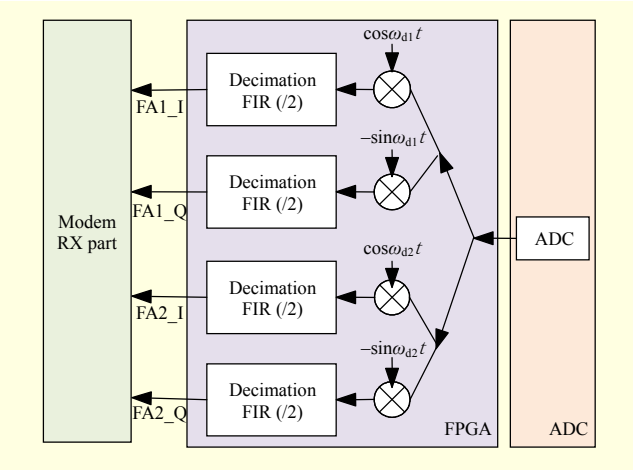

Fig. 7. Digital IF down-conversion block diagram of HSDPA.

sampling clock rate. This signal is then split into two paths for FA channel splitting. After being demodulated to the baseband signal using the NCO blocks, the output signal is downsampled by a factor of four through a decimation filter adapted to each I and Q path. Here, ω_{d1} is 16.16 MHz and ω_{d2} is 20.96 MHz, as shown in Fig. 7.

Table 4 shows the main specifications of the digital IF transceiver for the uplink direction of each system. The implemented transceiver hardware board is represented in Fig. 8. The transceiver board is operated at the digital

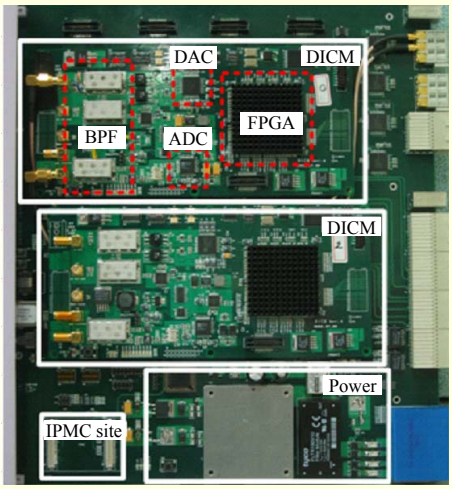

Fig. 8. Implemented digital IF transceiver hardware.

Table 4. Receiver specifications.

Profile	HSDPA	WiMAX 1.75 MHz	WiMAX 3.5 MHz	WiMAX 7 MHz
Input center freq. (MHz)	80	80	80	80
Number of FA	2	2	2	2
FA center freq. (MHz)	77.6/82.4	76/84	76/84	76/84
FA separation (MHz)	5	8	8	8
IF bandwidth (MHz)	10	9.75	11.75	15
FA bandwidth (MHz)	5	1.75	3.5	7
Input power (dBm)	–10	–10	–10	–10
Sample rate (MHz)	61.44	64	64	64
Digital data resolution (bits)	14	14	14	14
Impedance (Ω)	50	50	50	50
Modem interface	61.44 MHz LVDS	64 MHz LVDS	64 MHz LVDS	64 MHz LVDS

processing subsystem rack, which manages external network interfaces and the digital signal processing function of the SDR-based mobile communication base station.

The transceiver board can adopt two digital IF conversion modules (DICMs) to support a two-path transmitter and receiver diversity. One DICM on a transceiver board can process two channels simultaneously for one diversity path. In the DICM, a commercial DAC chip with 16 bit resolution was used. It converts a digital signal to an analog signal [10]. The chip has ×2/×4/×8 interpolation functionality internally and has a maximum output sample speed of 400 Msps. In the DICM, the DAC is capable of 245.76 Msps, which is equivalent to ×4 sampling speed of 61.44 MHz. In addition, an off-the-shelf ADC chip, which converts analog signals to digital signals, was used [11].

The overall digital signal processing for the digital IF block is implemented with a field programmable gate array (FPGA) chip [12]. This FPGA chip provides interpolation filtering, digital programmable NCO, digital complex quadrature modulation, FA combining for the digital up-conversion process, and FA channelization, demodulation, and decimation filtering for down-conversion.

2. Experimental Results

Figure 9 represents the overall jitter-effect test configuration for the digital IF transceiver uplink. The transceiver down-converts the analog IF signal of 80 MHz to the digital baseband signal. The EVM value of this baseband signal was measured using commercially available vector signal analyzer equipment.

The considered performance criterion was EVM, which is the most widely used modulation quality metric in digital communications systems. EVM is the root-mean-squared value of the error vector over time at the instants of the symbol clock transitions [13]. By convention, EVM is usually normalized to the outermost symbol magnitude at the symbol times and expressed as a percentage, as shown in the following equation:

$$EVM = \left(\frac{RMS\ error\ vector}{outermost\ symbol\ magnitude} \right) \times 100\% . \qquad (7)$$

Moreover, EVM with the unit of % RMS may be normalized to the square root of the average symbol power. In this way, EVM can be related to the SNR:

$$SNR = -20 \times \log \left(\frac{EVM}{100\%} \right). \qquad (8)$$

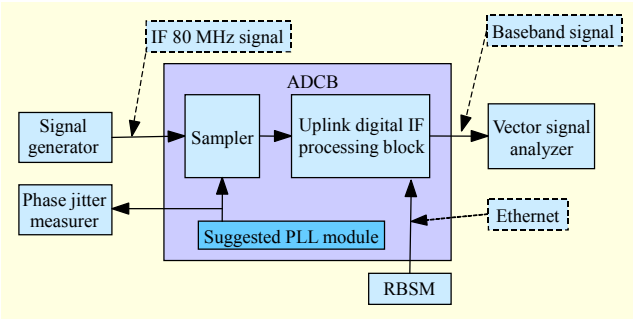

Fig. 9. Jitter effect test configuration.

The minimum requirement for transmit modulation of the HSDPA system is that the EVM shall not be worse than 12.5% RMS when the base station is transmitting a composite signal that includes 16 QAM modulation [14]. The EVM value of 12.5% RMS yields an SNR of 18.1 dB according to (8).

The reconfiguration to the HSDPA system and to the three WiMAX profiles was accomplished by downloading software through a middleware platform named reconfigurable base station manager that performs the overall reconfiguration, management, and operation of a SDR-based base station.

The sampling clock used to sample the IF signal was supplied by the suggested PLL module as shown in Fig. 10. In Fig. 10, the clock output of the PLL used as the sampling clock is contaminated by adding the voltage controlled crystal oscillator power to the noisy signal generated by a commercial arbitrary waveform generator. This noisy signal was intentionally generated and combined with the power signal supplied to the sampling clock made up of the PLL circuit. This noisy signal changes the time jitter of the sampling clock. The value of the time jitter of the sampling clock entering the ADC as an encode clock was measured by a spectrum analyzer with a phase noise personality measured in ps.

The captured EVM performance results for each system are presented in Fig. 11. The spectrum and constellation of each

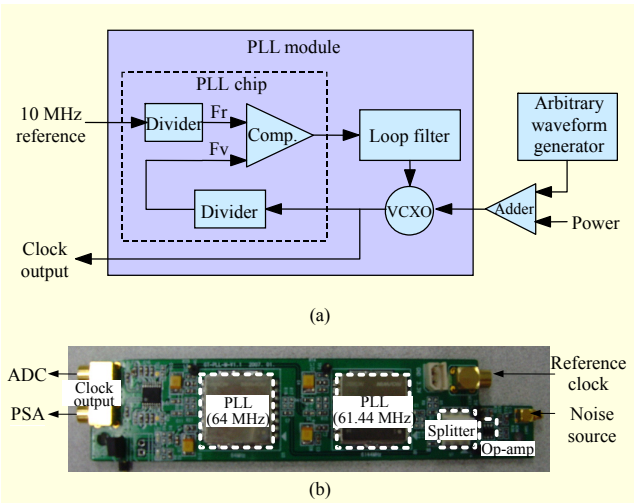

Fig. 10. (a) Block diagram of suggested PLL module and (b) implemented PLL module hardware.

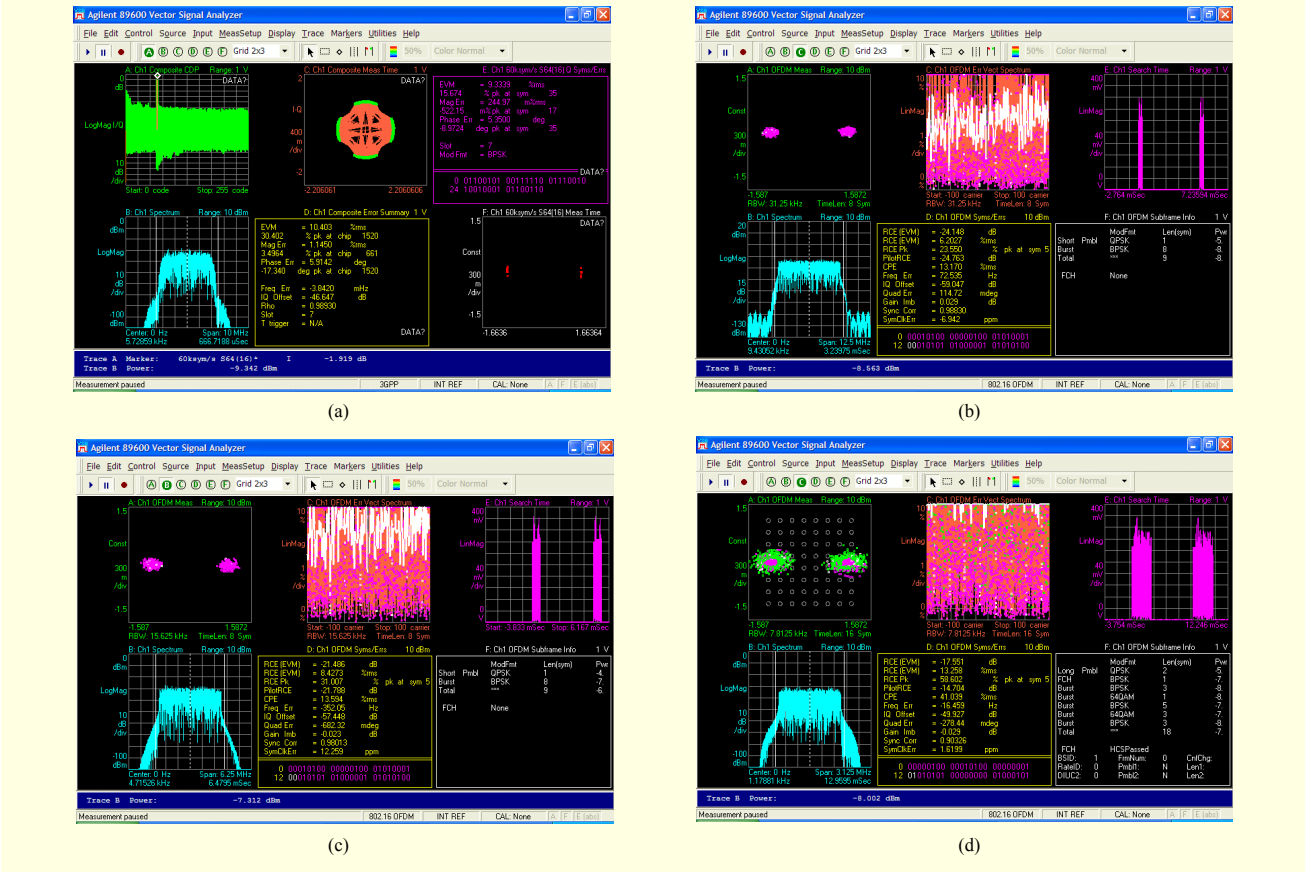

Fig. 11. Measured EVM performances of each system when RMS jitter, σ, is around 12 ps: (a) HSDPA: 19.7 dB when σ =12.6 ps, (b) WiMAX 7 MHz: 24.1 dB when σ =12.8 ps, (c) WiMAX 3.5 MHz: 21.4 dB when σ =12.1 ps, and (d) WiMAX 1.75 MHz: 17.5 dB when σ =11.6 ps.

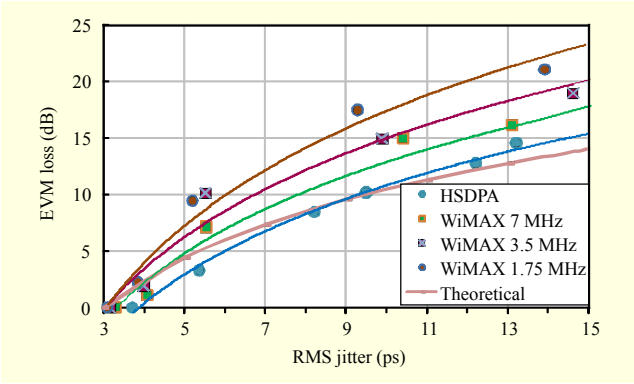

Fig. 12. Measured EVM loss due to RMS jitter.

system in the figures was obtained at a time jitter of approximately 12 ps. In addition, Fig. 12 shows the measured EVM performance degradation represented by a logarithmic curve produced by mapping the measured RMS time jitters in ps to the measured EVM loss sample values. The theoretical curve in Fig. 12 was achieved using (6).

As can be seen in Figs. 11 and 12, the experimentally measured values of the EVM performances of the HSDPA system and three WiMAX profiles are similar to the simulation results in Fig. 3.

In the case of the WiMAX systems, the EVM value decreases as the signal bandwidth decreases. Since the WiMAX 1.75 MHz profile has the narrowest subcarrier spacing among the three profiles, it showed the lowest EVM value. It was found that the time jitter is more critical to a narrower profile in an OFDM system. This is due to the ICI that was affected by the time jitter.

With respect to the time jitter, the HSDPA system outperforms the system with a WiMAX 3.5 MHz profile and comparable signal bandwidth. For example, at 15 ps time jitter, the EVM of the HSDPA system is 5 dB better than that of the WiMAX 3.5 MHz profile. Therefore, we can conclude that the multichannel OFDM system is more susceptible to the sampling time jitter than the multicode HSDPA system with similar bandwidth.

IV. Conclusion

In this paper, we presented an implemented SDR-based reconfigurable digital IF transceiver that can support an HSDPA system and three WiMAX profiles for a mobile communication base station. Additionally, SNR degradation to time jitter effect was evaluated by simulation and by examining the spectrum and constellation on the uplink baseband signal of the transceiver output using off-the-shelf equipment.

The study results verified that the performance degradation of the OFDM system according to the sampling clock time jitter is relatively high compared to a CDMA system. Moreover, performance degradation of the WiMAX 1.75 MHz profile with the narrowest subcarrier spacing was the greatest of the three implemented WiMAX profiles.

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Bong-Guk Yu received the BS, MS, and PhD in electronics engineering from Chungnam National University, Daejeon, Rep. of Korea, in 1992, 1994, and 2009, respectively. He worked as a research engineer from 1994 to 2000 at SK Telecom R&D Center, Seoul, Rep. of Korea, engaged in research on mobile communication systems and engineering. In 2000, he co-founded a start-up company and worked on developing wireless repeater systems. Since 2005, he has been with ETRI, Daejeon, Rep. of Korea, and has engaged in the research and development of 4th generation wireless mobile systems. From September 2009 to December 2010, he was with the Georgia Institute of Technology, Atlanta, Georgia, as a postdoctoral research fellow. His research interests include signal processing for wireless communication systems and cognitive radio.

Jaekwon Lee received his BS in electronics and radio engineering from Chungnam National University, Rep. of Korea, and his MS in mobile communication and digital broadcasting engineering from the University of Science & Technology, Rep. of Korea, in 2006 and 2008, respectively. In 2006, he joined ETRI as a student researcher. Since 2008, he has been working for the Korean Broadcasting System as a member of the research staff. His research interests are in next generation radio transmission technology, multiple antenna technique, digital RF, A-VSB, and HDTV.

JinUp Kim received the BS from Korea University, Seoul, Rep. of Korea, in 1985, and the MS and PhD from Korea Advanced Institute of Science and Technology, Seoul, Rep. of Korea, in 1987 and 1996, respectively. He has been with ETRI since 1987. He has also been a professor at the University of Science and Technology in the field of wireless communications since 2005. He has done research in the field of the wireless communication systems. His recent interests include digital RF, software defined radio, and cognitive radio technologies.

Kyutae Lim received the BS, MS, and PhD from Hanyang University, Seoul, Rep. of Korea, in 1991, 1993, and 1996, respectively. From 1996 to 2000, he was with the Samsung Advanced Institute of Technology, Giheung, Rep. of Korea, as a member of the technical staff. From 1998 to 1999, he has been with the Communication Research Lab of Ministry of Post and Telecommunication (currently NICT), Tokyo, Japan, as a research fellow. In January 2000, he joined the Microwave Application Group in the Georgia Institute of Technology as a senior research engineer. Currently he is serving as an associate director of the Georgia Electronic Design Center (GEDC) at the Georgia Institute of Technology, Atlanta, Georgia. His research interests include the cognitive radio wireless networks and systems, high-performance analog/mixed-signal circuits and systems, electromagnetic theory and antenna systems, and analogue signal processing and circuit implementation for ultra-low power electronics.