

# Wide-Band Fine-Resolution DCO with an Active Inductor and Three-Step Coarse Tuning Loop

YoungGun Pu, AnSoo Park, Joon-Sung Park, Yeon-Kug Moon, SuKi Kim, and Kang-Yoon Lee

**This paper presents a wide-band fine-resolution digitally controlled oscillator (DCO) with an active inductor using an automatic three-step coarse and gain tuning loop. To control the frequency of the DCO, the transconductance of the active inductor is tuned digitally. To cover the wide tuning range, a three-step coarse tuning scheme is used. In addition, the DCO gain needs to be calibrated digitally to compensate for gain variations. The DCO tuning range is 58% at 2.4 GHz, and the power consumption is 6.6 mW from a 1.2 V supply voltage. An effective frequency resolution is 0.14 kHz. The phase noise of the DCO output at 2.4 GHz is  $-120.67$  dBc/Hz at 1 MHz offset.**

**Keywords:** Wide tuning range, active inductor, automatic three-step coarse and gain tuning loop, fine-resolution, digitally controlled oscillator (DCO).

## I. Introduction

In submicron technology, digital radio frequency (RF) architecture will be adopted to reduce the cost, power consumption, and required area of the system. As the minimum feature size decreases, the supply voltage will also decrease. While an analog phase-locked loop (PLL) needs to be re-designed as the process is changed, a digital PLL can be easily translated into a new process. The digital PLL can be integrated into the digital RF transceiver. There are some issues in the digital PLL architecture. The digitally controlled oscillator (DCO) is one of the most critical blocks in the digital PLL. Conventionally, the frequency of the DCO is tuned with a varactor capacitance whose physical size is limited to several aFs. To overcome this limitation, a sigma-delta modulator is used to implement the fine capacitance [1]. Nevertheless there is still a limitation in the frequency resolution due to a physical limitation in the varactor size. In this case, the dithering bits of the sigma-delta modulator need to be increased in order to implement a finer resolution. Therefore, the area and power consumption also increases. In this paper, an active inductor is used for the frequency control, overcoming the minimum frequency resolution problem.

Typically, several LC-oscillators are used to cover the wide frequency band [2]. In this case, the area required and the power consumption can be a problem. So, several techniques are used to cover the wide frequency range with a single LC-oscillator. If the tuning range is wide, it comes at the cost of increased hardware and power consumption because the tuning range must be increased by using a capacitor array. The automatic coarse tuning scheme is typically used to widen the tuning range. The variation of the DCO gain,  $K_{DCO}$ , is large in wide range applications. The automatic calibration of the DCO

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gain is necessary to guarantee the same loop bandwidth for the phase noise and lock-time performances regardless of the channel frequency. This paper presents a wide-band fine-resolution DCO with an active inductor using an automatic three-step coarse and gain tuning loop.

## II. Wide-Band Fine-Resolution DCO Architecture

Figure 1(a) shows the block diagram of the proposed DCO with an active inductor. It is composed of the DCO core, a sigma-delta modulator, and a coarse tuning digital controller. A 3rd order MASH type sigma-delta modulator is used with five dithering bits (FDTW<4:0>). Figure 1(b) shows the structure of the sigma-delta modulator [1]. Generally, as the operation frequency of the sigma-delta modulator is increased, the noise shaping characteristic would be better. However, because the sigma-delta modulator is hard to design at high clock frequency, SDM\_CLK is determined to be 600 MHz, which can be simply generated through the divide-by-4 circuit. The delay of the critical path is minimized to guarantee the stable operation at 600 MHz.

Figure 2 shows the schematic of the DCO core. It consists of an active inductor, a passive inductor, a cap bank, and a negative-Gm. The active inductor is used for the wide-frequency range tuning and narrow-frequency range tuning control. The cap bank, which is composed of switches and MIM capacitors, provides the mid-frequency tuning range of the DCO. To meet the phase noise performance requirements,

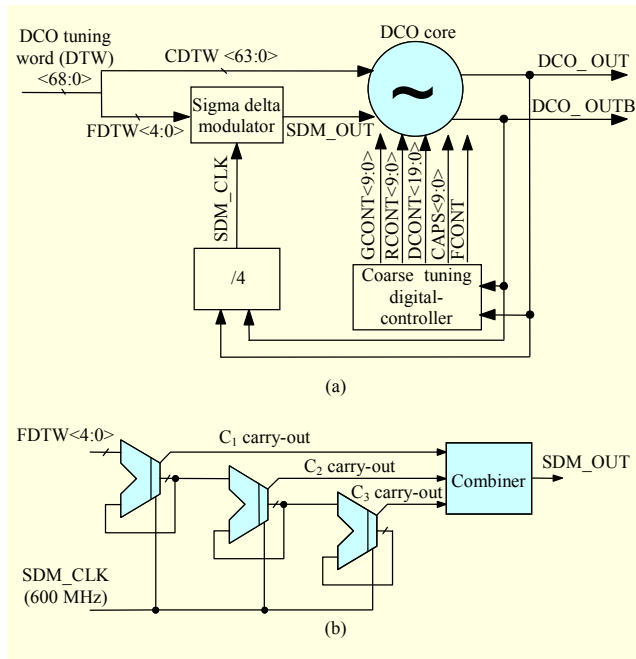


Fig. 1. (a) Block diagram of proposed DCO with active inductor and (b) structure of sigma-delta modulator.

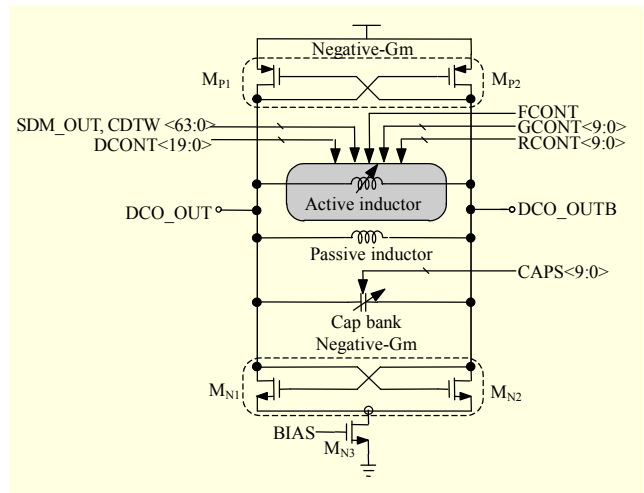


Fig. 2. Schematic of proposed DCO core.

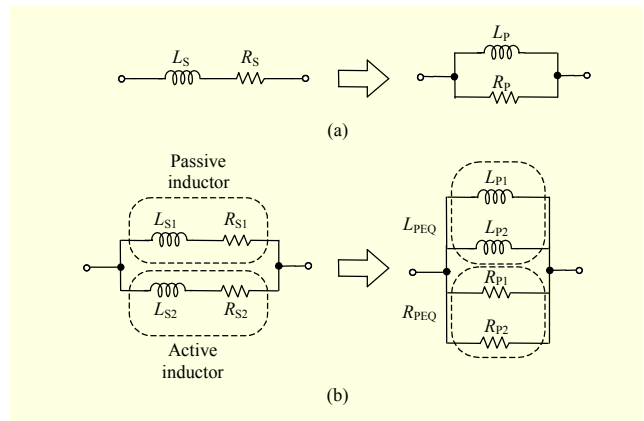


Fig. 3. (a) Transformation of series network to parallel network and (b) transformation of parallel two inductors to four parallel components.

a passive inductor is also used.

Figure 3(a) shows the transformation of the series network to a parallel network [3]. From the equivalence between two networks,  $R_p$  and  $L_p$  can be calculated as

$$R_p = L_S^2 \omega^2 / R_S, \quad (1)$$

$$L_p = L_S (1 + R_S^2 / L_S^2 \omega^2) \approx L_S, \quad (2)$$

where  $L_S$  and  $R_S$  are the series inductance and resistance, respectively. The quality factor of two networks is typically greater than 3, whose definition is presented in (3).

$$Q = L_S \omega / R_S = R_p / \omega L_p. \quad (3)$$

Figure 3(b) shows the transformation of two parallel inductors to four parallel components.

The equivalent resistance can be calculated from (1) by

$$\begin{aligned} R_{PEQ} &= R_{P1} R_{P2} / (R_{P1} + R_{P2}) \\ &= (\omega L_{S1} L_{S2})^2 / (L_{S1}^2 R_{S2} + L_{S2}^2 R_{S1}). \end{aligned} \quad (4)$$



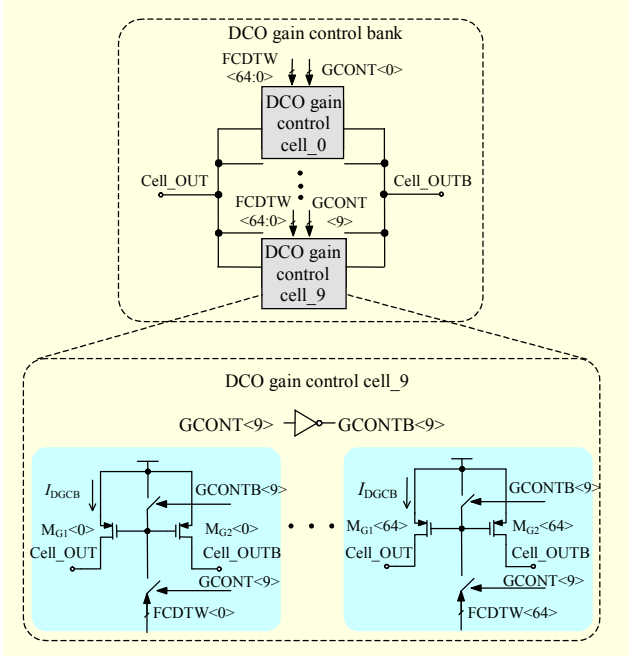


Fig. 5. Schematic of DCO gain control bank.

III. As mentioned above,  $G_{ds9}$ ,  $G_{ds11}$ , and  $G_{dsGCB}$  are also controlled by  $I_{D9}$ ,  $I_{D11}$ , and  $I_{DGCB}$ , respectively.  $I_D$  is dependent on the gate voltage and the size of the MOS (W/L). Thus, the method for the inductance tuning is to control the drain conductance  $G_{ds7}$ ,  $G_{ds9}$ ,  $G_{ds11}$ , and  $G_{dsGCB}$  except  $G_{ds5}$  by the gate voltage and the size of the MOS. The gate of  $M_5$  is connected to GND to prevent the gate node of  $M_1$  and  $M_3$  from floating and operate even when all the PMOS are turned off in the active inductor because the floating node is very sensitive to the digital noise.  $I_{D7}$ ,  $I_{D9}$ , and  $I_{D11}$  are controlled by the FCDTW<64:0>, FCONT, and DCONT<19:0> in the active inductor control bank, respectively.  $I_{DGCB}$  is controlled by the GCONT<19:0> in the DCO gain control bank.

Figure 5 shows the complete schematic of the gain control bank of the proposed DCO. It is composed of the ten DCO gain control cell arrays which are controlled by the signals from the GCONT<9:0>. When the GCONT<N> is high, the gate of the PMOS ( $M_1$ ,  $M_2$ ) is connected to the FCDTW<64:0>. However, if the GCONT<N> is low, the gate of PMOS ( $M_1$ ,  $M_2$ ) is connected to the VDD to disable the corresponding DCO gain control cell. The switches in the gain control cell are connected to the gate of the PMOS to reduce the degradation of the parasitic capacitance of the switches. The gain control bank is used to adjust  $K_{DCO}$  at the wide frequency tuning range. In order to compensate for the variation of  $K_{DCO}$ , the number of active DCO gain control cells is controlled by the automatic DCO gain tuning. Thus, the drain conductance ( $G_{dsGCB}$ ) is increased or decreased in the active inductor.

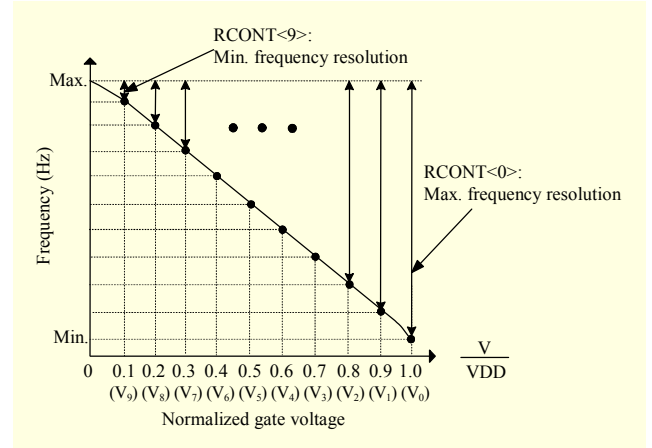


Fig. 6. Principle of adjusting frequency resolution.

Figure 6 shows the principle of adjusting frequency resolution. The CDTW<63:0> and SDM\_OUT are mapped to FCDTW<64:0> whose voltage levels are determined by RCONT<9:0> as shown in Fig. 4. The corresponding voltages are one of ten levels ( $V_0$  through  $V_9$ ) which are implemented with the resistor string ( $R_0$  through  $R_9$ ). The RCONT<9:0> are automatically controlled by the coarse tuning digital-controller in Fig. 1(a).

The adjustment of the voltage level corresponds to the fine frequency resolution of the DCO. For example, when the code value of RCONT<9:0> is “1000000000” and value of the SDM\_OUT is high, the SDM\_OUT is mapped to FCDTW<0> whose voltage level is  $V_9$ . It can be calculated as

$$V_9 = VDD \times \frac{R_9}{\sum_{i=0}^9 R_i} = VDD \times 0.1, \quad (10)$$

where all resistors ( $R_0$  through  $R_9$ ) has the same value, and  $VDD$  is the supply voltage. In this case, the FCDTW<0> has the minimum frequency resolution.

### III. Automatic Three-Step Coarse and DCO Gain Tuning Loop

The automatic three-step coarse and gain tuning procedure is as follows. Its principle is shown in Fig. 7.

**Step 1.** The 1st coarse tuning is the wide-frequency range tuning. The DCO frequency is measured through the coarse tuning digital-controller, as shown in Fig. 1(a). The optimum center frequency is selected by the FCONT adjusting the large inductance value of the active inductor. Thus,  $G_{ds9}$  is controlled by FCONT in this step, as shown in Fig. 4. The frequency tuning range of the 1st coarse tuning is 0.5 GHz. The active inductor tuning method is used in step 1 in order to reduce the area of the metal-insulator-metal (MIM) capacitor used in step 2. The

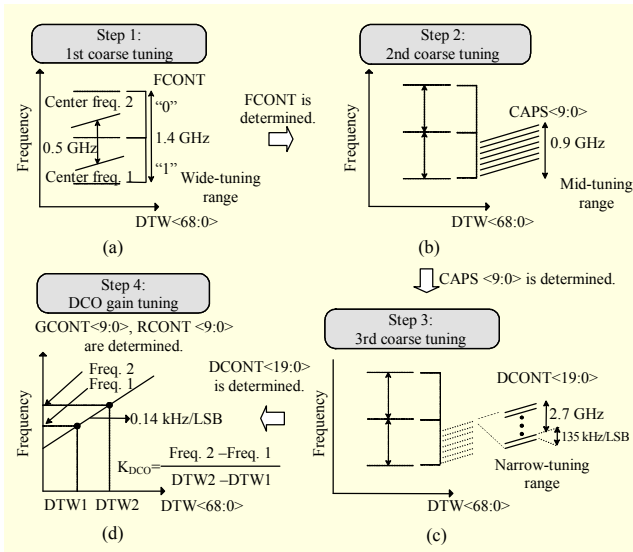


Fig. 7. Concept of proposed three-step coarse and gain tuning.

active inductor can cover the same frequency tuning range with smaller area than the MIM capacitor. If a very large MIM capacitor is used, it leads to reduction of the negative-Gm and voltage swing. Therefore, to alleviate the problem, an additional scheme is required to compensate for reduced negative-Gm, increasing the current consumption and necessitating a complicated frequency tuning method of DCO. In addition, it is better to perform the active inductor tuning in step 1 prior to the MIM capacitor tuning because the optimum active inductance value should be determined first for larger voltage swing and better phase-noise performance. The oscillation frequency of the DCO is determined by the product of overall inductance and capacitance, where the overall inductance is the parallel combination of active inductance and passive inductance. Since the quality factor of the DCO is dominated by the inductor and the quality factor of the overall inductor is determined by the active inductor, the optimum active inductor should be selected first, and MIM capacitance should be selected afterward.

**Step 2.** The 2nd coarse tuning is the mid-frequency range tuning. In this step, the MIM capacitances of the cap bank are controlled by CAPS<9:0>. The optimum MIM capacitances are selected through the 2nd coarse tuning process after the 1st coarse tuning is completed. The frequency tuning range of the 2nd coarse tuning is about 0.9 GHz.

**Step 3.** The 3rd coarse tuning is the narrow-frequency range tuning. Because the frequency step of the 2nd coarse tuning is several MHz and too coarse, additional fine-step tuning is required. At the 3rd coarse tuning step, DCONT<19:0> is determined to select the optimum frequency curve between the frequency curves at the 2nd coarse tuning step. In this step,  $G_{ds11}$  is controlled by DCONT<19:0> to adjust the inductance

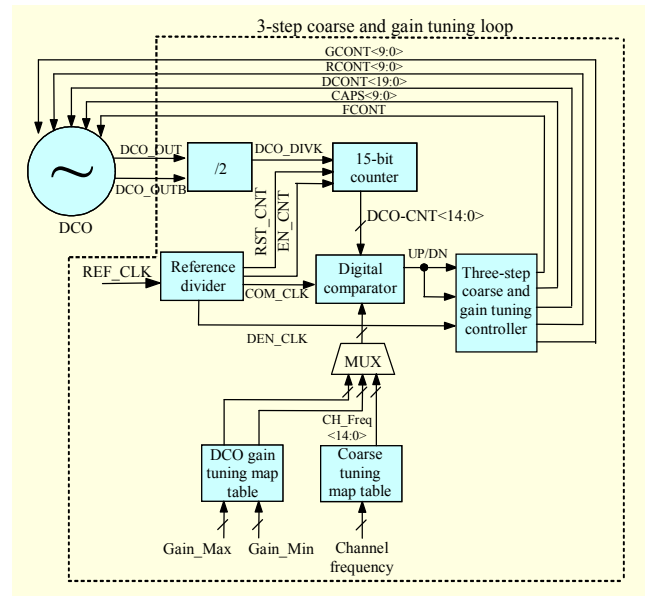


Fig. 8. Automatic three-step coarse and gain tuning loop of proposed DCO.

of the active inductor, as shown in Fig. 4. As a result, the frequency resolution of the 3rd coarse tuning is about 135 kHz/LSB.

**Step 4.** The DCO gain tuning begins when the three-step coarse tuning is completed. The  $K_{DCO}$ , which is defined as the frequency deviation of the DCO with respect to a 1-LSB change, is equal to the frequency resolution. Thus, the  $K_{DCO}$  is controlled by the value of the signal consisting of the RCONT<9:0> and the GCONT<9:0>, which adjust the frequency resolution. As shown in Fig. 6(d), the  $K_{DCO}$  can be estimated by dividing the difference of Freq. 2 and Freq. 1 by the difference of DTW2 and DTW1. It is measured and calculated through the coarse tuning digital-controller. Then, the RCONT<9:0> and the GCONT<9:0> are adjusted so the  $K_{DCO}$  can reach its reference boundary.

Figure 8 shows the automatic three-step coarse and gain tuning loop. Most of the blocks can be shared between the automatic three-step coarse and gain tuning loop. When the frequency tuning range of the DCO is wide range, the variation of the DCO gain,  $K_{DCO}$ , is very large depending on the frequency. Thus, the DCO gain control bank in Fig. 5 is required for the automatic DCO gain tuning loop. The  $K_{DCO}$  can be calculated with a 15-bit counter and digital blocks that can be shared with the three-step coarse tuning block. Therefore, no additional hardware is required for the automatic DCO gain tuning loop.

When the digital-PLL receives the channel information, the coarse tuning reference table converts the channel information to the appropriate timing parameter for the three-step coarse tuning. The coarse tuning digital-controller works with the

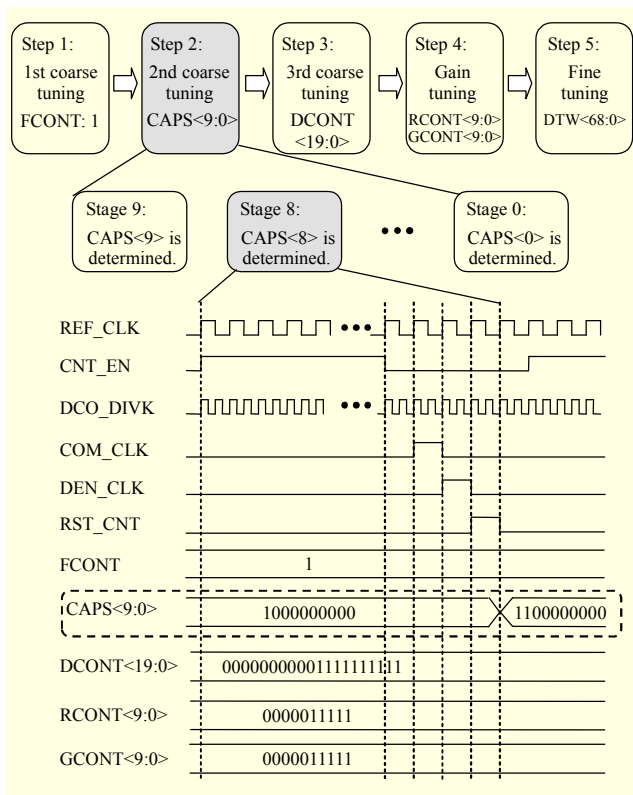


Fig. 9. Timing diagram of 2nd coarse tuning loop.

reference clock signal (REF\_CLK) to generate RST\_CNT, CNT\_EN, DEN\_CLK, and COM\_CLK signals. Since the coarse tuning process involves frequency tracking, the 15-bit counter is used to estimate the period of the DCO. This result, DCO\_CNT<14:0>, is compared with the channel reference number, CH\_Freq<14:0>, generated from the coarse tuning reference table based on the channel frequency. The frequency of DCO is detected through the 15-bit counter and is compared with the reference value. In each step, coarse and gain tuning control signals (FCONT, CAPS<9:0>, DCONT<19:0>, RCONT<9:0>, and GCONT<9:0>) are determined digitally based on the comparison result. After the three-step coarse and gain tuning, the DTW<68:0> is adjusted to finely tune the phase and frequency of the DCO at the fine tuning stage.

Figure 9 shows the timing diagram of the 2nd coarse tuning loop when FCONT is determined as “1” after the 1st coarse tuning. The 15-bit counter is periodically reset by the RST\_CNT. This counting operation is masked by the CNT\_EN signal. The 15-bit counter is enabled only when the CNT\_EN is high. When the output of the counter is smaller than the channel reference number, CH\_Freq<14:0>, the UP signal asserted at the rising edge of COM\_CLK so as to make the frequency of the DCO higher. The UP/DOWN signals are used to decide the coarse and gain tuning control signals in the

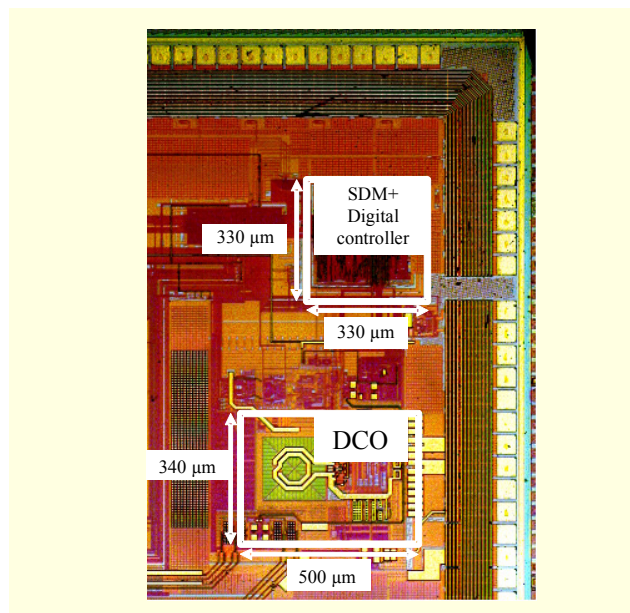


Fig. 10. Chip microphotograph.

each tuning controller.

In Fig. 9, we assume that the counting value (DCO\_CNT<14:0>) is less than the desired channel frequency (CH\_Freq<14:0>) when the code value of CAPS<9:0> is “1000000000”. The code value of CAPS<9:0> is determined as “1” in stage 9 of the 2nd coarse tuning and the code value of CAPS<8> is determined as “1” in stage 8 of the 2nd coarse tuning. The code value of CAPS<9:0> is changed from “1000000000” to “1100000000” at the falling edge of RST\_CNT signal. The CAPS<9:0> is selected through the 2nd coarse tuning process by fixing the code values of other signals (FCONT, DCONT<19:0>, RCONT<9:0>, and GCONT<9:0>). After ten cycles of the 2nd coarse tuning, the 3rd coarse tuning is started. The coarse and gain tuning signals are determined through the four steps before the fine tuning.

#### IV. Experimental Results

This chip was fabricated using the CMOS process with 0.13 μm technology, a single poly layer, six layers of metal, the option of MIM capacitors, and high sheet resistance poly resistors. The chip microphotograph is shown in Fig. 10. The total area of the DCO core, sigma-delta modulator, and coarse tuning digital-controller is 0.28 mm<sup>2</sup>.

Figure 11 shows the measured tuning curve of the DCO after the three-step coarse and gain tuning. The frequency tuning range that can be achieved with the planar passive inductor and capacitance tuning is 0.9 GHz. As a three-step coarse tuning scheme is used, the tuning range can be widened by 0.5 GHz

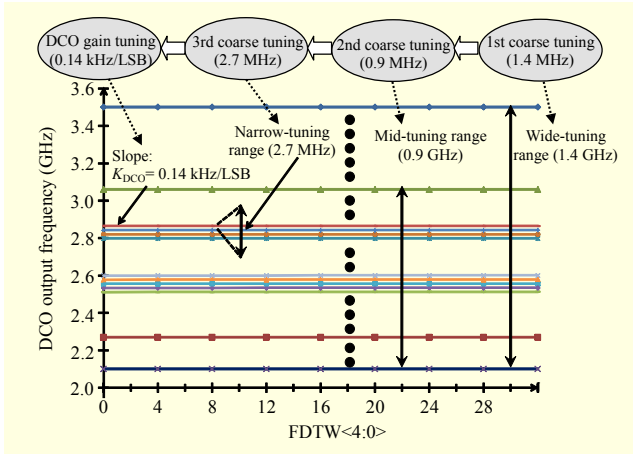


Fig. 11. Measured tuning curve of DCO after three-step coarse and gain tuning.

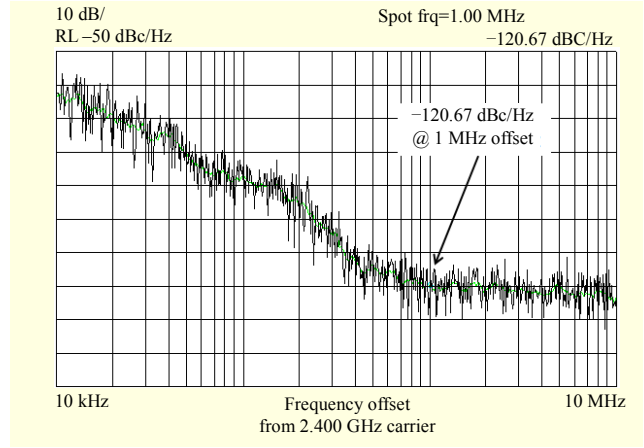


Fig. 13. Measured phase noise of DCO.

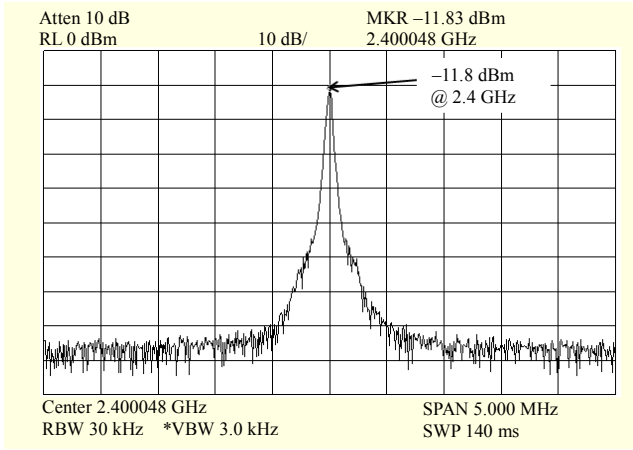


Fig. 12. Output spectrum of DCO.

under the same capacitance value. This has the effect of widening the tuning range without using extra capacitance.

The frequency resolution for the 1-LSB of the CDTW<63:0> is 4.6 kHz. Thus, the effective time-averaged frequency resolution done by the 5-bit SDM can be calculated as

$$\Delta f^{\Delta\Sigma} = 4.6 \text{ kHz} / 2^5 = 0.14 \text{ kHz}. \quad (11)$$

From (11), the  $K_{DCO}$  is about 0.14 kHz/LSB because the frequency resolution for the 1-LSB of the DTW<68:0> is 0.14 kHz.

Figure 12 shows the output spectrum of the DCO when the three-step coarse and gain tuning is enabled. The output power level of the DCO is  $-11.8$  dBm at 2.4 GHz. The phase noise of a free-running DCO output at 2.4 GHz is  $-120.67$  dBc/Hz at 1 MHz offset as shown in Fig. 13.

When the output frequencies are 2.1 GHz and 3.5 GHz, the phase noise at 1 MHz offset are  $-121.2$  dBc/Hz and  $-116.1$  dBc/Hz, respectively. The figure of merit with the frequency

Table 1. Summary of measured performance.

	[1]	[5]	[6]	This work
Process	0.13 $\mu\text{m}$ CMOS	0.18 $\mu\text{m}$ CMOS	65 nm CMOS	0.13 $\mu\text{m}$ CMOS
Supply voltage (V)	1.5	1.8	1.1	1.2
Power consumption (mW)	3.45	5	3.3	6.6
Center frequency (GHz)	2.4	3.8	10	2.4
Tuning range (%)	20.8	26.3	10	58
Frequency resolution without SDM (kHz)	23	20	1,030	4.6
Phase noise @ 1 MHz (dBc/Hz)	-117.0	-123 @ 1.2 MHz	-102	-120.67
FOM <sub>T</sub> (dBc/Hz)	-185.6	-194.4	-176.8	-195.3
Area (mm <sup>2</sup> )	0.54	N/A	0.02	0.28

tuning range (FOM<sub>T</sub>) for the DCO can be calculated using

$$FOM_T = PN(f_{\text{offset}}) - 20 \log \left( \frac{f_0}{f_{\text{offset}}} \right) + 10 \log \left( \frac{P_{DC}}{1 \text{ mW}} \right) - 20 \log \left( \frac{FDR}{10} \right), \quad (12)$$

where  $f_{\text{offset}}$  is the offset frequency,  $f_0$  is the oscillation frequency,  $PN(f_{\text{offset}})$  is the phase noise found in the  $f_{\text{offset}}$ ,  $P_{DC}$  is the DC power consumption, and the  $FDR$  is the frequency tuning range in a percentage. The performance of the proposed DCO is summarized in Table 1. The performance of the proposed DCO is summarized in Table 1. The phase noise performance of this work is better than that of [5], and the frequency resolution of the DCO is the smallest of all. In addition, the tuning range of the proposed DCO is the widest and FOM<sub>T</sub> of this work is the best among the references.

## V. Conclusion

This paper presents a wide-band fine-resolution digitally controlled oscillator (DCO) with an active inductor using an automatic three-step coarse and gain tuning loop. To control the frequency of the DCO, the transconductance of the active inductor is tuned digitally. To cover the wide tuning range, a three-step coarse tuning loop is used. At the same time, the DCO gain needs to be calibrated digitally to compensate for the gain variations. The tuning range of the DCO is 2.1 GHz to 3.5 GHz with the effective frequency resolution of 0.14 kHz. The power consumption is 6.6 mW from a 1.2 V supply. The phase noise of the DCO output at 2.4 GHz is to  $-120.67$  dBc/Hz at 1 MHz offset.

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