# A Twin Symbol Encoding Technique Based on Run-Length for Efficient Test Data Compression

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*Recent test data compression techniques raise concerns regarding power dissipation and compression efficiency. This letter proposes a new test data compression scheme, twin symbol encoding, that supports block division skills that can reduce hardware overhead. Our experimental results show that the proposed technique achieves both a high compression ratio and low-power dissipation. Therefore, the proposed scheme is an attractive solution for efficient test data compression.*

*Keywords: Test data compression, low-power dissipation.*

## I. Introduction

In order to test a chip, test data is sent from automatic test equipment to a target chip. The transmission time for the test data, which is a determining factor in the total test application time, is one of the main issues addressed in time-to-market research. Currently available tests require large amounts of test data because system-on-a-chip complexity is constantly increasing, and therefore the data compression methods that are employed are becoming increasingly important. Higher compression ratios translate to shorter chip testing times so that more chips can be tested within a fixed time period.

Many compression schemes and techniques have already been proposed. The data compression ratio is an important factor, and recently, two additional key factors, low hardware cost [1], [2] and power dissipation [3], have become areas of concern. An effective compression technique needs to satisfy the requirements for all three of these key factors.

There are three main categories: code-based schemes, linear decompressors, and broadcast scans. Linear decompressors and broadcast scans require simple and small decompressors, but they have low flexibility on X-filling [4]. On the other hand, the code-based schemes have the high flexibility in X-filling, so the characteristic of transitions in test vector can be set with optimum condition for low-power dissipation.

Golumb [5] and frequency-directed run-length [6], two representative code-based schemes, encode the run-lengths of blocks which end at the occurrence of a 1. To increase the compression ratio, many schemes have been developed, such as statistical skills like statistical coding [7], variable input Huffman coding (VIHC) [8], and run-length Huffman (RL-Huffman) [9]. Both VIHC and RL-Huffman, which are high-performance compression schemes based on run-length, have excellent compression ratios using statistical coding techniques. Both provide an optional function that limits the maximum block length when small hardware overhead is required. VIHC achieves reasonable compression ratios even though limiting the maximum block length negatively affects its compression ratios. VIHC, however, does nothing to ensure low-power dissipation. On the other hand, RL-Huffman guarantees low-power dissipation in the scan cells and achieves equal or better compression ratios than VIHC does when there is no maximum block length. When the maximum block length is limited, however, RL-Huffman results in a much lower compression ratio than VIHC does. A shorter block length limit further degrades the compression ratio.

This letter proposes a test data compression scheme, twin symbol encoding (TSE), with a new symbol definition, which satisfies all three key factor requirements. The experimental results show that the proposed scheme achieved high compression ratios, low-power dissipation, and low hardware costs.

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## II. Motivation

To lower power dissipation in scan cells, the "don't care" bits in test vectors can be filled with a minimum weighted-transition (WT) value. RL-Huffman encoding is an efficient compression technique with adjacent X-filling and the smallest WT value. Its compression ratio is quite high and is at least as good as that of VIHC. However, performance suffers when the block length is limited to reduce the hardware overhead. The cause of this rapid degeneration comes from the symbol 0 in the RL-Huffman definition. Whenever a block longer than the maximum block length is divided into several blocks, the symbol 0 is required for each division. This causes an inefficient increase in the number of symbols. Since every symbol should be encoded, it negatively affects the compression ratio.

## III. TSE Technique Description

TSE uses adjacent X-filling and defines a new symbol as part of its implementation. Table 1 shows how TSE divides blocks when $m$ is determined as the maximum block length. TSE and RL-Huffman have the same number of symbols for definition $m$+1. In RL-Huffman, the symbol 0, which is located between the divided blocks, represents the case in which the data of the next divided block is not inverted. On the other hand, TSE introduces a twin of the symbol $m$ denoted by the symbol $m'$. This twin holds the data of the next block, while the symbol $m$ toggles the data. Table 2 shows the symbol definitions when the maximum block length is set to four. For example, a 12-bit length block should be divided into three symbol 4s and two symbol 0s. For the TSE case, it is divided into two 4′ symbols and one symbol 4. TSE always requires a smaller number of symbols than RL-Huffman does whenever block dividing is requested in order to meet maximum block length requirements. Figure 1 is another example of the symbol definitions using a partial test vector. Twelve symbols are required for RL-Huffman, while only nine symbols are needed for TSE. This effectiveness leads to an improvement in the compression ratios. Figure 2 shows the TSE decoder, which is almost the same as the RL-Huffman decoder. The only minor difference is the very small part in the FSM which controls the one-bit data line designated by an arrow. The number of states in FSM of the proposed scheme for any different configurations is limited to $m$+1, and it is identical to that of RL-Huffman since the proposed scheme doesn't change the number of symbols. Therefore, the hardware overhead is almost the same between the RL-Huffman and TSE decoders.

Table 1. Symbol definitions for proposed scheme.

| Symbol | Definition | |
|---|---|---|
| | Current data | Next data |
| 1 | 0/1 * 1 | Toggle |
| 2 | 0/1 * 2 | Toggle |
| ⋮ | ⋮ | ⋮ |
| $m$–1 | 0/1*($m$–1) | Toggle |
| $m$ | 0/1 * $m$ | Toggle |
| $m$' | 0/1 * $m$ | Hold |

Table 2. Symbols of four-block length.

| RL-Huffman [9] | | | TSE | | |
|---|---|---|---|---|---|
| Symbol | Definition | | Symbol | Definition | |
| | Data | Next data | | Data | Next data |
| 0 | None | Toggle | 1 | 0/1 | Toggle |
| 1 | 0/1 | Toggle | 2 | 00/11 | Toggle |
| 2 | 00/11 | Toggle | 3 | 000/111 | Toggle |
| 3 | 000/111 | Toggle | 4 | 0000/1111 | Toggle |
| 4 | 0000/1111 | Toggle | 4' | 0000/1111 | Hold |

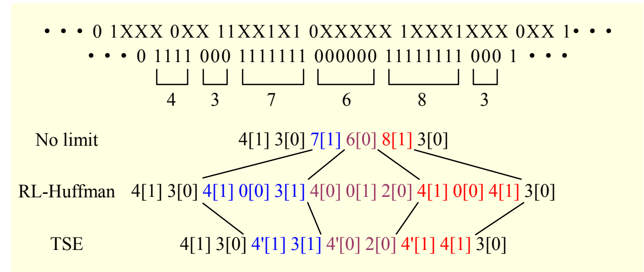


Fig. 1. Example of four-block length.

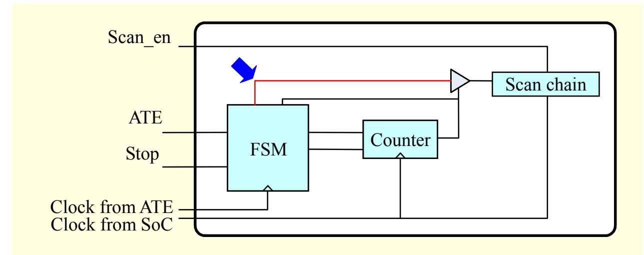


Fig. 2. Structure of proposed decoder.

## IV. Experimental Results

All experimental results for IWLS 2005 benchmarks are obtained using the same test data set generated by TetraMax [10], a well-known ATPG tool. The target circuits are classified

by two groups: ISCAS`89 benchmarks and opencores. Opencores are much larger than ISCAS`89. Table 3 illustrates that TSE significantly reduces the number of symbols required for testing. It is obvious that TSE is efficient for larger maximum block length but even more efficient for shorter maximum block length (see Fig. 3). Distinctively, the improvement ratios of vga_lcd do not show big differences because almost all bits are "don't care" bits in the test data of vga_lcd.

Table 3. Number of symbols.

| Circuit | RL-Huffman [9] | | | TSE | | |
|---|---|---|---|---|---|---|
| | 8 | 16 | 32 | 8 | 16 | 32 |
| s5378 | 6,161 | 4,119 | 3,141 | 4,388 | 3,367 | 2,878 |
| s9234 | 8,083 | 5,253 | 4,207 | 5,949 | 4,534 | 4,011 |
| s13207 | 19,322 | 11,054 | 7,374 | 12,092 | 7,958 | 6,118 |
| s15850 | 15,138 | 9,336 | 6,956 | 10,406 | 7,505 | 6,315 |
| s35932 | 16,583 | 12,101 | 9,995 | 12,474 | 10,233 | 9,180 |
| s38417 | 17,3387 | 9,2293 | 52,809 | 94,955 | 5,4408 | 34,666 |
| s38584 | 55,302 | 31,528 | 22,430 | 34,723 | 24,336 | 19,787 |
| tv80 | 50,419 | 28,467 | 17,467 | 30,167 | 19,191 | 13,691 |
| usb_funct | 172,087 | 92,619 | 53,679 | 95,091 | 55,357 | 35,887 |
| aes_core | 45,252 | 32,690 | 26,694 | 33,264 | 26,983 | 23,985 |
| def_perf | 282,554 | 198,756 | 160,798 | 203,833 | 161,934 | 142,955 |
| vga_lcd | 20,746k | 10,399k | 5,227k | 10,406k | 5,233k | 2,647k |

Three compression techniques, RL-Huffman, VIHC, and the proposed TSE scheme are compared in Table 4. There was a significant improvement in the compression ratio between RL-Huffman and TSE. TSE showed even greater improvement as the maximum block length decreased. RL-Huffman requires numerous symbol 0s for small block length limits since more blocks must be divided. However, TSE does not require

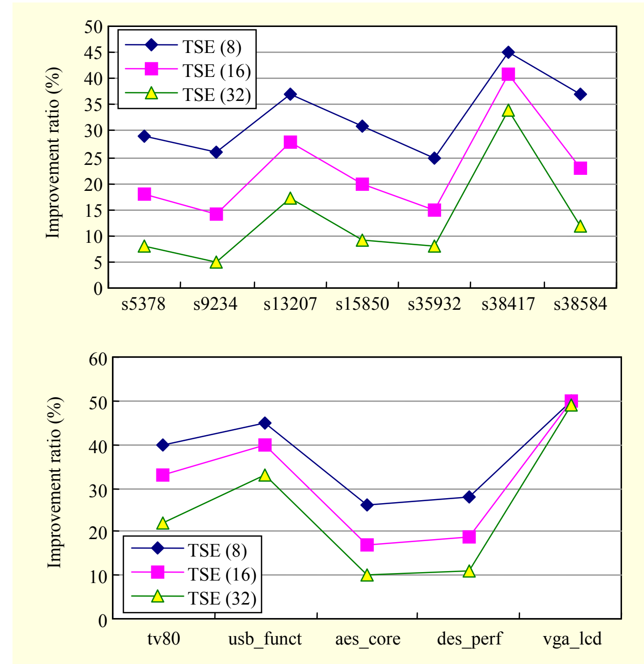


Fig. 3. Improvement ratio relative to Table 3.

Table 4. Comparison of compression ratios among compression skills.

| Circuit | VIHC [8] | | | RL-Huffman [9] | | | TSE | | |
|---|---|---|---|---|---|---|---|---|---|
| | Maximum block length | | | | | | | | |
| | 8 | 16 | 32 | 8 | 16 | 32 | 8 | 16 | 32 |
| s5378 | 44.77 | 49.13 | 51.94 | 24.48 | 39.12 | 48.09 | 47.19 | 51.36 | 53.60 |
| s9234 | 41.18 | 41.86 | 42.43 | 25.46 | 36.57 | 42.79 | 43.64 | 45.10 | 46.17 |
| s13207 | 66.26 | 67.48 | 68.77 | 42.01 | 54.06 | 60.60 | 65.08 | 65.58 | 67.13 |
| s15850 | 54.28 | 54.99 | 56.14 | 31.05 | 43.01 | 49.85 | 53.29 | 54.15 | 55.18 |
| s35932 | 35.10 | 41.99 | 46.01 | 18.19 | 32.46 | 42.10 | 41.08 | 46.19 | 49.39 |
| s38417 | 75.95 | 80.08 | 81.91 | 54.50 | 70.45 | 78.01 | 79.31 | 83.78 | 85.70 |
| s38584 | 58.43 | 59.28 | 60.46 | 34.56 | 47.19 | 54.04 | 57.93 | 58.55 | 59.70 |
| tv80 | 69.79 | 72.49 | 73.78 | 45.28 | 58.71 | 67.10 | 70.10 | 72.68 | 73.84 |
| usb_funct | 77.97 | 82.43 | 84.39 | 53.50 | 69.56 | 77.24 | 78.66 | 83.25 | 85.18 |
| aes_core | 40.48 | 45.96 | 50.63 | 20.13 | 34.46 | 45.29 | 43.94 | 49.90 | 53.90 |
| des_perf | 40.23 | 47.17 | 52.54 | 22.40 | 36.39 | 47.16 | 46.27 | 51.68 | 55.86 |
| vga_lcd | 87.16 | 93.35 | 96.43 | 62.24 | 80.90 | 90.23 | 87.23 | 93.44 | 96.53 |

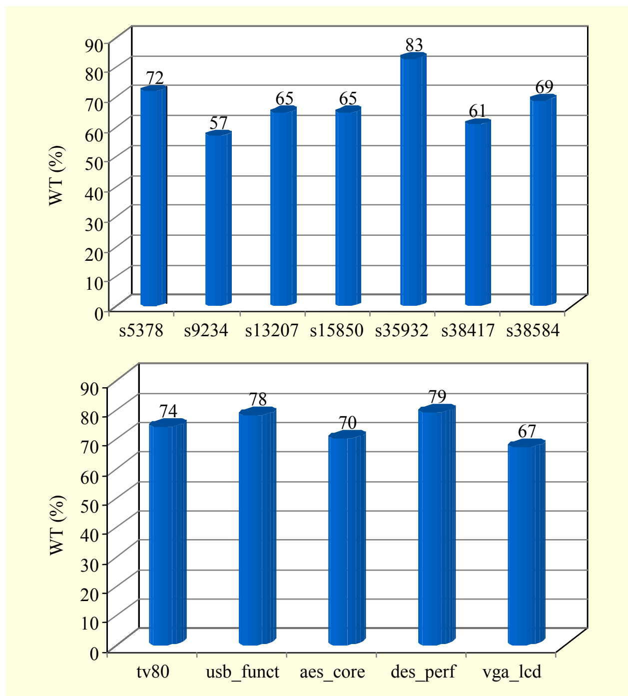


Fig. 4. WT ratio of TSE over that of VIHC.

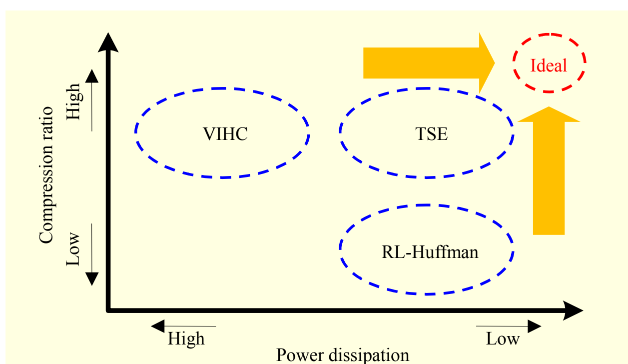


Fig. 5. Comparison chart of three schemes reviewed in this work.

additional symbols for block divisions. This difference causes the compression ratio gap between the two schemes. TSE and VIHC have almost the same compression ratio, similar to when there was no limit on the block length. However, TSE has a low-power dissipation characteristic, and the values in Fig. 4 indicate the superior power dissipation of the proposed scheme over that of VIHC. This is a significant advantage in building and operating scan cells. Furthermore, TSE shows much better compression performance as the target circuits become larger. This trend on the experimental results has good prospects in the current situation where the size of circuits is getting bigger. Overall, Fig. 5 shows that TSE is the superior choice for use as a data compression technique. TSE can be applied to both multiple scan chain and single scan chain environments. For both environments, TSE can provide an excellent compression ratio, hardware flexibility, and power dissipation compared to other compression schemes. Additionally, power dissipation can be drastically decreased in multiple scan chains due to shorter scan length.

## V. Conclusion

TSE supports the block length limitation technique for reducing hardware costs, and it shows high compression ratios, regardless of whether or not there are limits on block length. Furthermore, low-power dissipation in scan cells is guaranteed due to adjacent X-filling. In conclusion, TSE is an efficient compression technique since it satisfies the three key factor requirements. TSE becomes even more promising as the importance of low-power dissipation increases.

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