Measurement and Explanation of DC/RF Power Loci of an Active Patch Antenna

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A case study of an active transmitting patch antenna revealed a characteristic loop locus of DC power versus RF output power as drive frequency was varied, with an operational bandwidth substantially smaller than the impedance bandwidth of the radiator. An approximate simulation technique, based on separation of the output capacitance of the power transistor, yielded easily visualized plots of power dependence on internal load impedance, and a simple interpretation of the experimental results in terms of a near-resonance condition between the output capacitance and output packaging inductance.

Keywords: Patch antenna, active antenna, DC/RF power loci, power amplifiers, power added efficiency, RF transistor modeling.

I. Introduction

Over the past decade, there has been a revival of interest in high efficiency radio frequency (RF) power amplifiers [1]-[3]. Schemes based on careful control of harmonic impedance terminations have been one of the major avenues explored. There has also been new interest in active antennas, defined as arrangements, where an active device is connected directly to a radiating element with little or no intervening circuitry.

In the context of active antennas for transmission, the high-efficiency amplifier techniques present new problems. One major challenge is to create an antenna that presents the desired impedance to the active device at harmonics of the operating frequency as well as the fundamental signal. Where the active antenna uses a microstrip patch radiator, the problem is to design the patch shape to achieve the required impedance function, and this is a much more constrained process than traditional network synthesis.

Other researchers [4], [5] investigated an active antenna comprising a field effect transistor (FET) power device connected to a rectangular microstrip patch radiator. They reported an increase in power-added efficiency from using a set of shorting pins at the center line of the patch. This suppressed the TM_{20} resonance and ensured low terminal impedance at the second harmonic.

The present authors attempted to reproduce this experimental result [6], [7] and to consider other ways of controlling the harmonic impedances. In the course of this experimental investigation, a characteristic loop behavior was observed in the DC input power/RF output power plane as the frequency was swept at a constant input drive level. Before considering more subtle effects of harmonic impedance, it was considered desirable to obtain a clear qualitative understanding of the

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dominant physical effects producing this loop. This preliminary investigation is now described.

II. RF Power/DC Power Loop Loci

The experimental setup was similar to that described in [5]. Using the same transistor and with the rectangular patch radiator tuned to nearly the same center frequency. The drain of the transistor, an MLE351 medium power MESFET from Fujitsu, was connected to the patch through a microstrip line designed to be one wavelength long at a center frequency of 2.35 GHz. This is a longer line section than was used in [5] and was included to facilitate measurements of the patch impedance. It was also used in current and voltage waveform measurements, as described elsewhere [7]. The test board included single stub input matching for the gate drive, with no attempt to optimize gate input matching for the harmonics. The DC bias was almost at pinch off, with a quiescent drain current of only 10 mA, so that Class B operation was expected as in [5]; the same drain bias of 6 V was also used.

A basic observation was made. Working with a constant input drive level to the active antenna and constant DC bias on gate and drain, an upward sweep of frequency would produce a characteristically shaped loop traced counterclockwise in the DC power (*x*-axis) versus RF load power (*y*-axis) plane (see Figs. 2 and 3). As the frequency was swept upwards from a value close to the patch resonance frequency, at which current and power were low, the indicated point passed in turn through points of maximum DC current or power, maximum RF power, maximum drain efficiency, and finally, minimum current. Along the top section of the loop, the DC current and RF output fell rapidly with frequency while the drain efficiency in this section varied relatively weakly.

This pattern occurred for all patch loads that were tried, (see Fig. 1), regardless of their precise configuration. Figure 2 shows some typical loops measured with a plain rectangular patch, the various operating parameters being indicated in the figure. As the input power to the active antenna was reduced, a smaller loop was produced, but its shape remained similar.

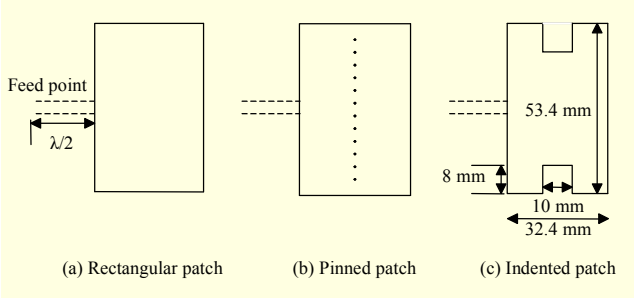


Fig. 1. Schematics of antennas used.

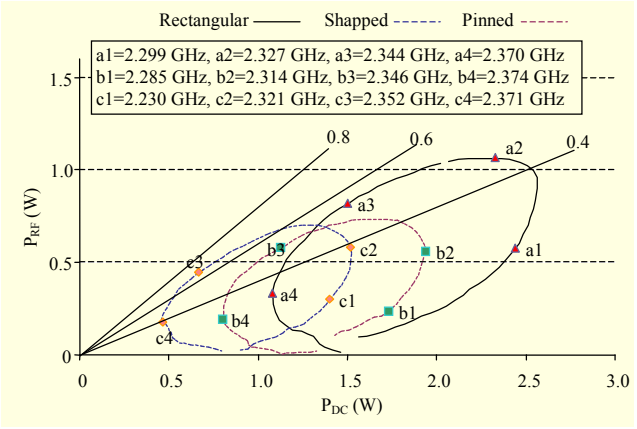


Fig. 2. DC power/RF power loops for rectangular patch, generated by sweeping frequency. Each locus corresponds to a certain power level.

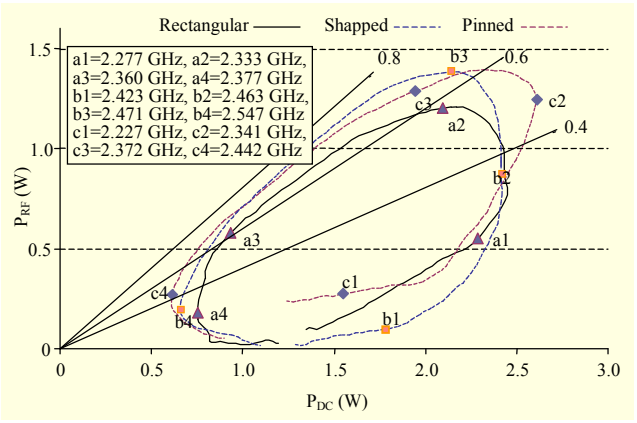


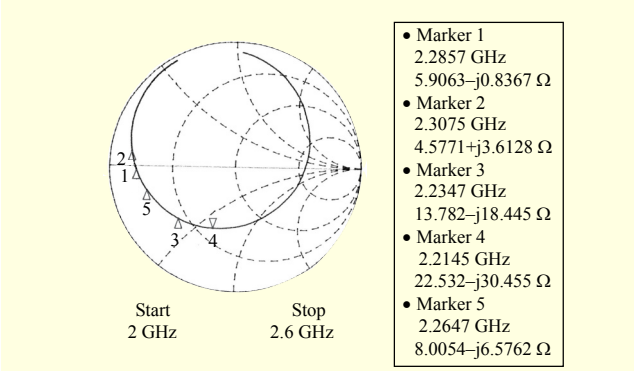
Fig. 3. DC power/RF power loops generated by sweeping frequency at fixed drive level for different patch types.

Other examples in Fig. 3 show that the gross behavior is similar for different patch types.

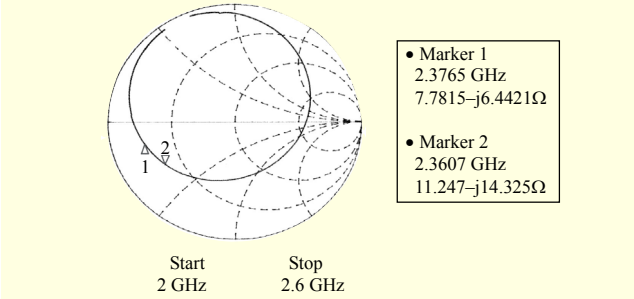
III. Investigation of Loop Loci by Simulation

The observed loop behavior is obviously very different from that expected of the simple model of a transistor whose drain, above a knee voltage, behaves roughly as a gate-controlled constant current source. Simulation tools, combined with circuit models of the device, were found to be a powerful way to elucidate such effects, where the object is physical understanding rather than high quantitative accuracy.

The active antenna was simulated using the advanced design system (ADS) simulator, with the physical layout of the test board entered as accurately as possible into the simulation layout and the patch load described as a data file of measured impedance versus frequency. The impedance was measured by soldering a shape-memory alloy connector to the output microstrip line at its mid-point, with the line section between



(a) Impedance locus of rectangular patch



(b) Impedance locus for shaped patch

Fig. 4. Impedance locus before and after indentation.

this point and the transistor drain temporarily disconnected. As all measurements were taken over a fairly small percentage bandwidth, it was reasonable to assume that the impedances at the measuring point, the patch itself, and the transistor drain were effectively the same.

Figure 4 shows the measured impedance loci of two of the patches used. The dimensions of the rectangular patch are similar to those in [5]. The important section of this plot is the frequency range between markers 2 and 4, over which most of the loop locus is generated. The various antennas were adjusted to have almost identical impedance versus frequency in this range, so that performance differences caused by different harmonic impedances would be observable. As the object here is to explain the basic loop locus structure, which was very similar for all the patch types, we shall not discuss the harmonic effects here. Figure 4(b) confirms the similarity of the fundamental impedance locus of the indented patch, and very similar plots were obtained for pinned and sector-shaped patches.

The simulation was able to predict the approximate shape of the observed loop, but this does not in itself clarify the main mechanisms involved. Certain effects were shown to be fairly insignificant by initial simplifications of the simulation model. Driving the external gate terminal from a simple 50 Ω source (by removal of the input matching circuit), or from a constant

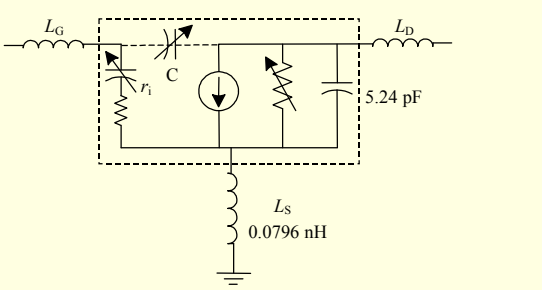


Fig. 5. Simulation model for MLE3.

voltage source, did not markedly change the loop structure. These tests suggested that feedback effects, whether at the fundamental signal or its harmonics, were not a major factor in the operation of the circuit. Simulations with harmonic load impedances set to zero also predicted little change in the loop shape, and this was consistent with the experimental observation that different patch types with similar fundamental impedances produced similar loci. Attention was turned to the modeling of the transistor and its packaging on its drain side.

Figure 5 shows the equivalent circuit used to model the MLE351 transistor in the ADS simulation package. The intrinsic transistor contained within the packaging model can easily be seen. The connections to the intrinsic gate and drain are modeled as transmission line sections. Since these are electrically short, even at the third harmonic, they can also be approximated as inductors shunted by small capacitors, and the latter can be absorbed into the intrinsic device's input and output capacitances. The source packaging inductance introduces some additional feedback between the input and output ports but it has a small value.

In the simulation it was possible to remove all the packaging parasitics and leave only the intrinsic device. This could not easily be done physically, but it made it possible to see how a much more ideal device would behave in the circuit.

The ADS simulator permits the packaging components shown as L_S, L_D, and L_G in Fig. 5 to be simply disconnected, effectively reducing the device to an intrinsic or unpackaged transistor. Nevertheless, a significant element in the model is the shunt capacitor C_{DS}, which is still present in the intrinsic device. The software does not provide any direct means of removing this component from the model, but it does permit insertion of capacitors of negative value. To reveal the simplest possible model, a capacitor of nearly equal negative value was connected between drain and ground. Although the capacitor in the transistor model is slightly nonlinear, a sufficiently accurate mean linear equivalent could be found. This exercise further simplifies the intrinsic transistor to a nearly ideal one, providing a very simple starting point for explaining the load impedance effects. The intrinsic (de-packaged) transistor which has

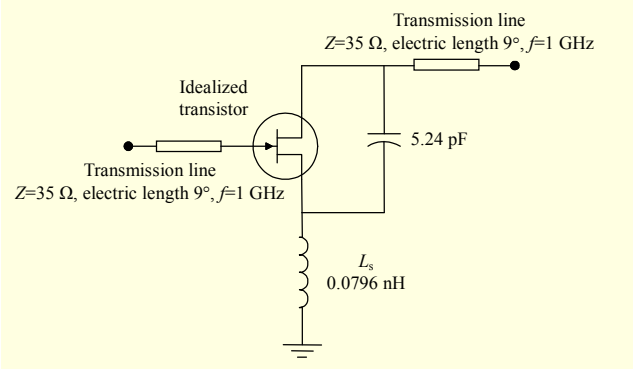


Fig. 6. Simulation model using idealized transistor.

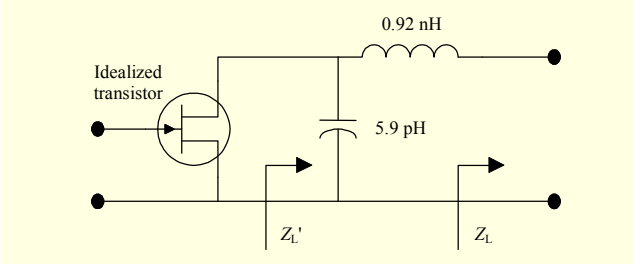


Fig. 7. Simplified simulation model.

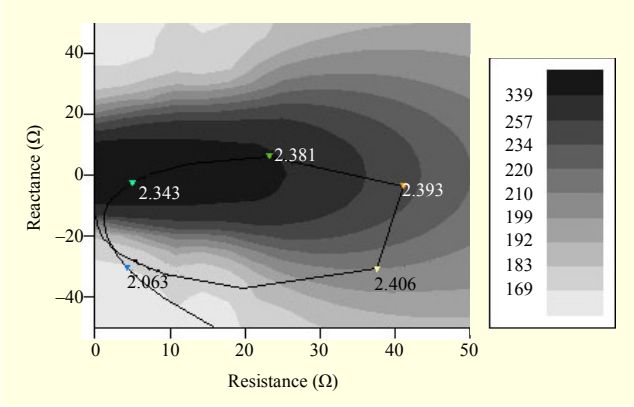


Fig. 8. Simulated values of DC supply current (mA) versus fundamental load impedance, for idealized transistor. (Harmonic impedances are zero. Incident drive power is constant at 26 dBm.)

additionally had its output capacitance removed is referred to here as "idealized" (Fig. 6). It is also possible to connect positive and negative capacitors of equal magnitude in shunt across the intrinsic device.

This leaves its electrical properties unchanged but makes it possible to insert a simulated ammeter between the capacitors, and this then reads the current in the idealized device. It should be noted that, because of the dispersion effect in gallium arsenide field effect transistors (GaAsFETs), the idealized device model must be viewed as quasi-static. This means that its characteristics differ significantly from the static ones, and it is valid above the very low turnover frequency of the dispersion effect. However, with the exception of its small drain-gate capacitance, it may be viewed as a memoryless system at the operating frequencies.

Note that the packaging introduces some feedback via the source lead inductance, whose reactance X_{source} is about 1.2 Ω at the design frequency. In ideal Class B, a peak-to-peak gate swing V produces a fundamental component of drain current with a peak-to-peak amplitude of only ½ g_m V. Therefore, the feedback effect modifies the effective gate drive by a factor of about $1/(1 + ½ \text{ j } g_m X_{source})$. This has a modulus of 0.96 when calculated using the static g_m of the device, approximately 500 mS. Since the GaAsFET dispersion would reduce the effective g_m appreciably, it is, therefore, expected that the source feedback will not have a major effect on the power output at a given input drive level.

Neglecting the source inductance, the transistor model reduces to the idealized transistor cascaded at its output with the shunt capacitor C_{DS} and then with a short section of transmission line of 35 Ω characteristic impedance. As this has an electrical length of only 9° at 1 GHz, it is a fair approximation to take it as electrically short, even at 2.3 GHz, and to approximate it as a series inductor, at least at the fundamental frequency. At 2.35 GHz, it has a 13.5 Ω equivalent reactance and 0.92 nH inductance. Figure 7 shows this very simple model, with the transmission line capacitance absorbed in the increased C_{DS}. Z_L now denotes the actual load impedance and Z_L' the value presented to the idealized transistor. Ignoring the feedback inductance, we can now describe the power and efficiency dependencies equivalently in the Z_L and Z_L' planes using the simple bilinear relationship between these impedances to visualize how the external dependencies arise from the internal ones. The lossless nature of the transformation implies that the whole right-half of the Z_L' plane is accessible and that the zero resistance lines are mapped into each other.

The resonant frequency of the output inductor and capacitor is 2.16 GHz and very importantly is near the design frequency of this active antenna. At resonance, the transformation of Z_L to Z_L' is a drastic one, approximating to an impedance inversion for small Z_L. At 2.35 GHz, $Z_L = 0$ is transformed to $Z_L' = -j74$ Ω. The second and third harmonics are well above the resonant frequency of the LC network, and so are also subject to major changes.

To explain the formation of the DC-power/RF-power loop using this highly simplified model, the DC current, RF (fundamental) power output, and DC/RF efficiency were plotted as functions of the complex internal fundamental load impedance Z_L', with the internal harmonic impedances set to zero. The frequency was fixed at 2.334 GHz, the precise value

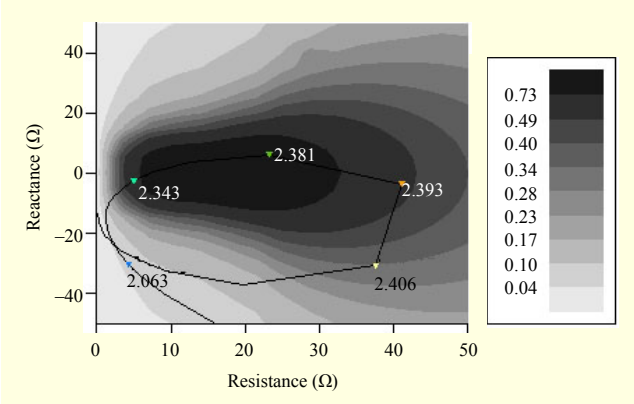


Fig. 9. Simulated values of fundamental output power (W) versus fundamental load impedance, for idealized transistor. (Harmonic impedances are zero. Incident drive power is constant at 26 dBm.)

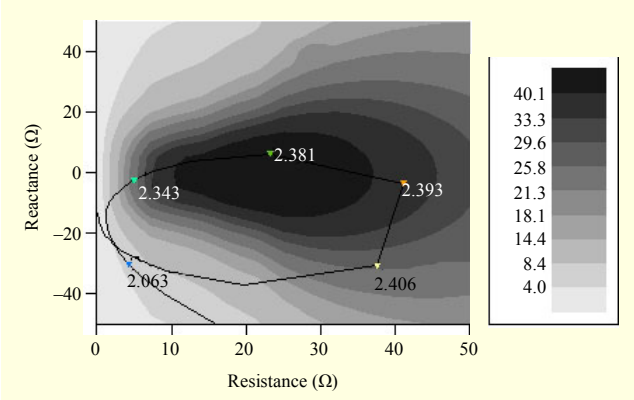


Fig. 10. Simulated values of DC to RF efficiency (%) versus fundamental load impedance for idealized transistor. (Harmonic internal impedances are zero. Incident drive power is constant at 26 dBm.)

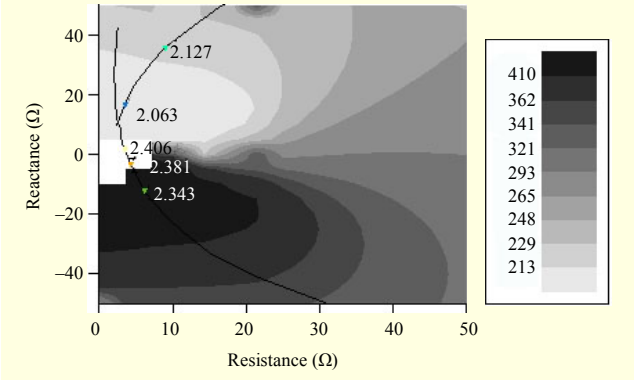


Fig. 11. Simulated values of DC supply current (mA) versus fundamental load impedance, for packaged transistor. (Harmonic impedances are zero. Incident drive power is constant at 26 dBm.)

being non-critical since there are no longer any sharply resonant elements in the circuit. The incident drive power at the

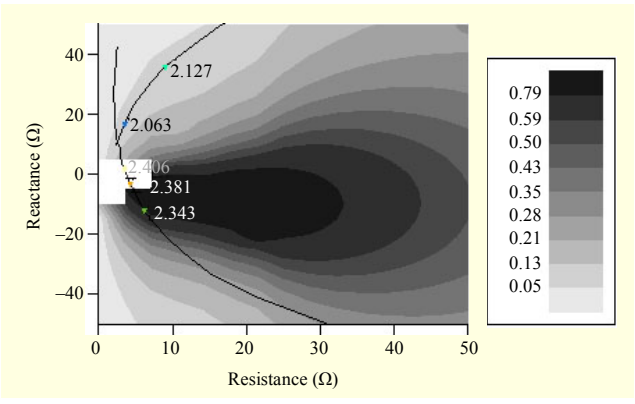


Fig. 12. Simulated values of fundamental output power (W) versus fundamental load impedance, for packaged transistor (Harmonic impedances are zero. Incident drive power is constant at 26 dBm.)

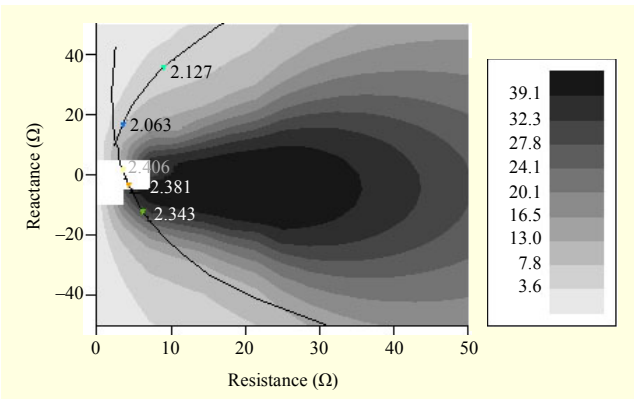


Fig. 13. Simulated values of DC to RF efficiency (%) versus fundamental load impedance, for packaged transistor. (Harmonic internal impedances are zero. Incident drive power is constant at 26 dBm.)

amplifier input was fixed at 26 dBm. Figures 8 through 10 show the simulation plots obtained.

The almost perfect symmetry of these plots about the zero reactance axis indicates that the internal capacitive feedback in the device is fairly small, and that with the output capacitance and packaging removed, we have an idealized device whose behavior is easily explicable by quasi-static characteristics. The behavior of the DC current plot is intuitively quite straightforward since increasing either resistance or reactance reduces the current by producing a negative excursion of the drain voltage below its knee point. The output power and efficiency plots are also easy to visualize in the Z_L' plane: the power is given by $I^2 R_L'$, where I is the fundamental component of load current, and the rough approximation can be made that I is proportional to DC supply current in nominal Class B operation, with some error arising from distortion of the ideal Class B current waveform when R_L' and/or X_L' is large enough to cause current clipping.

Figures 11 through 13 show the same power and efficiency dependencies plotted as functions of the external impedance Z_L. Note that these were obtained using the full transistor model (The simulator failed to converge in a small region of low load impedance, though instability was not observed experimentally).

By tracing the locus of Z_L or Z_L' in the power/current contour plots as they are swept out with increasing frequency for a rectangular patch load, it is a straightforward matter to predict the DC-power/RF-power loops that should be observed. Figures 11 through 13 show the locus of Z_L', and this is a straightforward image of the patch's resonant loop as seen in the Smith chart of Fig. 4.

Figures 8 through 10 show the corresponding locus of Z_L' as transformed by the output LC network only. The locus is totally different and shows an additional resonance loop (somewhat undersampled because of its very rapid frequency dependence). Figure 14 shows the power loops predicted by the two methods. They are quite similar in shape, and comparable current/power values are obtained at the same frequency. This confirms that it is a fair approximation to neglect the source feedback effects and thus obtain a very simple qualitative description of the main effects.

The formation of the loop results from the resonance effects caused by the interaction of the packaging L_D and C_{DS} with the resonant loop locus of the patch impedance. A critical range of Z_L values has a low enough real part and appropriate reactance to series resonate with L_D to give very low impedances. As the reactance approaches zero, there is a transition to parallel resonant behavior. The rate of change of Z_L' in this frequency region is very rapid, and most of the DC/RF power loop is traced out over a smaller frequency range than might be expected from the Q of the patch resonance alone. The practical operating bandwidth is correspondingly reduced. For example, if an operation is between points a2 and a3, the output power would fall by about 1 dB over a full bandwidth of 27 MHz (see Fig. 3). The interval between points a2 and a4 is only 44 MHz. The intrinsic impedance bandwidth of the patch, assuming perfect match at the center frequency, is 98 MHz and 57 MHz for return losses of 3 dB and 6.9 dB, the latter corresponding to 1 dB reduction of accepted power in a linear system.

Simulations using the complete model of this transistor, with arbitrary (not patch constrained) load impedances, predicted an optimum Z_L for power added efficiency of 6.9 – j6.0 Ω, with a corresponding power output of 31 dBm (the device is capable of higher outputs). This is in very close agreement with the value of 7 – j6.5 Ω quoted in [2]. The corresponding Z_L' is 14 – j3 Ω; as expected, the optimum internal impedance is close to a pure resistance. A capacitive external load is needed to partially cancel the inductive reactance, leaving in effect a ladder LC network with a reduced L value, which can transform 6.9 Ω into being resistive to a higher resistive value. Assuming for 6 V drain bias a peak to peak drain swing of 11 V, the predicted output power is approximately $1/8 \times 11^2/14 = 1.1$ W, which is in good agreement with the more accurately simulated value and is also consistent with the outputs near the highest efficiency region in Fig. 3.

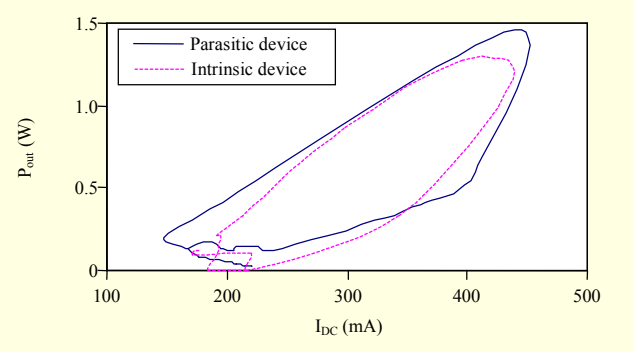


Fig. 14. Power loops predicted by approximate simulations.

IV. Conclusion

This case study of an active antenna successfully reproduced earlier results [5] for a similar structure and provided a simple physical explanation of its behavior. Sweeping the drive frequency generated a loop-shaped locus of RF versus DC power with very rapid frequency dependence, showing in this example that the usable bandwidth of an active antenna can be substantially smaller than the return loss bandwidth of its patch radiator.

A new simulation technique plotted contours of power-related parameters versus internal impedance, as seen at the terminals of an idealized device from which not only packaging parasitics but also the drain capacitance had been removed. These plots are highly symmetrical about the zero reactance axis and are easy to understand from quasi-static characteristics of the idealized device.

Viewing the drain capacitance as part of an LC impedance transformer between the patch and the idealized device, it was now easily seen that this particular active antenna was working near a resonance of this network; the formation of the loop and its rapid frequency dependence could easily be explained by the corresponding impedance transformation. The optimum internal load impedance proved as expected to be nearly resistive with a value close to that expected from a simple load line analysis, and the capacitive component of the optimum external load was immediately explicable.

The methods presented here can also help in visualizing harmonic load impedance effects, such as the prediction and

observation in [5], [6] of efficiency improvement from suppressing the TM_{20} patch resonance. Further analyses of these effects, and of design strategies for high efficiency such as Class F, can readily be made along the lines described.

References

[1] S. Cripps, *RF Power Amplifiers For Wireless Communications* 2nd ed., Artech House, 2006.

[2] J.D. Rhodes, "Output Universality in Maximum Efficiency Linear Power Amplifiers," *Int. J. Circuit Theory Appl.,* vol. 31, no. 4, 2003, pp. 385-405.

[3] M. Wren and T.J. Brazil, "Experimental Class-F Power Amplifier Design Using Computationally Efficient and Accurate Large-Signal pHEMT Model," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 5, May 2005, pp. 1723-1731.

[4] K. Chang et al., "Active Integrated Antennas," Invited Paper, *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, Mar. 2002, pp. 937-944.

[5] V. Radisic et al., "High-Efficiency Power Amplifier Integrated with Antenna," *IEEE Microw. Guided Wave Lett.*, vol. 7, no. 2, Feb. 1997, pp. 39-41.

[6] N.T. Ali et al., "Shaping Technique of an Active Patch Antenna for Harmonic Radiation Control," *IEEE MELCON*, May 16-19, Malaga, Spain, 2006, pp. 332-335.

[7] E.A. Elkhazmi, N.J. McEwan, and N.T. Ali, "A Power and Efficiency Measurement Technique for Active Patch Antennas," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 5, May 2000, pp. 868-870.

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