

# A Subthreshold CMOS RF Front-End Design for Low-Power Band-III T-DMB/DAB Receivers

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*This letter presents a CMOS RF front-end operating in a subthreshold region for low-power Band-III mobile TV applications. The performance and feasibility of the RF front-end are verified by integrating with a low-IF RF tuner fabricated in a 0.13- $\mu\text{m}$  CMOS technology. The RF front-end achieves the measured noise figure of 4.4 dB and a wide gain control range of 68.7 dB with a maximum gain of 54.7 dB. The power consumption of the RF front-end is 13.8 mW from a 1.2 V supply.*

*Keywords: CMOS, subthreshold, Band-III, T-DMB, DAB, mobile TV, low-IF, tuner.*

## I. Introduction

The minimization of power consumption is of primary concern for battery-operated handheld devices. Subthreshold operation is one of the low-power design approaches available. Although the devices in a subthreshold region have drawbacks such as degraded noise and linearity performance due to lower bias current [1], advances in device technology allow subthreshold region operation to be utilized in designing for low-power very-high-frequency (VHF) applications.

In this letter, we present a subthreshold CMOS RF front-end (RFE) for low-power mobile TV receivers. The RF performance of the proposed subthreshold RFE was confirmed by integrating it with a low-IF terrestrial digital multimedia broadcasting (T-DMB) tuner and validating the tuner output.

T-DMB requires BER of  $10^{-3}$  for a Band-III Gaussian channel for RF signal level from  $-95$  dBm to  $-10$  dBm. Therefore, the RFE should have at least 6 dB of noise figure (NF) to meet the requirements. The proposed RFE achieves the measured NF of 4.4 dB and a wide gain control range of 68.7 dB with the maximum gain of 54.7 dB. The power consumption of the RFE is 13.8 mW from a 1.2 V supply.

## II. Proposed Subthreshold RF Front-End Design

Figure 1 shows the simplified block diagram of the proposed subthreshold RFE. In this design, all RF circuits with large signal bandwidth are designed to operate in a subthreshold region or designed in a passive circuit topology for lowering the power consumption. Large transconductance for a lower current can be achieved by using a larger device in the subthreshold region [2]. The power consumption in subthreshold operation can reduce about 6.4 times less than that in saturation region [3].

Figure 2(a) shows the gain-switched common-gate low noise amplifier (CG-LNA), which operates in the subthreshold region. The gain-switched amplifiers relax the required linearity of the following stages, resulting in power saving. The

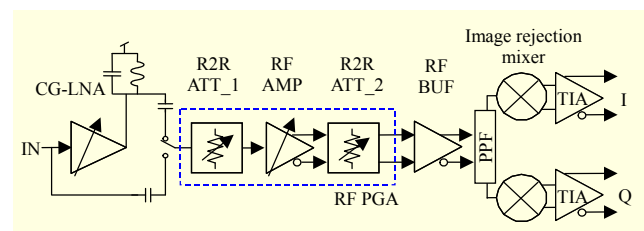


Fig. 1. Simplified block diagram of proposed subthreshold RFE.

Manuscript received Feb. 11, 2011; revised Apr. 21, 2011; accepted May 6, 2011.

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<http://dx.doi.org/10.4218/etrij.11.0211.0055>

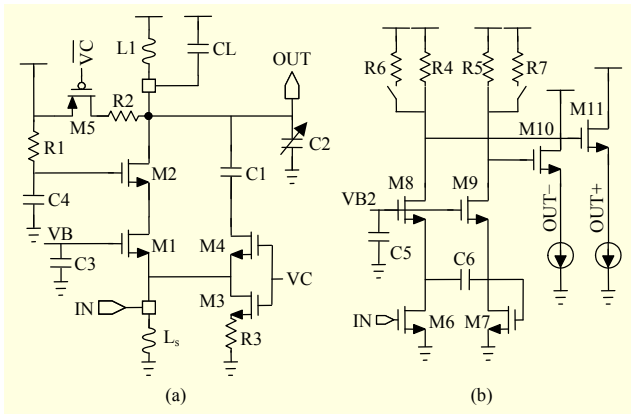


Fig. 2. (a) Gain-switched CG-LNA and (b) gain-switched RF amplifier.

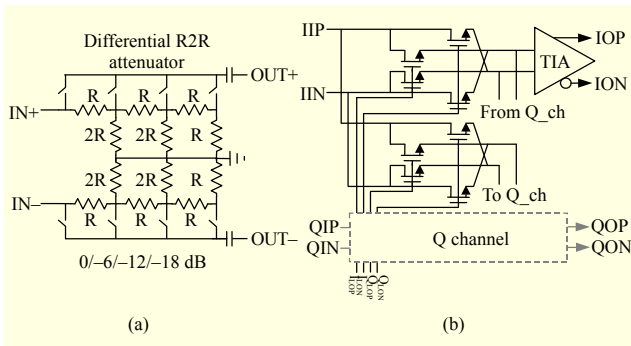


Fig. 3. (a) Differential R2R attenuator and (b) double quadrature image rejection passive mixer.

transistor M1 has a very large width of  $160 \mu\text{m} \times 16$  for large  $g_m$  with small currents, and the impact of large  $C_{gs}$  can be removed by configuring a parallel resonant circuit with the inductor  $L_s$  at operating frequency. The gate bias of the LNA is set through bandgap reference (BGR) circuit and adjusted by tuning circuits. Since the drain current in the subthreshold region operation is exponentially proportional to the gate and drain voltage, the DC bias point of the device is very important. The accurate bias circuit such as BGR is required to guarantee the stable operation. The RF signals which pass through M1 and M2 in the gain-switched CG-LNA are amplified in high gain mode. The transistors M3, M4, and M5 are turned on, and M1 is turned off in low-gain mode, transferring the received RF signal to the output terminal. The output matching frequency can be tuned by the switched capacitor bank, C2. The CG-LNA achieves 1.7-dB NF and  $-10$ -dBm IIP3 at the maximum gain of 24.4 dB. The bias current is 6.6 mA.

Figure 2(b) shows the gain-switched differential RF amplifier. It operates as a part of the RF automatic gain control (AGC). The transistors M6 and M7 have both a  $W/L$  of  $160 \mu\text{m}/0.13 \mu\text{m}$  and achieve a transconductance of 17 mS at  $814 \mu\text{A}$ . The RF amplifier achieves 7.6-dB NF and  $-5$ -dBm

IIP3 with a maximum gain of 19.1 dB.

Figure 3(a) shows the differential R2R attenuator. Since the parasitics of the attenuator increase with increasing the gain control range, two R2R attenuators are designed so that the parasitics are minimized. The first and second R2R attenuators have the attenuation range of 12 dB and 18 dB, respectively. Figure 3(b) shows the image rejection mixer. The image rejection mixer is designed in a double quadrature passive circuit topology to achieve high linearity and further power saving [4]. The mixer is carefully designed to have symmetrical geometry to minimize gain and phase mismatches among the quadrature signal paths. The transimpedance amplifiers have a fixed gain of 20 dB.

### III. Low-Power T-DMB Tuner Architecture

Figure 4 shows the RF tuner based on the proposed subthreshold RFE, which has a 2.048-MHz low-IF topology. The proposed RFE consists of a gain-switched CG-LNA, two R2R attenuators, a gain-switched RF amplifier, an RF buffer, an image rejection mixer, and an RF AGC with received signal strength indicator (RSSI). The 6th-order Chebyshev type-I complex bandpass filter is used to select the wanted channel and reject image signal [5]. The filter has a gain control range of 12 dB and an upper cutoff frequency of 2.816 MHz. IF programmable gain amplifier (PGA) operates as a part of the IF AGC. It has a wide gain control range of 61 dB with 1-dB control step and keeps the input level of the ADC constant to improve the SNR. For precise quadrature local oscillators (LOs) and fine frequency resolution, 4th-order sigma-delta fractional- $N$  frequency synthesizer (FS) is adopted [6], which employs 4/16/31 dividers and tuning circuits. The on-chip LC voltage-controlled oscillator (VCO) is designed to operate over the range from 620 MHz to 1,144 MHz. Then, the divider is used to obtain the mixer LO frequency. This scheme minimizes chip area by reducing the inductance. The RF tuner is configured via an I2C interface.

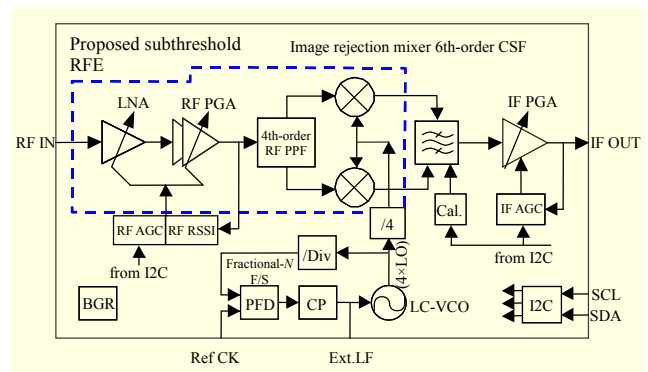


Fig. 4. Architecture of RF tuner with proposed subthreshold RFE.

## IV. Experimental Results

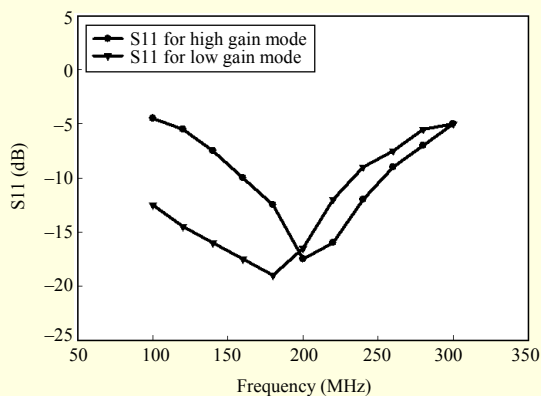
To verify RF performance and feasibility of the proposed subthreshold RFE, a T-DMB RF tuner, including the RFE, is fabricated in a 0.13- $\mu\text{m}$  CMOS technology as shown in Fig. 9. The proposed RFE with RF RSSI occupies  $1.2 \text{ mm} \times 1.6 \text{ mm}$ . In addition to the proposed RFE measurements, the performance for the entire tuner is also evaluated and summarized in Table 1.

Figure 5 shows that the measured S11 of the entire RF tuner is less than  $-10 \text{ dB}$  over the frequency range from 170 MHz to 236 MHz, regardless of the LNA operation mode. Figure 6 shows the measured NF for the entire RF tuner and gain for the proposed RFE as a function of frequency. Measurements show

**Table 1.** Measurement results summary and entire tuner performance comparison.

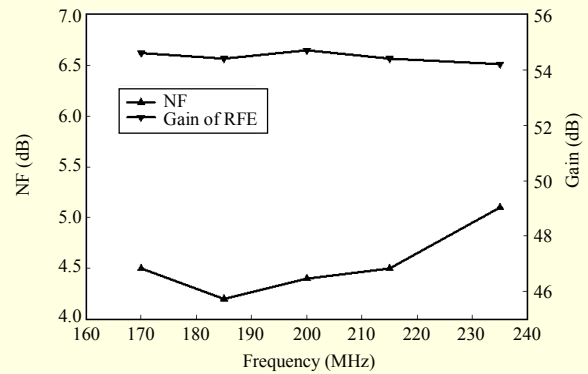
Reference	[7]	[8]	[9]	[10]	This work
Technology	0.18- $\mu\text{m}$ CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS	0.13-nm CMOS
Frequency	Band-III (174 MHz to 236 MHz)				
NF (dB)	1.4**	3.0	3.0	2.8	4.4
$G_{\text{MAX}}$ (dB)	(37)	(25*)	(30)	(-)	(54.7)
$G_{\text{CR}}$ (dB)	(33)	(28)	(30)	(-)	(68.7)
IIP3 (dBm)	(-)	(-)	(-)	(-)	(-)
$P_{1\text{dB}}$ (dBm)	(-)	(-)	(-)	(-)	(-)
$P_{\text{D}}$ (mW)	(27)	(-)	(-)	(-)	(13.8)
$V_{\text{DD}}$ (V)	1.8	1.2/2.5	1.2/1.8	1.2/1.8	1.2

Note. (-): RFE only, gain control range ( $G_{\text{CR}}$ ), and power dissipation ( $P_{\text{D}}$ ); \*: simulated or estimated value, \*\*: DSB NF, and \*\*\*: maximum gain mode.

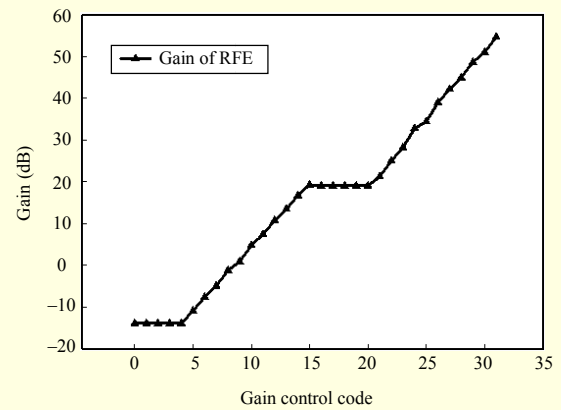


**Fig. 5.** Measured S11 of entire RF tuner as function of frequency.

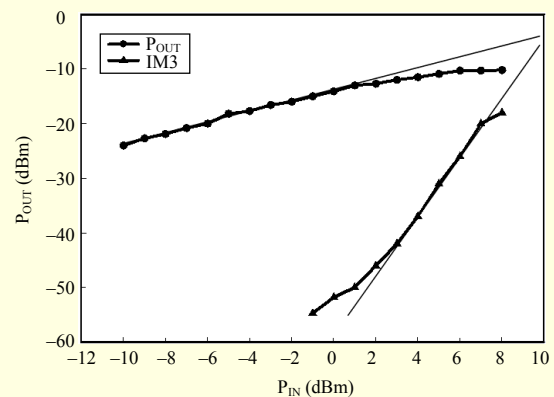
a minimum NF of 4.4 dB and the maximum RFE gain of 54.7 dB. The RFE and digital signal processors are integrated on the same silicon substrate. Since the NF is measured on condition that the RFE and digital signal processor are both turned on, the measured NF is much higher than that of the simulated NF due to the noise induced from the digital domains. Since the receiver noise performance is mostly



**Fig. 6.** Measured NF of entire RF tuner and maximum gain of proposed RFE as function of frequency.



**Fig. 7.** Measured gain control range of proposed RFE.



**Fig. 8.** Measured IIP3 for entire RF tuner.

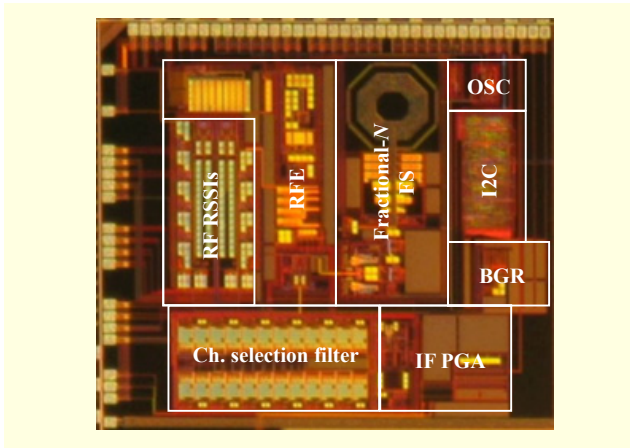


Fig. 9. Die photograph.

determined by the RFE, the measured tuner NF can be considered as the noise performance for the proposed subthreshold RFE. Figure 7 shows the measured gain control range of the proposed RFE, which has a wide range of 68.7 dB. The entire tuner achieves a gain control range of 129.3 dB. Figure 8 shows the measured IIP3 of +10 dBm and  $P_{1dB}$  of +3 dBm of the entire RF tuner at 200 MHz under minimum gain operation. The receiver's overall power consumption is about 38.4 mW while the proposed subthreshold RFE consumes 13.8 mW from a 1.2 V supply. The implemented RF tuner, which is based on the proposed subthreshold RFE, also has been validated with a T-DMB baseband demodulator. As shown in Table 1, the proposed RFE and the tuner are superior in terms of power dissipation to previously published works, except for the tuner in [10] which consumes less power than ours. The die photograph is shown in Fig. 9.

## V. Conclusion

In this letter, we presented a low-power RFE operating in a subthreshold region for VHF applications. The RF performance is evaluated through an RF tuner with the proposed RFE fabricated with 0.13- $\mu$ m CMOS technology. The proposed subthreshold RFE achieves a minimum NF of 4.4 dB with a good impedance matching over Band-III range and a high gain control range of 68.7 dB with a maximum gain of 54.7 dB, while consuming only 13.8 mW from a 1.2 V supply. Measurement results confirm that the subthreshold operation technique can be utilized in designing RF circuits for low-power VHF applications.

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