A Hybrid Audio ΔΣ Modulator with dB-Linear Gain Control Function

Yi-Gyeong Kim, Min-Hyung Cho, Bong Chan Kim, and Jong-Kee Kwon

A hybrid ΔΣ modulator for audio applications is presented in this paper. The pulse generator for digital-to-analog converter alleviates the requirement of the external clock jitter and calibrates the coefficient variation due to a process shift and temperature changes. The input resistor network in the first integrator offers a gain control function in a dB-linear fashion. Also, careful chopper stabilization implementation using return-to-zero scheme in the first continuous-time integrator minimizes both the influence of flicker noise and inflow noise due to chopping. The chip is implemented in a 0.13 μm CMOS technology (I/O devices) and occupies an active area of 0.37 mm^2. The ΔΣ modulator achieves a dynamic range (A-weighted) of 97.8 dB and a peak signal-to-noise-plus-distortion ratio of 90.0 dB over an audio bandwidth of 20 kHz with a 4.4 mW power consumption from 3.3 V. Also, the gain of the modulator is controlled from –9.5 dB to 8.5 dB, and the performance of the modulator is maintained up to 5 ns_{RMS} external clock jitter.

Keywords: Delta-sigma modulator, hybrid delta-sigma modulator, chopper stabilization (CHS), return-to-zero (RZ) DAC, RZ DAC, RTZ DAC, programmable gain amplifier (PGA), dB-linear.

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I. Introduction

Delta-sigma (ΔΣ) modulators in audio codecs are commonly realized using switched-capacitor circuits. A discrete-time (DT) ΔΣ modulator implemented using a switched-capacitor circuit offers many advantages such as good coefficient matching, low sensitivity to feedback digital-to-analog converter (DAC) clock jitter, and scalable sampling rate. However, there are several drawbacks associated with DT implementation of a ΔΣ modulator. A DT ΔΣ modulator requires an additional anti-aliasing filter. An anti-aliasing filter consumes additional power and its on-chip integration is difficult to achieve. In addition, DT implementation causes switching noise coupling to the input of the ΔΣ modulator. Switched-capacitor input circuitry creates signal-dependent glitches that cause harmonic distortion.

To avoid these drawbacks of a DT ΔΣ modulator, hybrid ΔΣ modulators composed of continuous-time (CT) and DT integrators have been reported in [1]-[4]. Compared to a ΔΣ modulator consisting of only DT integrators, a hybrid ΔΣ modulator offers several important advantages. For example, an anti-aliasing filter is not required. Because the sampling point is positioned after the CT first integrator, the ΔΣ modulator has inherent low-pass filter properties similar to an anti-aliasing filter. Also, since there are no capacitor-switching circuits at the input of the CT integrator, there are no signal dependent glitches. Therefore, hybrid implementation offers many conveniences from a system point of view.

Despite the advantages mentioned above, the architecture of a hybrid ΔΣ modulator has some problems that need to be solved to satisfy high-quality audio performance. For a high dynamic range (DR), the flicker noise of the first integrator has to be removed. Moreover, clock jitter requirement must be

alleviated to mitigate the PLL performance and achieve high DR. Finally, coefficient variations due to a process shift need to be calibrated to keep the modulator stable.

In this paper, we present a hybrid audio ΔΣ modulator with a loop filter composed of a CT first integrator and a DT second integrator. A chopper-stabilization (CHS) technique is carefully implemented in the CT first integrator using return-to-zero (RZ) scheme to minimize both the effect of the flicker noise and inflow noise due to chopping. A pulse generator using a simple oscillator is used to generate DAC pulses containing low pulse width jitter, and to calibrate coefficient variation due to a process shift. A dB-linear gain controller is incorporated in the first integrator. This paper is organized as follows. Section II introduces the ΔΣ modulator architecture. Section III describes the proposed circuit techniques and implementation. Section IV provides measurement results, and section V offers some concluding remarks.

II. Architecture

Figure 1 shows the architecture of the proposed ΔΣ modulator. The ΔΣ modulator is a second-order, 17-level, single-loop design composed of a CT first integrator and DT second integrator. The input signal range of the ΔΣ modulator is 2 V_{RMS}. The ΔΣ modulator is operated at a clock speed of 6.144 MHz, which corresponds to an OSR of 128. The theoretical SNR due to quantization noise alone is 117 dB. A scrambler is used in the feedback path to shape the mismatch noise from the multibit DAC. The scrambler adopts a data weighted averaging (DWA) technique, which is widely used to achieve first-order mismatch shaping [5], [6]. A feed-forward path is adopted between the output of the first integrator and input of the quantizer. This feed-forward path makes the first integrator process a second-order high-pass filtered signal component, thereby reducing the signal swing at the first integrator output and saving power consumption [7]-[9]. A

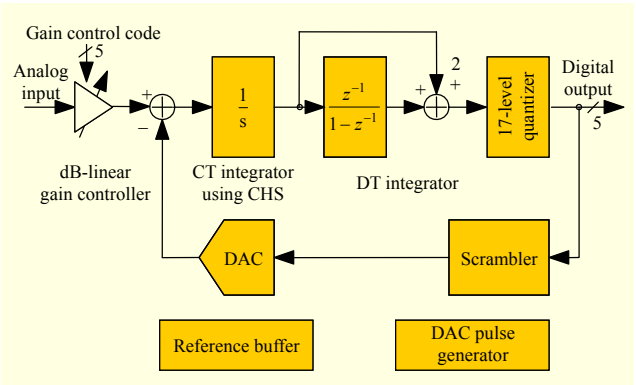

Fig. 1. ΔΣ modulator architecture.

feed-forward path could be implemented using a different method that connects the input of the ΔΣ modulator to the input of the second integrator, as in [1]. This method creates the same effect as the previous one. However, this structure has impure resistive input impedance, which generates capacitor switching noise [10]. In this paper, although there is an additional circuit, a summing node implemented with a capacitive adder, the ΔΣ modulator adopts the internal feed-forward path as shown in Fig. 1. Therefore, the modulator has pure resistive input impedance.

III. Circuit Techniques and Implementation

1. CHS in Continuous-Time Integrator

Flicker noise occurring in the first integrator goes through a loop filter with a signal transfer function (STF) characteristic. Flicker noise will then appear at the output of the ΔΣ modulator with little attenuation. By increasing the area of the input transistors of the operational amplifier in the integrators, especially the first integrator, flicker noise can be reduced. To achieve a DR of more than 95 dB and to maintain a small integrator area, another method for removing flicker noise is needed. CHS is a suitable method for the removal of flicker noise in a ΔΣ modulator due to the low-pass filter characteristic of the integrator [11], [12]. Although CHS is widely used in DT ΔΣ modulators, the use of CHS in a hybrid ΔΣ modulator has to give attention to the chopping noise in a CT integrator. To reduce the chopping noise in the CT integrator, an RZ scheme is used. Figure 2 shows the first integrator along with the timing diagram. After the RZ switches SW1 are open, chopping is performed. During the P2 phase, the chopping noise vanishes due to the charge conservation of the integrating capacitors. When the P1 phase starts, the integrator begins to integrate the signals from the input and DAC. The frequency of the CHS is set at half the sampling frequency (Fs/2). The RZ scheme has another benefit, which is the elimination of inter-symbol interference (ISI) errors [13]. A folded cascode OTA is used as an amplifier thanks to the feed-forward path. A simple resistor feedback DAC is adopted for good noise performance.

2. DAC Pulse Generator

The DAC consists of resistors, switches, and positive/negative reference voltages, and operates using the RZ scheme as in the timing diagram illustrated in Fig. 2. The performance of a ΔΣ modulator with an RZ DAC is sensitive to DAC pulse width jitter [14]. For more than a 95 dB DR, the DAC pulse width jitter requirement is about 78 ps_{RMS}, which is calculated from a 100 dB DR. This is not a stringent requirement in many systems. However, this is a stern requirement on the system

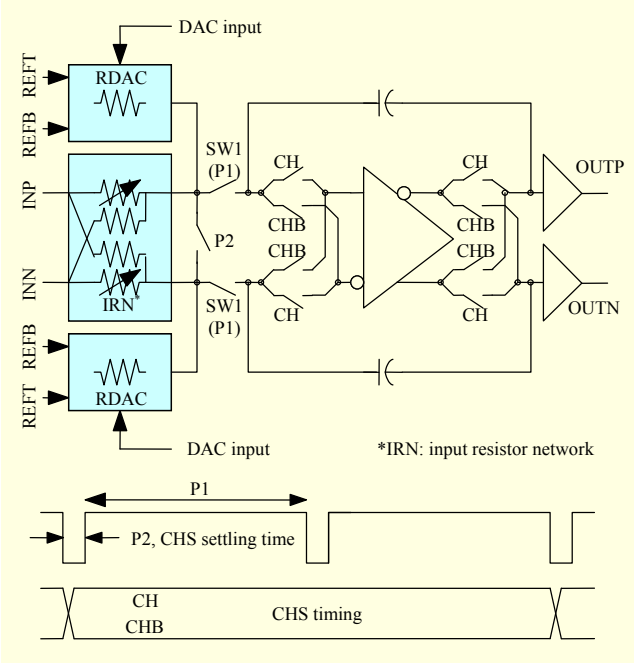

Fig. 2. First integrator and chopping timing diagram.

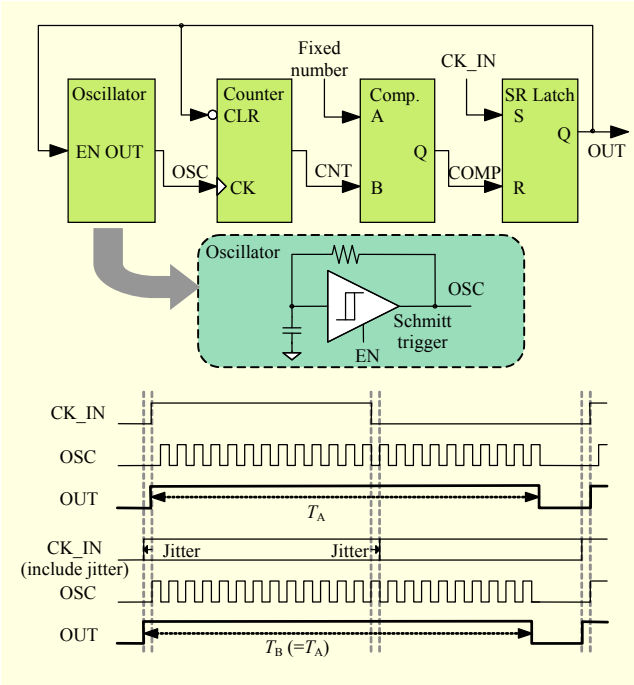

Fig. 3. DAC pulse generator and timing diagram.

clock compared to that of a DT ΔΣ modulator. To improve robustness to external clock jitter such as DT ΔΣ modulator, the proposed modulator adopts the DAC pulse generator which generates DAC pulses from the external clock and filters out the pulse width jitter. Therefore, the proposed modulator can maintain the dynamic performance under a low-quality system clock.

Figure 3 shows the DAC pulse generator and its timing diagram. The DAC pulse generator is composed of a counter, a comparator, SR-latch, and an oscillator that consists of a Schmitt trigger, resistors, and capacitors. The DAC pulse starts at the rising edge of the external clock and ends when the number of oscillator pulses equals a fixed number. That is, the pulse width is determined by the number of oscillator pulses. The pulse width jitter is not affected by the external clock but by the DAC pulse generator. In simulations, the jitter of the DAC pulse generator shows 24.6 ps_{RMS}, making it possible for the ΔΣ modulator to achieve an SNR of 116 dB.

In addition, the DAC pulse generator not only alleviates the requirement of the external clock jitter but also calibrates the coefficient variation due to process shift and temperature changes. The coefficient variation of the first integrator can lead to degradation in the performance of the ΔΣ modulator [1]. Therefore, it is important to calibrate the coefficient of the CT integrator to prevent the performance degradation or the modulator from becoming unstable. Since the ΔΣ modulator uses the RZ DAC, the coefficient of the integrator is determined by both the passive elements and the DAC pulse width for SW1. The pulse width is adjusted according to the frequency of the oscillator, which consists of the same resistors and capacitors as in the first integrator. The pulse width is proportional to the resistor-capacitor (RC) product value. For example, when the RC product value increases, the pulse width increases. When the RC product value decreases, the pulse width decreases, thereby resulting in a constant coefficient. Therefore, the coefficient variation of the first integrator is calibrated, and the ΔΣ modulator then does not suffer any stability problems.

3. dB-Linear Gain Controller

A dB-linear gain controller, usually called a programmable gain amplifier (PGA), is used in the audio codec. To satisfy a DR of more than 95 dB, a low-noise operational amplifier for the PGA is needed, resulting in a PGA with large area and high power consumption. The proposed ΔΣ modulator includes both PGA and ΔΣ modulator functions. The dB-linear gain control function is incorporated into the first integrator through an input resistor network, as shown in Fig. 4. It consists of fixed resistors R_B and adjustable resistors for gain control R_A connected to each other in a cross-coupled way. The current at the TP branch I_{TP} is given by

$$I_{TP} = \left\{ \frac{2}{(1-x)\cdot R_{REF}} - \frac{1}{R_{REF}} \right\} \cdot V_{INP} = \frac{1+x}{1-x} \cdot \frac{1}{R_{REF}} \cdot V_{INP}$$
$$\cong 10^{x} \cdot \frac{1}{R_{REF}} \cdot V_{INP}. \quad (1)$$

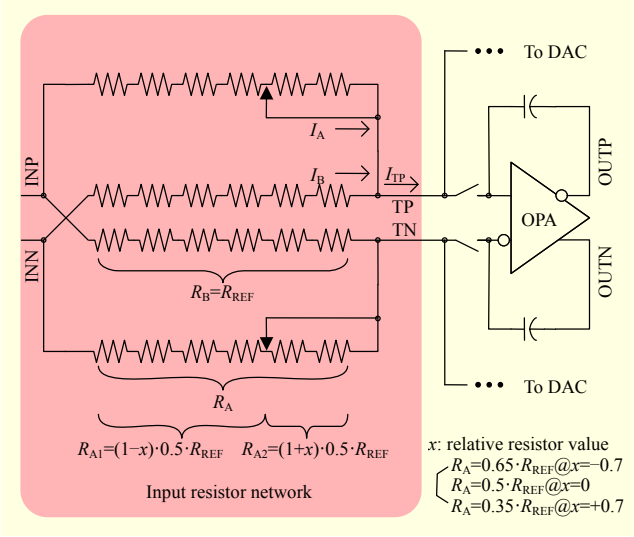

Fig. 4. Input resistor network for dB-linear gain control.

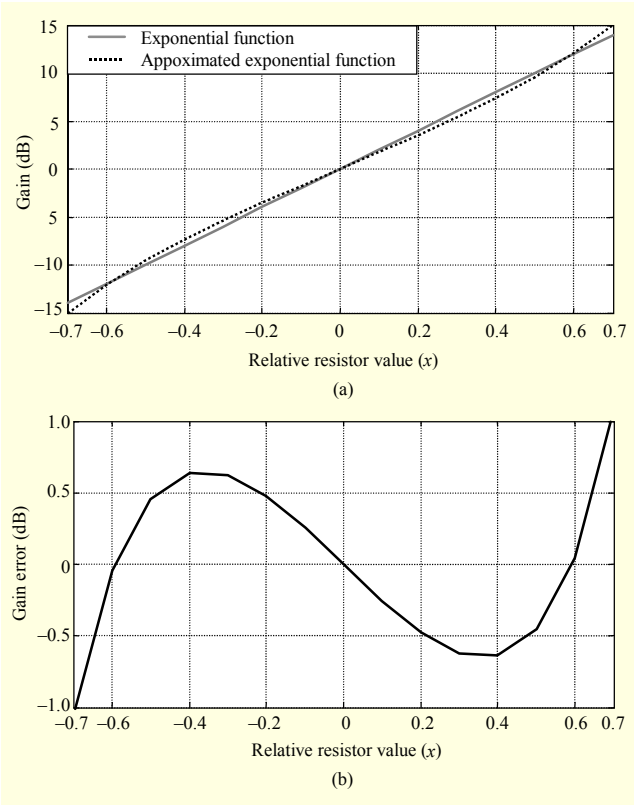

Fig. 5. (a) Gain plot and (b) gain error of approximated dB-linear function.

This shows that the gain term is an approximated exponential function of the variable x, which is the relative value of the variable resistor R_A. That is, the gain is controlled in a dB-linear fashion according to the variable x. Since the variable resistors are adjusted in a linear manner, the variable input resistors can be implemented using several identical

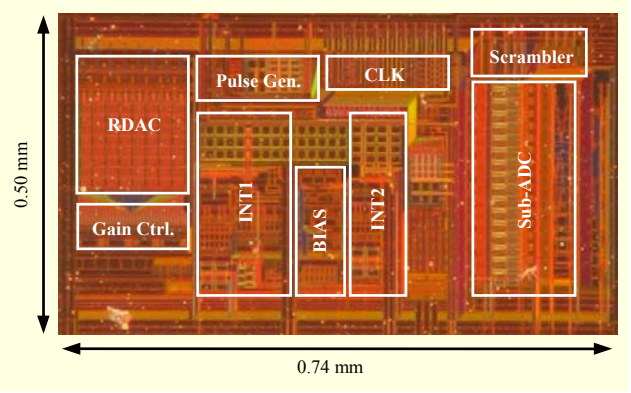

Fig. 6. Photograph of the chip.

resistors and switches. This makes it possible to implement a simple and small input resistor network.

Figure 5 shows a comparison between the exponential function and approximated exponential function given in (1). The results show that the gain can be adjustable within the range of –15 dB to 15 dB with an error of ±1 dB. The prototype ΔΣ modulator is designed with a gain adjustment from –8 dB to 7.5 dB in 0.5 dB steps.

IV. Measurement Results

A prototype chip was fabricated in a 0.13 μm CMOS technology (I/O devices) and occupies a 0.37 mm^2 (0.74 mm × 0.50 mm) active area, as shown in Fig. 6. The total power consumption is 4.4 mW (analog 3.6 mW, digital 0.8 mW) from a 3.3 V supply. The modulator achieves a 90.0 dB peak SNDR (A-weighted) and a 97.8 dB DR (A-weighted) over a bandwidth of 20 kHz. Figure 7(a) shows the measured output spectrum of a 1 kHz and –4 dBFS sinusoidal signal. When the CHS of the integrator is ON or OFF, the SNDR (A-weighted) values are 90.0 dB or 84.9 dB, respectively. Figure 7(b) shows the measured output spectrum of a 1 kHz and –30 dBFS sinusoidal signal. The SNDR (A-weighted) values are 67.8 dB or 59.4 dB with the CHS of the integrator in ON or OFF states, respectively. These results show that peak SNDR and DR are enhanced by the CHS technique used in the CT first integrator. Figure 8 shows the SNR and SNDR values versus the input level.

The input stage offers a 32-level gain control function with 0.5 dB steps. As shown in Fig. 9, the measured gain is from –9.5 dB to 8.5 dB, and the maximum differential nonlinearity (DNL) is 0.27 LSB, with a 0.13 dB error, which is acceptable for 0.5 LSB step.

Figure 10 shows the ΔΣ modulator performance in the presence of clock jitter. A wide-band jitter of up to 40 ns_{RMS} is injected into the main clock. As shown in Fig. 10, the SNDR of

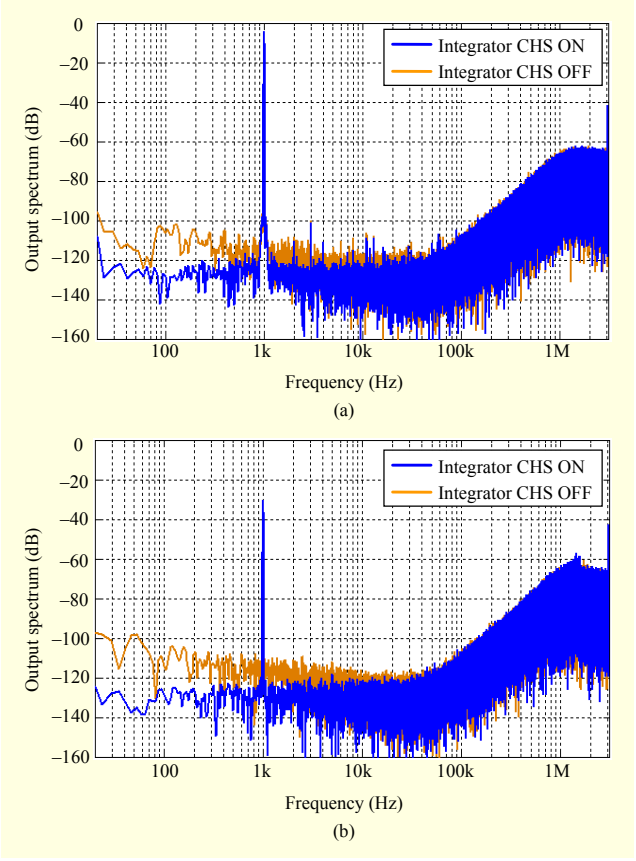

Fig. 7. FFT plot of (a) –4 dBFS input and (b) –30 dBFS input, 1 kHz sine wave.

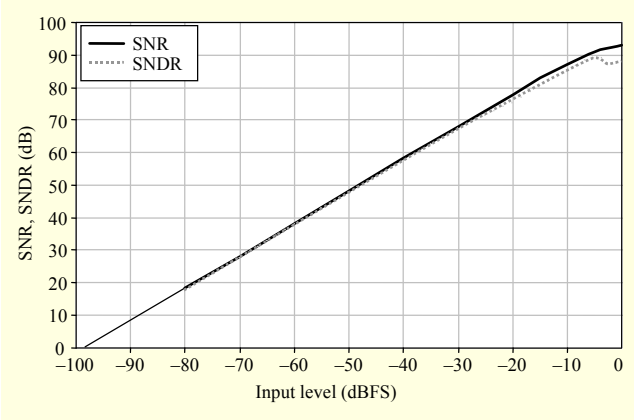

Fig. 8. SNR and SNDR versus the input level.

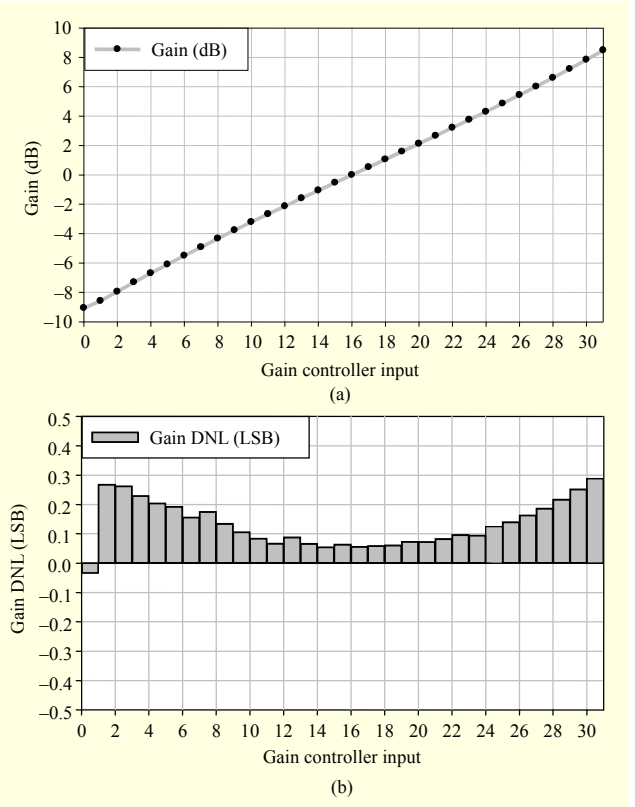

Fig. 9. (a) Gain and (b) gain DNL versus the gain controller input.

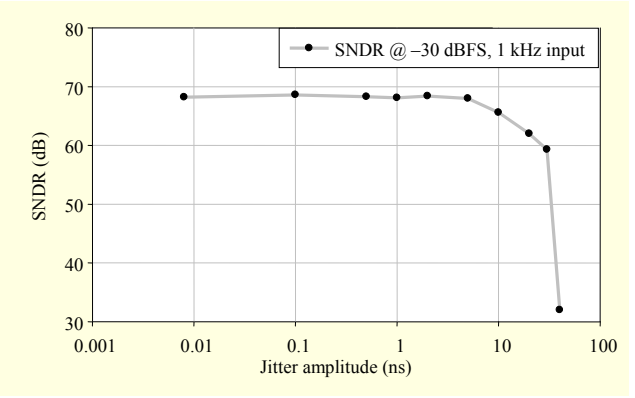

Fig. 10. SNDR versus external clock jitter amplitude.

the modulator is maintained in the presence of clock jitter up to 5 ns_{RMS}. In conclusion, the jitter requirement of the external clock can be neglected.

The performance of the proposed ΔΣ modulator is summarized in Table 1.

The figure of merit (FoM) of a ΔΣ modulator is defined as in [8] as

$$\text{FoM} = \text{DR} + 10 \cdot \log\left(\frac{\text{Signal bandwidth}}{\text{Power}}\right). \quad (2)$$

A performance comparison of several designs for state-of-the-art ΔΣ modulators with the same bandwidth is shown in Table 2. The proposed ΔΣ modulator has 164.4 dB FoM. This FoM is comparable to those of the ΔΣ modulators shown in Table 2. In addition the proposed ΔΣ modulator has a programmable gain control function.

Table 1. Performance summary.

Power supply voltage	3.3 V
Signal bandwidth	20 kHz
Sampling frequency	6.144 MHz
Full scale input	2 V_{RMS} differential
SNR	97.8 dB (A-weighted)
DR, –30 dBFS	97.8 dB (A-weighted)
Peak SNDR, –4 dBFS	90.0 dB (A-weighted)
Total power consumption	4.4 mW
Chip area	0.37 mm^2 (0.74 mm × 0.50 mm)
Technology	0.13 μm CMOS technology, 3.3 V I/O devices

Table 2. Comparison of FoM.

Architecture	BW (kHz)	DR (dB)	VDD (V)	Power (mW)	FoM (dB)
2nd order, 32 b, SC [15]	20	102	3.3	70.4	156.5
2nd order, 4 b, Hybrid [3]	20	102	3.3	37.3	159.3
2nd order, 4 b, Hybrid [1]	20	106	3.3	18	166.5
3rd order, 1.5 b, Hybrid [4]	20	101	3.3	15	162.2
2nd order,17 level, Hybrid (this work)	20	97.8	3.3	4.4	164.4

V. Conclusion

The hybrid audio ΔΣ modulator is presented in this paper. The CHS technique is applied to the first CT integrator to minimize the effects of flicker noise. The DAC pulse generator alleviates the requirement of the external clock jitter and calibrates the coefficient variation due to a process shift and temperature changes. The input resistor network in the first integrator offers a gain control function in a dB-linear fashion. The prototype ΔΣ modulator achieves a DR (A-weighted) of 97.8 dB, and a peak SNDR of 90.0 dB over an audio bandwidth of 20 kHz with a 4.4 mW power consumption from 3.3 V. Also, the gain of the ΔΣ modulator is controlled from −9.5 dB to 8.5 dB, and the performance of the modulator is maintained up to 5 ns_{RMS} external clock jitter. The chip occupies an active area of 0.37 mm^2.

References

[1] K. Nguyen et al., "A 106-dB SNR Hybrid Oversampling Analog-to-Digital Converter for Digital Audio," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, Dec. 2005, pp. 2408-2415.

[2] S.D. Kulchycki et al., "A 77-dB 7.5-MHz Hybrid Continuous-Time/Discrete-Time Cascaded ΣΔ Modulator," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, Apr. 2008, pp. 796-804.

[3] P. Morrow et al., "A 0.18 μm 102 dB-SNR Mixed CT SC Audio-Band ADC," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 178-179.

[4] M.Y. Choi et al., "A 101-dB SNR Hybrid Delta-Sigma Audio ADC Using Post Integration Time Control," *Proc. IEEE Custom Integr. Circuits Conf.*, 2008, pp. 89-92.

[5] E. Prosalentis and G.S. Tombras, "Elimination of Idle Tones by a 2-Bit Adaptive Sigma-Delta Modulation System," *ETRI J.,* vol. 31, no. 4, Aug. 2009, pp. 393-398.

[6] R.T. Baird and T.S. Fiez, "Linearity Enhancement of Multibit ΔΣ A/D and D/A Converters Using Data Weighted Averaging," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 12, Dec. 1995, pp. 753-762.

[7] S.R. Norsworthy, R. Schreier, and G.C. Temes, *Delta-Sigma Data Converters: Theory, Design and Simulation*, New York: IEEE Press, 1996.

[8] R. Schreier and G.C. Temes, *Understanding Delta-Sigma Data Converters,* Piscataway, NJ: IEEE Press, 2005.

[9] Y.G. Kim and J.K. Kwon, "Multi-bit Sigma-Delta Modulator for Low Distortion and High-Speed Operation," *ETRI J.*, vol. 29, no. 6, Dec. 2007, pp. 835-837.

[10] Y.D. Jeon et al., "A 1.2 V 12 b 60 MS/s CMOS Analog Front-End for Image Signal Processing," *ETRI J.,* vol. 31, no. 6, Dec. 2009, pp. 717-724.

[11] A.B. Early, "Chopper Stabilized Delta-Sigma Analog-to-Digital Converter," U.S. Patent 4, 939,516, to Crystal Semiconductor, 1990.

[12] Y.G. Kim et al., "A 105.5 dB, 0.49 mm^2 Audio ΣΔ Modulator Using Chopper Stabilization and Fully Randomized DWA," *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, 2008, pp. 503-506.

[13] R. Adams, K.Q. Nguyen, and K. Sweetland, "A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, Dec. 1998, pp. 1871-1878.

[14] O. Olieai and H. Aboushady, "Jitter Effects in Continuous-Time Sigma-Delta Modulators with Delayed Return-to-Zero Feedback," *Proc. IEEE ISCAS*, vol. 46, June 1998, pp. 991-1001.

[15] E. Fogleman, J. Welz, and I. Galton, "An Audio ADC Delta-Sigma Modulator with 100-dB Peak SINAD and 102-dB DR Using a Second-Order Mismatch-Shaping DAC," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, 2001, pp. 339-348.

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