Low-Power Cool Bypass Switch for Hot Spot Prevention in Photovoltaic Panels

Salvatore Pennisi, Francesco Pulvirenti, and Amedeo La Scala

With the introduction of high-current 8-inch solar cells, conventional Schottky bypass diodes, usually adopted in photovoltaic (PV) panels to prevent the hot spot phenomenon, are becoming ineffective as they cause relatively high voltage drops with associated undue power consumption. In this paper, we present the architecture of an active circuit that reduces the aforementioned power dissipation by profitably replacing the bypass diode through a power MOS switch with its embedded driving circuitry. Experimental prototypes were fabricated and tested, showing that the proposed solution allows a reduction of the power dissipation by more than 70% compared to conventional Schottky diodes. The whole circuit does not require a dedicated DC power and is fully compatible with standard CMOS technologies. This enables its integration, even directly on the panel, thereby opening new scenarios for next generation PV systems.

Keywords: Photovoltaic cells, hot spot, charge pump, bypass diode, Schottky diode.

I. Introduction

A photovoltaic (PV) panel (also referred to as module) is realized by interconnecting in series a suitable number of PV cells to provide the required output voltage (for instance, 72 cells in mono or poly-crystalline technology are used to provide around 36 V), as illustrated in Fig. 1(a). A PV array is then obtained by connecting in series a certain number of panels to form a string and strings are then connected in parallel to achieve the required output power [1], [2]. Under optimal operating conditions, the PV cells are uniformly illuminated; hence, all are able to generate the same nominal current. However, under actual operating conditions, the cells are never exactly identical due to fabrication tolerances. Besides, some cells may be partially shaded (due to optical obstacles, clouds, dust collection, and so on) or damaged and consequently limit the current flow of the other cells connected in series and illuminated normally [3]. More precisely, what is limited is the current of all those modules connected in the same series string of the array. This may drastically reduce the power and efficiency of the whole PV system [4], [5]. When a PV cell is sufficiently shaded, the current generated by the other cells reverses the polarity across the shaded cell. This causes an overvoltage which, if higher than the cell breakdown voltage, may produce an excessive overheating and in some cases a permanent damage, like broken glass or even start a fire. This effect is known as a hot spot [6]-[8]. In a conventional PV panel, hot spots are avoided by connecting a bypass diode in reverse across a certain group of cells [9]-[11]. This solution is shown in Fig. 1(b). It is seen that these diodes offer an alternative path to the current flow, so the shaded cell does not act as a load. Indeed, if a cell is shaded (marked with an "X" in the figure), the voltage drop across that cell causes the

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Salvatore Pennisi (phone: +39 095 7382318, email: spennisi@dieei.unict.it) is with the Dipartimento di Ingegneria Elettrica Elettronica e Informatica, University of Catania, Catania, Italy,

Francesco Pulvirenti (email: francesco.pulvirenti@st.com) and Amedeo La Scala (email: amedeo.la-scala@st.com) are with the Photovoltaic Business Unit, STMicroelectronics, Catania, Italy.

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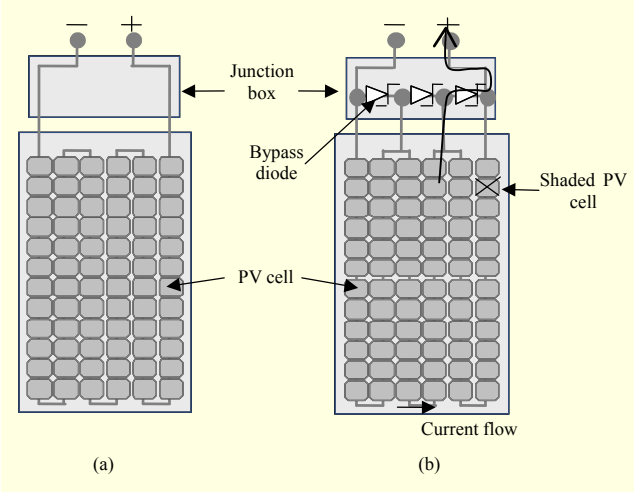

Fig. 1. PV panel: (a) realized through series connection of PV cells and (b) where shaded cell is marked with "X". Alternative current path offered by bypass diode is highlighted.

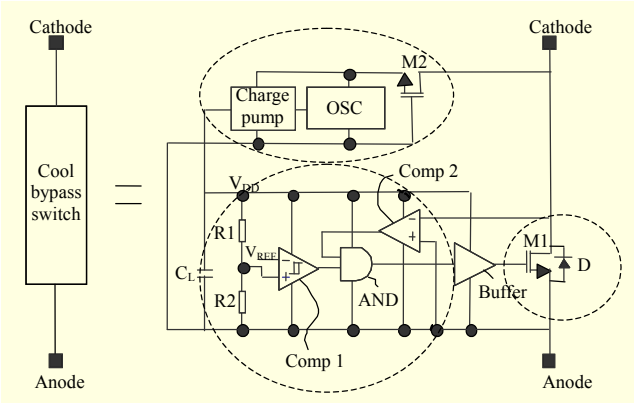

Fig. 2. Simplified block diagram of the proposed cool bypass switch (CBS).

associated diode to be forward biased thereby acting as a bypass element for the current. The above described solution is effective, but it shifts the overheating problem to the bypass diodes.

To minimize power dissipation, Schottky diodes are employed as their threshold voltage is around 0.35 V, which is much less than a conventional diode. The suitability of these diodes, however, has been reduced with the emergence in the market of high-efficiency 6-inch PV cells, that are able to generate currents as high as 9 A. Such high currents cause the forward voltage of each Schottky diode to rise up to 450 mV; hence, the associated power dissipation, with results around 4 W, become unacceptable.

To limit the power dissipation, one possible solution is to replace the bypass diode with a power MOS transistor. Indeed, the voltage drop between the MOS drain and source terminals can be limited to a few tens of millivolts so that the power dissipation can be contained to a few hundreds of milliwatts. This approach has been implemented by the Fraunhofer Institute [11]. In this original solution, the voltage drop of the MOS parasitic drain-source diode is boosted through an inductive DC/DC converter circuit to obtain the required driving voltage for the gate terminal of the same MOS transistor. Unfortunately, this technique cannot be integrated into a monolithic circuit because of the presence of the bulky inductor. Instead, a solution compatible with standard low-cost IC technologies would be desirable as it would allow a sensible area and cost reduction. The miniaturization coupled with the reduction of the power dissipation would also enable the integration of the circuit directly on the panel, avoiding mounting the diode in a junction box and further reducing costs.

To achieve these targets, we present in this paper a solution that overcomes the limitations exhibited by the Fraunhofer approach and that is fully compatible with CMOS technologies; hence, suitable for integration as a system in a package. Since the working temperature of the proposed bypass device is lower than for conventional diodes, we refer to the proposed solution as the cool bypass switch (CBS). We describe the principle of operation and implementation of the CBS in section II. Experimental results will be discussed in section III, including a comparison with two conventional diodes used in this application. Finally, some author conclusions will be given in section IV.

II. Circuit Description

Starting from the approach proposed in [12], we eliminate the need for the inductor in the DC/DC voltage boosting converter by exploiting a charge pump to generate the driving voltage for the power MOS transistor. Capacitive charge pumps are normally easier to integrate than inductive step-up converters with standard IC technologies [13], [14]. Besides, the turning on and turning off events are controlled by a threshold comparator Comp1, whose threshold voltages are easily and precisely set (for example, by means of a resistive voltage divider) and may be adjusted according to the minimum turn on threshold of the power MOS transistor M1.

A different strategy was originally adopted in [12] where the turning on/off events are defined with a timer. From a fabrication point of view, relating the turning on/off events to a time constant rather than to voltage thresholds (as implemented in the proposed architecture) could severely impact the yield because of the process spread. In fact, any correlation between a constant time defined by diffused resistor/capacitor and the turn-on threshold of a power MOS cannot be guaranteed.

The block scheme of the proposed circuit is illustrated in Fig. 2. It is made up of four main sections in which:

i) The power MOS M1 is the main switching element. In the same figure, the parasitic drain-bulk diode of M1, D, is also shown. Since the source and bulk terminals of M1 are short circuited, this diode is connected between the drain and source. D plays a fundamental role in the circuit operation.

ii) The voltage-boosting section includes a charge pump and a local oscillator. This pump boosts the voltage drop across D to the supply voltage V_{DD} required by the following sections. The role of the MOS transistor M_2 is to protect from high voltage the oscillator circuit normally realized with low voltage transistors. For this purpose, M_2 must have a turn-on threshold smaller than that of the intrinsic diode of the integrated structure of the MOS power transistor M_1 (generally, about 300 mV to 400 mV).

iii) Comparator Comp1 monitors the two V_{DD} threshold voltages, and Comp2 monitors the polarity across M_1. Both comparators are used to generate the switch-on signal to M_1.

iv) The Buffer drives the gate terminal of M_1.

During normal PV panel operations, the voltage between the drain and source of M_1 is positive, M_1 is held in the cut-off region and the auxiliary driving system is disabled. This situation is exemplified in Fig. 3(a).

If the portion of the panel connected to the power MOS transistor is shaded, then the drain-source voltage of M_1 inverts its sign becoming negative as the current generated by the illuminated cells flows from the anode to the cathode of D. As soon as M_2 turns on, the voltage drop across D can be exploited by the charge pump. This situation is exemplified in Fig. 3(b) with the voltage values annotated on the left. The current from the other cells/panels flows through D.

After some oscillator cycles, capacitor C is charged to the required voltage V_{DD} needed by the buffer to turn on M_1 with the adequate overdrive to minimize the drain-source resistance, $R_{ds,on}$. This situation is exemplified in Fig. 3(b) with the voltage values annotated on the right. In this case, the major part of the current flows through M1.

Of course, the charge on C_L must be periodically restored due to unavoidable current losses. The whole driving system can be designed so that the time needed to charge C_L is much less (for instance <10%) than the time in which M_1 remains in its on state. Actually, when the voltage across C_L increases to a certain threshold value (for instance, it may be set to 5 V), this occurrence is detected through the voltage comparator Comp1, so that the driving block can turn on M_1. Conversely, when the voltage across C_L decreases to a lower threshold (it may be 4.5 V), M_1 is turned off to restore the charge in the capacitor C_L.

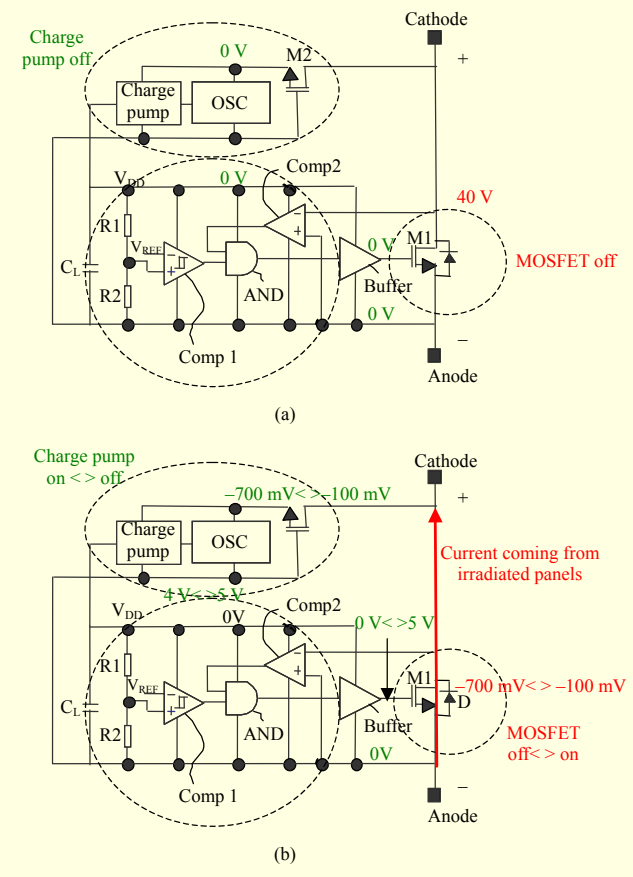

Fig. 3. CBS under different operating conditions: (a) panel fully irradiated and M1 and D both off and (b) two different cases: i) panel shaded and M1 off (D in forward mode and charge pump not completely settled) and ii) panel shaded and M1 on (charge pump has fully turned on M1 so that D is in forward mode but below his threshold). In these two last cases, the current coming from the other irradiated panels flows through either D or M1, respectively.

When the shadow is removed, the comparator Comp2 detects the reverse polarity condition switching off M_1 (also M_2 is turned off and the charge pump disabled). The AND gate performs the logic product of the signals coming form Comp1 and Comp2, so that M_1 is switched off provided that at least one comparator output is 0.

As can be seen, the proposed architecture is made up of conventional subblocks. This represents a remarkable advantage because it allows circuit reliability and robustness to be preserved. As a result, almost all the building blocks of the proposed device have been designed with quite standard topologies, and for this reason, they will not be described in this paper. Both the oscillator and the charge pump have been implemented with low-voltage threshold CMOS transistors because these circuits are directly supplied by the voltage across the body diode D of M_1, which can drop down to

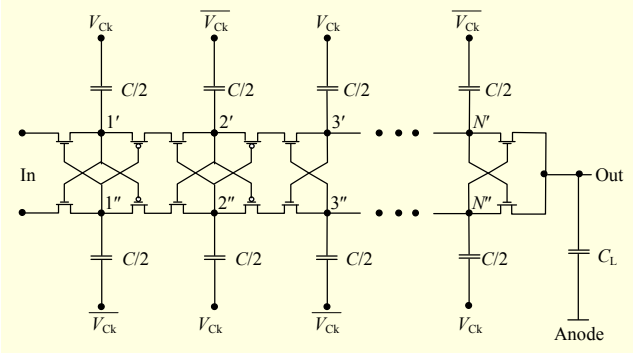

Fig. 4. Block scheme of adopted charge pump [15]. Required number of stages is 13.

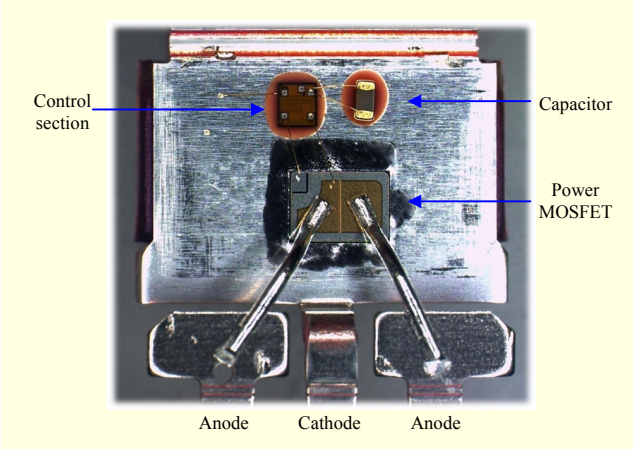

Fig. 5. Photograph of fabricated CBS prototype.

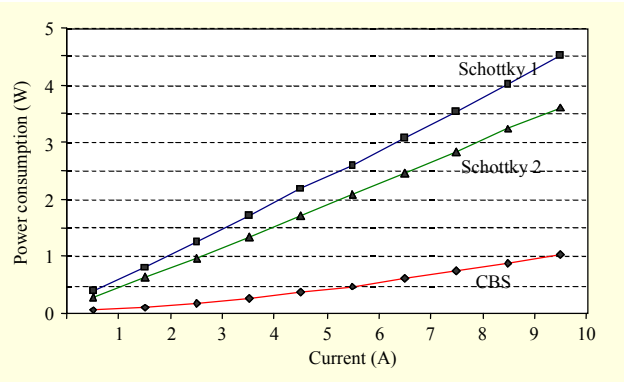

Fig. 6. Power consumption of two commercially available Schottky diodes used in photovoltaic applications and of proposed CBS, versus forward bias current.

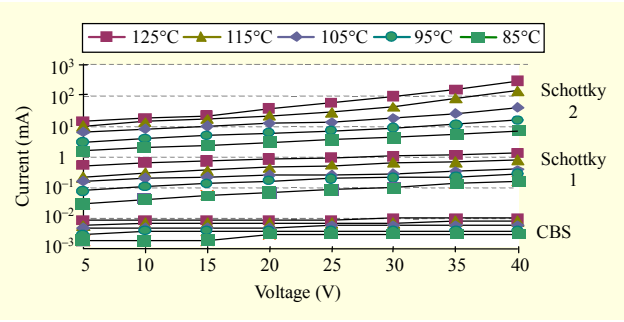

Fig. 7. Leakage current of the two reference Schottky diodes and of the proposed CBS versus reverse voltage, for five different temperature values (85°C to 125°C).

500 mV at high temperature. Furthermore, the charge pump has been implemented according to the architecture discussed in [15] where, the number of multiplication stage has been set to 13. The schematic of the charge pump is illustrated in Fig. 4, and it is often referred to as latched charge pump because it includes a latch in each stage. Finally, the oscillator is of the relaxation type with oscillation frequency of 2.5 MHz.

III. Experimental Validation

The proposed CBS was prototyped by assembling three devices into one package (TO-220) as illustrated in Fig. 5. The devices are i) the control block (charge pump, control section, and buffer) expressly designed for this application and fabricated using the BCD6S (Bipolar-CMOS-DMOS) technology of STMicroelectronics [16], ii) the discrete capacitor C_L, and iii) the power MOSFET fabricated using the 5H4C technology of STMicroelectronics [17].

The CBS was tested according to the TÜV standard [18]. In addition, we compared the performance of the proposed circuit with two standard Schottky diodes, the first one having a very low leakage current in reverse polarity but a relatively high voltage drop and the second one having a higher leakage current and a lower voltage drop.

Figure 6 depicts the power consumption of the proposed circuit and the two above mentioned Schottky diodes versus the biasing forward current.

It can be seen that the power consumption of the Schottky diodes is almost three times than that of the proposed circuit in the considered current range. In particular, the power consumption of the proposed circuit is around 0.8 W at 8 A (which is the maximum current provided by standard 6-inch cells).

Figure 7 shows the leakage current of the two reference Schottky diodes, assembled in a TO-220 package, and of the proposed solution, versus the reverse voltage. Five temperature values ranging from 85°C to 125°C with a step of 10ºC were considered. As expected, the leakage current increases with temperature. However, in the proposed solution, it is always lower than 10 μA, for the temperature range considered. Compared to the proposed solution, the leakage currents of the Schottky diodes is greater by one order of magnitude at least. The heat dissipation was measured at the steady state and without using dissipation tools. The ambient temperature was

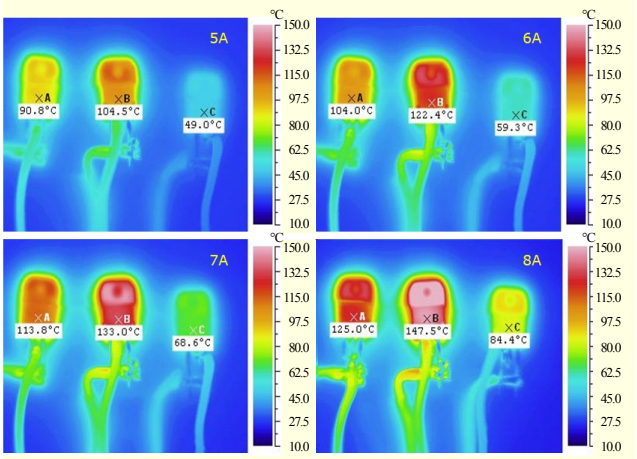

Fig. 8. Heat dissipation of two reference Schottky diodes (A and B) and of proposed CBS (C) for four different forward currents (5 A through 8 A). Ambient temperature is kept constant to 25ºC.

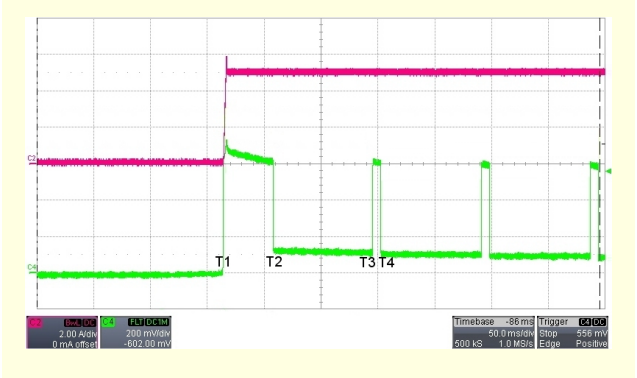

Fig. 9. Anode-to-cathode CBS voltage response (lower trace) to a 5-mA step (upper trace). After current step is applied (for t>T1), upper voltage levels correspond to M1 switched off and lower voltage level correspond to M1 switched on.

set to 25ºC.

Figure 8 has been acquired with an infra-red sensitive camera and shows the iso-thermal map of the three devices, biased in forward mode at the following currents (5 A, 6 A, 7 A, and 8 A). The upper bound of 8 A was dictated by the fact that the temperature of one of the Schottky diodes nearly reached the limit specification of 150ºC.

To demonstrate the effectiveness of the proposed circuit to prevent the hot spot, we first tested experimentally the time-domain behavior of the CBS when applying a 5-mA current step. This condition emulates the actual operating condition in which no current flows through the CBS under regular shadowing, and then a large current flows through the CBS if one or more PV cells are shadowed.

In Fig. 9, the CBS anode-to-cathode current (upper trace, C2) and the anode-to-cathode voltage (lower trace, C4) is

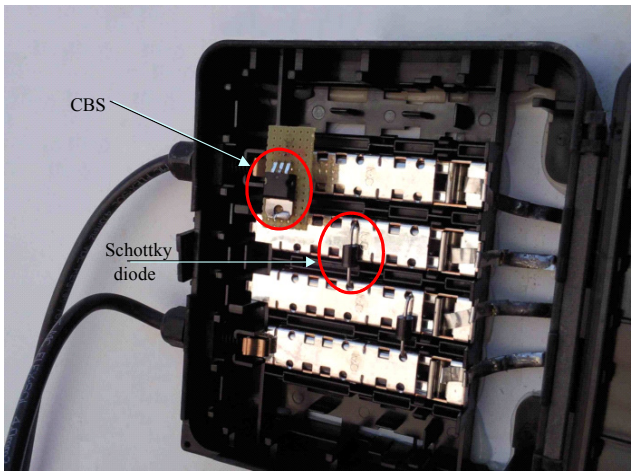

Fig. 10. Junction box equipped with one prototyped CBS and two conventional Schottky diodes.

plotted. Before time T1, no current is applied; therefore, the CBS is turned off. In T1, we apply a 5-mA step. This current flows initially through the drain-bulk parasitic diode that is hence forward biased with a peak voltage of 730 mV. This voltage is used by the charge pump and boosted across the capacitor C_L. In T3, the boosted voltage equals 5 V and detected by the comparator that enables the gate driver of the power MOS. During the T2-to-T3 interval, the power MOSFET is turned on and the anode-to-cathode voltage decreases to about 100 mV. In this interval, the voltage across C_L decreases due to charge losses and, once a threshold is reached, the charge pump is re-activated, during interval T3-to-T4. Observe that the repetitive charge time interval T4–T3 ≅ 6 ms is lower than the non-repetitive charge time interval, T2–T1 ≅ 50 ms. This is because the capacitor is initially discharged and subsequently never discharges completely. At a steady state, the voltage drop across the CBS is around 60 mV when the power MOSFET is turned on. It reaches the value of 560 mV, which corresponds to the voltage drop of the intrinsic body diode, when the power MOSFET is turned off.

Finally, the proposed CBS was connected inside the junction box of a commercial PV panel, as illustrated in Fig. 10. The panel was made up of 72 cells grouped into three sections and was exposed to the sunlight. We preliminarily measured the temperature of one PV cell (belonging to the group of cells connected in parallel to the CBS) under normal sunlight exposure and subsequently under different shading levels. The temperature of the cell remained constant and about equal to 38ºC. The same performance under the same conditions was observed in one PV cell belonging to the group connected to the Schottky diode. Therefore, the CBS was found to be effective in preventing the hot spot effect.

IV. Conclusion

We presented the architecture of an active low-power bypass switch for use in photovoltaic panels that is able to profitably replace the traditional Schottky diodes. The solution does not require a dedicated power supply as it comprises a charge-pump that boosts the voltage drop across the parasitic drain-bulk diode of the power MOSFET switch. The proposed switch was prototyped by assembling three ICs (power MOSFET and control and boosting sections) into one package and was experimentally characterized. It was found to be effective in preventing the hot spot effects. Compared to two conventional Schottky diodes traditionally adopted in such applications, the cool bypass switch reduces the power consumption by more than 70% allowing the overall conversion efficiency of the panel to be increased. Moreover, since the working temperature of the bypass device is significantly lower, the mean lifetime of the device itself and overall reliability of the system are expected to be improved.

Despite the fact that the prototype was implemented as a system on a package, the proposed architecture is fully compatible with CMOS technologies and further work is aimed to integrate the whole system into a monolithic circuit.

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Salvatore Pennisi received the laurea degree in electronic engineering in 1992 and the PhD in electrical engineering in 1997, both from the University of Catania, Italy. In 1996, he became a researcher (assistant professor) and in 2002, he was appointed an associate professor at the same university. His main research interests include circuit theory and analog design with emphasis on low-voltage and current-mode techniques, multistage amplifiers with related frequency compensation, data converters, and the analysis of high-frequency distortion in analog circuits. More recently, his research activities have involved driving circuits and techniques for liquid crystal displays and circuits for efficient energy harvesting. He has published over 70 international journal papers, 120 conference proceedings, and is the co-author of the books *CMOS Current Amplifiers* (1999), *Feedback Amplifiers: Theory and Design* (2001) both edited by Kluwer Academic Publishers, and *Liquid Crystal Display Drivers: Techniques and Circuits* (Springer 2009). Dr. Pennisi

has served as an associate editor of the *IEEE Transactions on Circuits and Systems-Part II: Express Briefs* and is member of the IEEE CASS Analog Signal Processing Technical Committee.

Francesco Pulvirenti graduated in electronic engineering from the University of Pisa, Italy, in 1989. He joined STMicroelectronics in 1991, where he is currently the director of the Photovoltaic Business Unit with the mission to define and develop new application specific devices for Photovoltaic Market. He started as a design engineer spending ten years developing smart power ICs, linear regulators, switch mode power supply and power management, respectively, for industrial, mobile phone, battery charger, and computer applications. In 2001, he moved to the display segment to manage the design of new drivers dedicated to liquid crystal display applications for portable equipments. In 2004, he was appointed as design director of the Display Division. Francesco Pulvirenti holds more than 50 international patents on analog and smart power ICs. He is also co-author of 12 papers published in international conferences/magazines and co-author of the book *Liquid Crystal Display Drivers*: *Techniques and Circuits*, edited by Springer in 2009.

Amedeo La Scala received the laurea degree in electronic engineering in 1996 from the University of Palermo, Italy. In 1997, he joined STMicroelectronics, Catania, as a digital designer for set top boxes. In 2004, he moved to the Liquid Crystal Display Division, to develop display drivers for portable devices. Since 2008, he has worked on a new challenging activity for photovoltaic applications. In this context, he has contributed to the development of new products for efficient power extraction like the SPV1001 and SPV1020 devices.