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Transmission Line Analysis of Accumulation Layer in IEGT

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Abstract – Transmission line analysis of the surface accumulation layer in injection-enhanced gate transistor (IEGT) is presented for the first time, based on per-unit-length resistance and conductance of the surface layer beneath the gate of IEGT. Lateral electric field on the accumulation layer surface, as well as the electron current injected into the accumulation layer, is governed by the well-known wave equation, and decreases as an exponential function of the lateral distance from the cathode. Unit-length resistance and conductance of the layer are expressed in terms of the device parameters and the applied gate voltage. Results obtained from the experiments are consistent with the numerical simulations.

Keywords: IEGT, Accumulation layer, Surface potential, Transmission line analysis

1. Introduction

Injection-enhanced gate transistors (IEGTs) [1] are extensively used for high-voltage and -current applications that combine the best properties of gate turn-off thyristors (GTO) and insulated gate bipolar transistors (IGBT) devices. The surface accumulation layer beneath the gate of depletion-mode devices, such as vertical double-diffused MOS (VDMOS), spreads the majority carrier current from the thin surface layer into the bulk region of the device. Current flow changes from lateral to vertical direction along the length of the accumulated surface. The two-dimensional nature of this current flow should be regarded principally as a distributed structure. The surface layer of such a device is characterized, in general, by the accumulation layer resistance. An expression analogous to the channel resistance enhancement mode with a correction factor accounts for the effect of current spreading. Layer resistance plays an important role in total on-resistance of the device [2].

In IGBT and IEGT, both electrons and holes are injected in a very high level. This gives rise to the conductivity modulation with PiN diode-like carrier distribution inside the n-base region of the device. Electrons are injected through the accumulation layer, whereas holes are injected through the P-anode. The enhanced excess carrier density in the proximity of the accumulation layer by the action of the PiN diode plays a critical role in the on-state characteristics of the device [3]. A comprehensive understanding of the electron-injection mechanism of the accumulation layer is therefore of basic importance for the device design. One-dimensional models for IGBT have been presented in literature [4], and have been used to represent IEGT. A two-dimensional model [5] describing the static and dynamic behavior of IEGT or trench IBGT has also been reported. However, thus far, no analytical modeling has exposed a detailed current spreading of the accumulation layer.

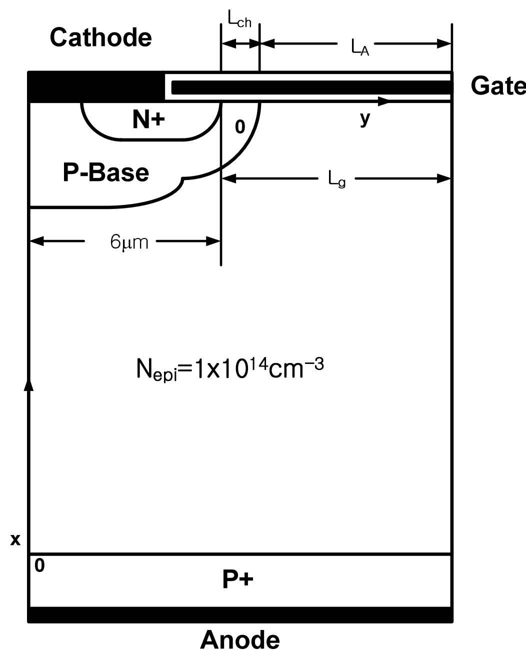

Fig. 1. Cross-section of a half unit cell of an IEGT with parameters

2. Simulation Results

A cross-section of the half-unit cell for IEGT with blocking capability of $600[V]$, N-epi drift region with fixed impurity concentration of $N_{epi} = 10^{14} / cm^3$, thickness of $95\mu m$, and total width of $(6 + L_g)\mu m$ used in the simulation is shown in Fig. 1, where the double-diffused p

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body region has a depth of $5\mu m$ and peak concentrations of $2\times10^{19} cm^{-3}$ and $1\times10^{17} cm^{-3}$ at the cathode contact and the inversion layer, respectively. The carrier lifetimes for the drift region are taken as $\tau_{n0}=\tau_{p0}=1\mu s$ with ambipolar lifetime of $\tau_a=2\mu s$. In the simulation, the device has a fixed channel length of $L_{CH}=2\mu m$ and an accumulation layer length of L_A that varies from $4\mu m$ to $48\mu m$, resulting in $L_g=L_A+L_{CH}$ for the gate length. The p+ anode has a thickness of $30\mu m$ and a uniform impurity distribution with a concentration of $5\times10^{18}/cm^3$.

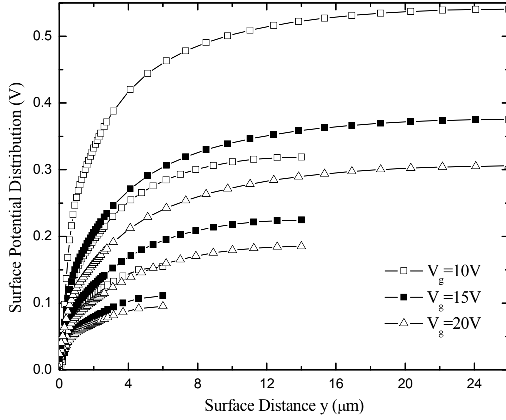

Fig. 2. Variation of surface potential along lateral path beneath gate of the device for a fixed gate length of $L_g=6,14, and 26[um]$ with gate voltage as a parameter

Fig. 2 shows the simulation results for the variation of the surface potential beneath the gate $V_s(y)$ as a function of the surface distance y measured from the n+ cathode $(y=0)$ for a fixed gate length of $L_g=6,14, and 26[um]$, with the gate voltage as a parameter. The variation of the surface potential is continuous, such that that no distinction between the inversion and accumulation layer could be identified, and such that the lateral electric field on the surface would decrease rapidly with increasing distance. This observation seems to contradict what can be expected for a MOS with an inverse layer, where the lateral field in the channel increases with increasing distance towards to the drain.

Gate-length dependence of the surface voltage drop $V_s(L_g)$ is found to increase linearly with increasing gate length, but to decrease with increasing gate voltage. The best fit for the linear relationship of $V_s(L_g)$ can be approximated by $V_s(L_g)=0.025+\gamma L_g$ where $\gamma=20.8\times 10^{-3}$ and $11.76\times10^{-3}(\mu m^{-1})$ for $V_g=10$ and $20[V]$, respectively, and L_g in [μm]. This indicates that the surface voltage drop contributes substantially to the total forward voltage drop of the device, especially when the gate length increases.

Fig. 3 shows the surface potential $V_s(y)$ as compared with potential variation at 0.3 [μm] below the surface $V_w(y)$, along the lateral path of n+ cathode p body N_{EPI},

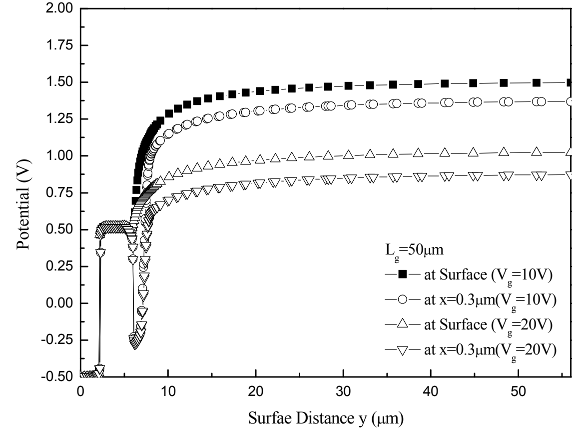

Fig. 3. Comparison of surface and bulk potential variation along lateral path beneath gate for a fixed gate length of $L_g=50[um]$ at $V_g=10[V]$ and $V_g=20[V]$

where the condition for conductivity modulation with an nearly equally high level of electron and hole densities over their equilibrium values in the bulk drift region of IEGT is satisfied. Here, $V_s(L_g)=1.5[V]$ at the gate edge surface and $V_w(L_g)=1.36[V]$ at the bulk region below the surface for $V_g=10[V]$. Thus, a reverse-voltage drop of $\Delta V=0.14[V]$ occurs on the gap of the thickness $\Delta t=0.3[\mu m]$ for an accumulation layer between the semiconductor surface and the bulk drift region. The corresponding reverse-voltage drop of $\Delta V=0.15[V]$ is $V_g=20[V]$. This reverse-voltage drop acts as a potential barrier for holes and prevents them from flowing into the accumulation layer.

Simulation results for the lateral electron current density variation $J_s(y)$ are shown in Fig. 4, with the gate length as a parameter. Note that $J_s(y)$ decreases exponentially along the lateral path on the surface of the accumulation layer.

3. Analysis and Discussions

An L-type equivalent circuit model for the incremental portion of length Δy in the accumulation layer is shown as an inset in Fig. 4. The layer parameters R and G are the resistance and the conductance on a per-unit-length basis. A two-dimensional nature of the accumulation layer is clearly presented. Electron current at y along the lateral path of the accumulation layer satisfies $I_s(y)= I_s(y+\Delta y)+I_n(y)$, which for the limit of $\Delta y\to0$, yields $I_n(y)\cong-(\partial I_s/\partial y)\Delta y$, with $I_n(y)$ for the vertical electron current flowing into the accumulation layer:

$$I_n(y)=J_n(y)W\Delta y=G\Delta yV_{dr} \tag{1}$$

where W is the width of the device ($W=1\mu m$ in the simulation), $J_n(y)$ is the vertical electron current density

flowing into the accumulation layer, and $V_{dr} = V_a - V_s(y)$ with V_a for the voltage at the position. The total current density begins to decrease in the proximity of the layer from the value fixed at the anode. Here, V_a may be approximated from the difference in voltage drop on the drift region from the total forward voltage drop of the device [6].

The above relation thus gives

$$\partial I_s / \partial y = -GV_{dr} = -WJ_n(y) \tag{2}$$

Considering the surface potential drop on the incremental length Δy of the accumulation layer, we obtain

$$E_s(y) = -\partial V_s / \partial y = -RI_s(y) \tag{3}$$

Combining Eqs. (3) and (2) leads to

$$\partial E_s(y) / \partial y = WRJ_n(y) \tag{4}$$

Taking the second derivative of I_s in Eq. (2) and applying it to Eq. (3), we obtain the well-known wave equation:

$$\partial^2 I_s / \partial y^2 - \alpha^2 I_s = 0 \tag{5}$$

which is the same equation that could be employed to V_d. In Eq. (5), $I_s(y) = I_{MOS}e^{-\alpha y}$ with $I_{MOS} = I_s(0)$ for the total electron current, and $\alpha = \sqrt{RG}$, the decaying constant for the electron current of the accumulation layer.

From Eq. (2), we obtain

$$\partial J_n(y) / \partial y = (G/W)E_s(y) \tag{6}$$

where $E_s(y)$ is the lateral surface field and $J_n(y)$ is the vertical electron current density coupled in Eqs. (4) and (6) that lead to the wave equation given in Eq. (5). Thus, the solutions can be presented as $E_s(y) = E_0e^{-\alpha y}$ and $J_n(y) = J_0e^{-\alpha y}$ with $E_0 = E_s(0)$ and $J_0 = J_n(0)$, respectively. Substituting these equations in Eq. (4) or (6) leads to $J_0 = -g(E_0/W)$, where $g = \sqrt{G/R}$. The lateral surface field given above allows expressions for the surface electron current, as well as the surface potential:

$$I_s(y) = -W\mu_{ny}\sigma_s E_s(y) \tag{7}$$

$$V_s(y) = -(E_0/\alpha)(1 - e^{-\alpha y}) \tag{8}$$

where μ_{ny} is the effective electron mobility in the lateral direction of the layer and $\sigma_s \cong C_{OX}[V_g - V_T][C/cm^2]$ is the induced charge density on the semiconductor surface C_{OX} for the capacitance per unit area of the gate oxide and V_T for the accumulation layer threshold voltage.

Combining Eqs. (3) and (7) gives an expression for the unit-length resistance of the layer:

$$R = 1/[W\mu_{ny}\sigma_s][\Omega/cm] \tag{9}$$

where $R = 4.83$ and 2.63 in $[k\Omega/\mu m]$ are obtained using $C_{OX} = 34.52[nF/cm^2]$ and $V_T = -2[V]$ for the present device at $V_g = 10$ and $20[V]$, respectively when $\mu_{ny} = 500[cm^2/Vs]$, which is close to the value for the inversion layer.

Integrating Eq. (4) from $y = 0$ to $y = L_g$ results in $[E_s(L_g) - E_s(0)] = RI_{n,tot}$ where $I_{n,tot} = W\int J_n(y)dy = I_s(0) - I_s(L_g)$ is the total electron current flowing into the accumulation layer from Eq. (2). The result gives a useful expression for the lateral conductance of the layer defined for electron current:

$$g \equiv I_{n,tot} / V_s(L_g) \tag{10}$$

where $V_s(L_g)$ is given in Eq. (8). As long as the condition of $1 >> e^{-\alpha L_g}$ is assumed valid, $I_s(0) = I_{MOS} \cong I_{n,tot}$ may lead to $g = I_{MOS}/V_s(L_g) = \sqrt{G/R}$.

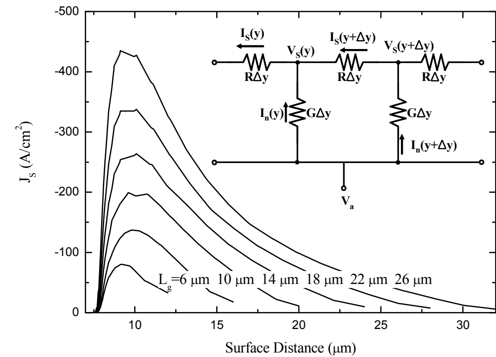

Fig. 4. Lateral component of electron current density along lateral path on semiconductor bulk surface beneath gate at $V_g = 15[V]$ with gate length as a parameter

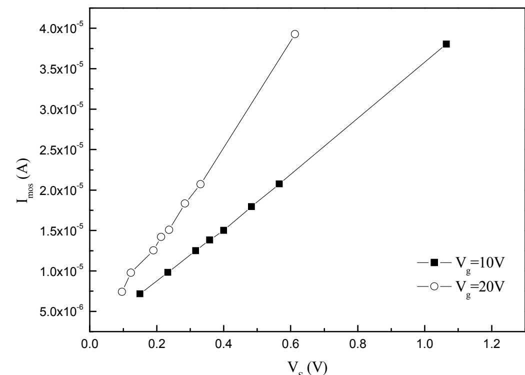

Fig. 5. Total electron current injected into the accumulation layer as a function of total surface potential drop at $V_g = 10[V]$ and $V_g = 20[V]$

Fig. 5 shows the linear relationship between $V_s(L_g)$ and I_{MOS} obtained from the simulation results, yielding $g = 34.6$ and $65.7[\mu\Omega^{-1}]$ for $V_g = 10$ and $20[V]$, respectively. Using the given values for g and R, the above relation gives $\alpha \cong 0.17[\mu m^{-1}]$ for both $V_g = 10$ and $20[V]$ independent of the applied gate voltage. This value of α is very close to the decaying constant of the lateral electron current, $\alpha \cong 0.16[\mu m^{-1}]$ from Fig. 4. A rapid increase of the surface potential at the very beginning of increasing distance, as shown in Fig. 2, is consistent with the analytic result from Eq. (8).

The corresponding values for the unit-length conductance of the layer are $G = \alpha g = 5.8$ and 11.4 $[\mu\Omega^{-1} / \mu m]$ for $V_g = 10$ and $20[V]$, respectively.

A simplified analytical expression for G may be obtained by considering the current density $J_n(y) = qn_{eff}\mu_{sx}E_n$. Here, μ_{sx} is the surface electron mobility in the vertical direction of the layer and $E_n = \Delta V / \Delta t$ with the potential barrier ΔV underneath the accumulation layer and gap $\Delta t = 0.3\mu m$ wherein the hole current component vanishes, such that $G = qn_{eff}\mu_{sx}W / \Delta t$. Thus, the electron density at Δt below the surface to be related to $n_0 = n_s \exp(-\Delta V / v_T)$ of density $n_s = \sigma_s / q\Delta t$ at the semiconductor surface and thermal voltage, v_T. The value of $n_{eff} = (\sigma_s / q\Delta t)\exp(-\Delta V / 2v_T)$ is used to yield

$$G = [\sigma_s W \mu_{sx} / (\Delta t)^2] \exp(-\Delta V / 2v_T) \quad (11)$$

where the values of G correspond to $\mu_{sx} \cong 19[cm^2 / V \cdot s]$ for both $V_g = 10$ and $20[V]$, exhibiting very small electron mobility in the vertical direction of the accumulation layer. The value $V_s(y)$ can now be computed using Eq. (8) with $E_0 = -RI_{MOS}$, which decreases with increasing gate voltage through R, and increases with increasing gate length through linear dependence [7] of I_{MOS} on L_g when the total current density at the anode junction is fixed at $100[A/cm^2]$. This observation agrees with the simulation result on surface potential shown in Fig. 2.

5. Conclusion

In conclusion, transmission line analysis of the accumulation layer exhibits two-dimensional current that spreads as a natural consequence through the layer. Unit-length resistance and conductance in the accumulation layer, presented in terms of gate length and voltage, allow calculation of the decaying constant for both the electron current and the surface field of the layer, as well as the lateral conductance of the layer. Lateral conductance of the accumulation layer is defined as the ratio of the total electron current to the total surface potential drop of the layer. . Hence, the analytical results are consistent with the simulation results, suggesting that the accumulation layer of an IEGT can be applied to both conventional IGBT and VDMOS design calculations.

Acknowledgements

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