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Design of UHF CMOS Front-ends for Near-field Communications

Sotoudeh Hamedi-Hagh*, Maryam Tabesh, Sooseok Oh*, Noh-Joon Park*** and Dae-Hee Park†**

Abstract – This paper introduces an efficient voltage multiplier circuit for improved voltage gain and power efficiency of radio frequency identification (RFID) tags. The multiplier is fully integratable and takes advantage of both passive and active circuits to reduce the required input power while yielding the desired DC voltage. A six-stage voltage multiplier and an ultralow power voltage regulator are designed in a 0.13 μm complementary metal-oxide semiconductor process for 2.45 GHz RFID applications. The minimum required input power for a 1.2 V supply voltage in the case of a 50 Ω antenna is -20.45 dBm. The efficiency is 15.95% for a 1 MΩ load. The regulator consumes 129 nW DC power and maintains the reference voltage in a 1.1% range with V_{dd} varying from 0.8 to 2 V. The power supply noise rejection of the regulator is 42 dB near a 2.45 GHz frequency and performs better than -32 dB from 100 Hz to 10 GHz frequencies.

Keywords: Low-power voltage multipliers, Passive UHF RFID transponders, RF–DC conversion

1. Introduction

Radio frequency identification (RFID) is applied in supply chain management, access control, public transportation, library checkout, and airport baggage control. To cover more applications, the need for high volume, low cost, small size and large data rate is increasing; stringent regulation of transmission power and bandwidth also have to be met [1]. Furthermore, interest in the integration of smart tags into sensor networks is growing. These systems require a wide range of operation (preferably above 10 m) without the use of a battery for cost efficiency. In such sensor networks, high-data-rate transmission is desirable to achieve low duty cycle operation and to increase the throughput efficiency of the system [2].

New RFID transponders are designed using the 2.45 GHz frequency band, which allows the use of smaller power coupling structures, such as antennas, as well as higher data rates due to larger available bandwidths. The reduced effective isotropic radiated power (EIRP) from regulations and the increased loss from the Friis equation make the maximum attainable range a major issue in this band. Therefore, the design of efficient voltage multipliers with the minimum number of stages for providing sufficient output power and voltage levels is the ultimate objective in the design of new RFID transponders.

† Corresponding Author: Dept. Of Electrial Electronics & Information Engineering, Wonkwang University, Korea (parkdh@wku.ac.kr)
* RFIC Research Lab, San Jose State University (hamedi@email.sisu.edu, sooseokoh@gmail.com)
** University of Calfornia at Berkeley (tabesh@eecs.berkeley.edu)
*** Center for Advanced Electric Application, Wonkwang University, Korea (njpark@kilt.re.kr)
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The main goal of the present paper is to design a transponder with increased reading distance using a new voltage generator topology. The technology used is a standard six-metal 0.13 μm digital complementary metal-oxide-semiconductor (CMOS) process with low-threshold transistors. The designed CMOS RF–DC converter generates high supply voltage levels from a very low incident RF power, and the designed low-power voltage regulator generates constant supply voltage, which is suitable for the rest of the circuits of the RFID system.

2. Architecture

The block diagram of an RFID system is shown in Fig. 1. The antenna and the voltage multiplier must be matched to ensure the maximum power transferred between the two blocks. The voltage multiplier converts the incoming RF signals to a DC voltage that will serve as the power supply for other blocks. The DC voltage is stored across a large on-chip capacitor. The capacitor, which acts as an energy storage element, must be completely charged within a short time interval to ensure that a proper V_{dd} is provided for the rest of the circuits.

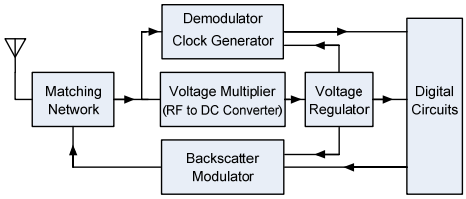

Fig. 1. Block diagram of an RFID system

The series voltage regulator in the RFID system generates a constant DC voltage independent of the power at the antenna and of the power consumption of the transponder. To prevent decreasing the overall power efficiency of the RFID front-end, the voltage regulator must have an extremely low power consumption.

The demodulator in the RFID system converts the pulse-width modulated input signal into digital data and generates synchronous system clocks. After the data is processed in the digital section, the modulator unit applies phase-shift keying (PSK) modulation on baseband signal and transmits the information signal through antenna using backscattering.

3. RF–DC Converters

The voltage multiplier circuit of an RFID system converts the received input signal to a stable DC voltage. The schematic of the voltage multiplier, which consists of six peak-to-peak detectors, is shown in Fig. 2. One of the most important factors in the design of RF–DC converters in RFID systems is the minimum required DC voltage to ensure proper operation of the digital and analog circuits. Given the range specifications and the power level requirements in the 2.4 GHz band, as stated by the Federal Communications Commission, the required DC voltage level determines the number of stages in the voltage multiplier circuit. The use of double polarity supply voltage circuits ($\pm V_{dd}/2$) instead of single polarity (V_{dd} and ground) supply voltage circuits decreases the required input signal level by half. The voltage level (V_{rf}) of the RF signal at antenna is given by

$$V_{rf} = \sqrt{8P_r R_{ant}} \tag{1}$$

where P_r is the received power at the antenna and R_{ant} is the equivalent antenna impedance.

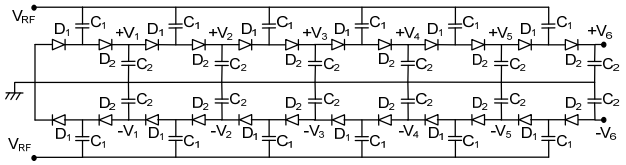

Fig. 2. Six-stage voltage multiplier circuit

The power efficiency of the voltage multiplier describes how much power is lost during the RF–DC conversion process. This efficiency depends on the number of stages, the performance of the diodes, and the input power of the multiplier. A decrease in the input power level of the voltage multiplier reduces efficiency and significantly lowers the output voltage. For diode-based multipliers, the efficiency is described by [3]

$$\eta = \frac{V_{dd} I_{laod}}{2nI_s V_p B_1(\frac{V_p}{V_T}) \exp(\frac{-V_{dd}}{2nV_T})} \tag{2}$$

where V_{dd} is the generated output DC voltage, I_{laod} is the output DC current, I_s is the saturation current, V_p is the peak of the input signal, V_T is the thermal voltage, n is the number of stages, and $B_1(x)$ is the first-order modified Bessel function.

The ratio of the DC output of the voltage multiplier to the input RF signal determines the impedance transformation, which is also affected by the loss factor of the voltage multiplier. The value of the load resistance R_{load} at the output of the multiplier can be obtained from the supply voltage and power consumption of the baseband circuits connected to the output of the voltage multiplier. The input impedance R_{in} of the voltage multiplier can be calculated when R_{load} and the current and voltage ratios of the voltage multiplier circuit are known. For most cases, R_{in} and the effective antenna resistance R_{ant} are not equal. This inequality mandates the use of a matching network between the antenna and the voltage multiplier. Another factor in designing the voltage multiplier is the time constant associated with the discharge of the capacitors. This time constant must be sufficiently larger than the signal period to ensure that the change in the supply voltage caused by transistor activity in the digital circuits remains minimal.

3.1 Functionality

The first stage of the voltage multiplier receives a 2.4 GHz RF signal with a 0 DC voltage, thereby generating a low DC voltage. Therefore, the input of the other stages of the voltage multiplier consists of both RF and DC voltages. As the RF signal moves toward the last stage of the voltage multiplier, it adds to the magnitude of the DC voltage, enabling it to be used as the supply voltage for the rest of the transistors in an RFID circuit.

A single-stage voltage multiplier is designed by replacing diodes with diode-connected transistors, as shown in Fig. 3. When the input signal is in the negative cycles, the voltage V_{c1} across capacitor C_1 is charged through the M_1 diode to the peak of the input signal. In the positive cycles, M_1 is OFF and M_2 rectifies the voltage sum of the V_{c1} and V_{in}.

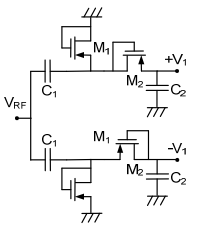

Fig. 3. Schematic of the first stage of the voltage multiplier

This produces a DC voltage (V_1) equal to twice the peak of the input signal (V_p) minus the ON voltage drop (V_D) across the two diode-connected transistors.

The output voltage provided by the voltage multiplier can be expressed by

$$V_n = 2n(V_{in} - V_D) \tag{3}$$

where n is the number of stages. In conventional voltage multiplier circuits, RF signals of different stages are equal to the input RF signal (considering the matching network effect). Increasing the input signal V_P using resonance-boosting methods significantly increases the output voltage V_n.

3.2 Resonance boosting of the voltage multiplier

A novel technique to increase the RF signal level is to use passive tuned elements at the input of the voltage multiplier. This technique does not introduce extra loading on the multiplier stages, and does not need any biasing current due to the elimination of subthreshold amplifiers. The voltage (V_c) across the capacitor C of a simple series RLC circuit is given by

$$V_C = \frac{I}{j\omega C} = \frac{V_{in}}{R + j\omega L + (j\omega C)^{-1}} \cdot \frac{1}{j\omega C} \tag{4}$$

At the resonance frequency, the impedance of the RLC circuit becomes equal to the resistance R, and the voltage across the capacitor becomes

$$V_c = jV_{in}Q \tag{5}$$

where Q is the quality factor of the series RLC circuit. This analysis shows that if an RC circuit is connected to a source, the RF signal across the capacitor can be boosted by a factor of Q if a series inductor is placed between the source and the load. This inductor is provided by the antenna and helps increase the output voltage of the voltage multiplier circuit, which can effectively be modeled by a small-signal RC circuit, as shown in Fig. 4.

The series input capacitance and resistance of the small-signal models in negative and positive input cycles can be extracted using parallel–series transformation. The addition of an inductor to the input of the voltage multiplier circuit improves the gain of the voltage multiplier. The simulation result of the single-stage voltage multiplier with an input power of -19.5 dBm with and without the resonating antenna inductor is shown in Fig. 5. When the antenna inductor is used for voltage boosting, the output DC voltage of the multiplier increases by a factor of 4.2.

The input capacitance and resistance of the multistage voltage multiplier circuit are derived to obtain the optimum value of the inductance used for the passive multiplication

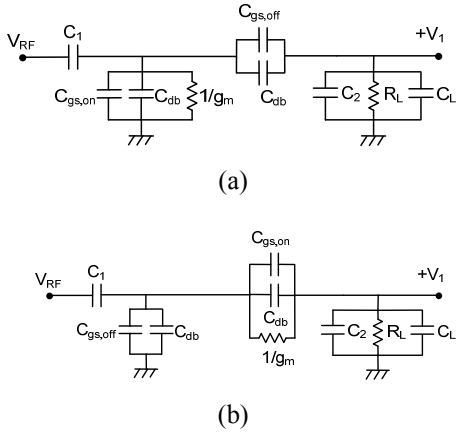

Fig. 4. Small-signal model of single-stage voltage multiplier: (a) negative input cycles; (b) positive input cycles

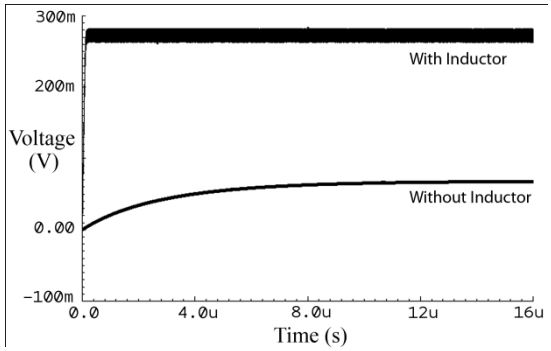

Fig. 5. First-stage output of the voltage multiplier with and without Inductor

of the six-stage voltage multiplier. A differential inductor is used to boost the positive and negative supply voltages. This differential inductor yields 3.8 nH with a Q of 26 at 2.45 GHz. It is designed using the top metal layer realized over the polysilicon pattern ground shield. The gain at the input of the voltage multiplier circuit after the addition of the inductors is shown in Fig. 6.

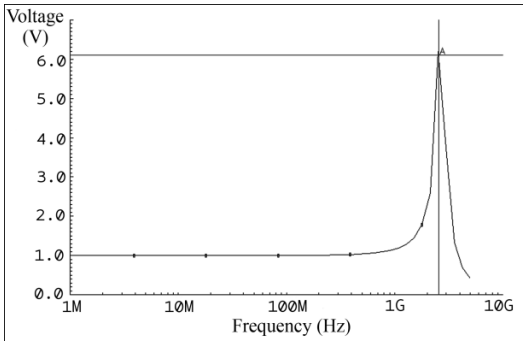

Fig. 6. Voltage gain after antenna inductor

Input impedance matching is one of the challenges in the design of conventional voltage multiplier circuits for RFID applications. In the proposed topology, the series inductor

helps in bringing the input impedance R_{in} closer to the 50 Ω of the antenna. The voltage multiplication and impedance transformation are achieved at the same time because of the embedded LC-matching network.

4. Regulator

The output voltage of the multiplier circuit is dependent upon the input signal level at the antenna, and fluctuates with the distance between the transmitter and receiver antennas. A voltage regulator is required to maintain constant supply voltage for proper operation of the analog and digital circuits. Because of limited power availability, the regulator in RFID systems must be extremely power efficient and work with low current levels. Furthermore, the regulator must have a very good power supply noise rejection (PSNR) to filter out the supply voltage fluctuations. The schematics of the reference voltage generator and the series voltage regulator are shown in Fig. 7. A start-up circuit is used in the reference voltage generator to ensure proper operation of the regulator [4].

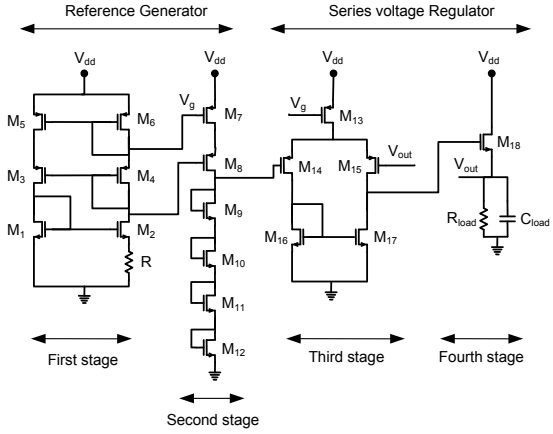

Fig. 7. Voltage regulator circuit

The reference voltage generator uses a self-biased current reference to drive the current into a stack of diodes. These diodes are realized using low-threshold transistors, and present a voltage at the input of the series regulator. The self-biased current source consists of a cascode PMOS current mirror stacked on top of a Widlar current source. The current mirror circuit operates in the subthreshold region for low-current and low-power operations. The output current I_{out} of the current mirror can be obtained using the general V_{gs} equation in the subthreshold region as follows [5]:

$$I_{out} = \frac{nV_T}{R}\ln\left(\frac{(\frac{W}{L})_2}{(\frac{W}{L})_1}\right) \quad (6)$$

The cascode current mirrors increase the output resistance; therefore, they are less susceptible to current mismatches between transistor pairs. Based on Eq. (6), to reduce I_{out}, either resistance R can be increased or the width-to-channel length ratio of the transistors can be selected close to unity. Although the latter seems attractive in terms of layout area reduction and matching improvement, it may not be a desirable choice in terms of the sensitivity of I_{out} to this ratio, which can be calculated from the following equations in the subthreshold region:

$$V_{gs} = V_{th} + nV_T\ln\left(\frac{I_{out}}{(\frac{W}{L})I_t[1-\exp(-\frac{V_{ds}}{V_T})]}\right) \quad (7)$$

and

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\ln\left(\frac{1-\exp(-V_{ds,2max}/V_T)}{1-\exp(-V_{ds,2min}/V_T)}\right)}{\ln\frac{(W/L)_2}{(W/L)_1}} \quad (8)$$

where $V_{ds,2}$ is the drain-source voltage of M_2 given by

$$V_{ds,2} = V_{dd} - 2V_{diode} \quad (9)$$

A large value of the resistor R is selected to decrease I_{out}, and the W/L ratio is chosen to yield minimum sensitivity.

The last two stages of the voltage regulator involve a differential amplifier with feedback. The feedback senses the output voltage and compares it with the V_{ref} provided by the voltage reference of the second stage. The PSNR of the circuit is determined by the voltage division between R_{load} and $R_{ds,18}$.

5. Results

The hybrid six-stage multiplier and regulator have been designed using a 6-metal 0.13 μm digital CMOS process with a modified PDK that has been precisely characterized initially using RF test structures. Both polarities of the supply are available, and all circuits are designed using double polarity supplies. A differential inductor is used to provide the passive multiplications for the two double-polarity supply voltage circuits, as shown in Fig. 8. The layout is 0.7×1.17 mm^2.

The minimum input voltage required to obtain a 1.2 V DC voltage at the output of the six-stage multiplier used in the present work is 60 mV (peak), which corresponds to -20.45 dBm incident power at the antenna. The output DC voltage of the voltage multiplier with a 1 MΩ load, with respect to the received power at the antenna, is shown in Fig. 9.

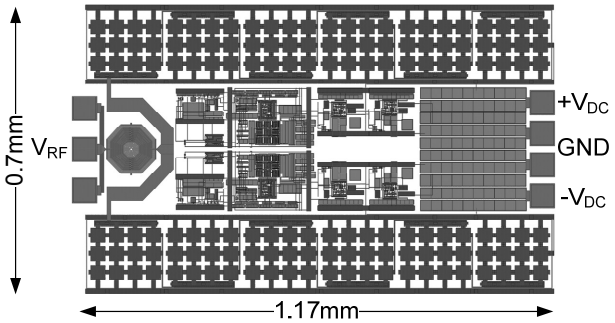

Fig. 8. Layout of the multiplier and regulator

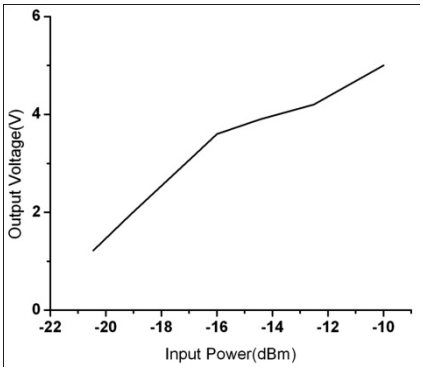

Fig. 9. Output voltage of the multiplier as a function of the input power

The DC voltage generated at the output of different voltage multiplier stages, as well as the settling time and behavior of the output voltage of the six-stage multiplier, are illustrated in Figs. 10 and 11 for an input power of -19.1 dBm and 1 MΩ load.

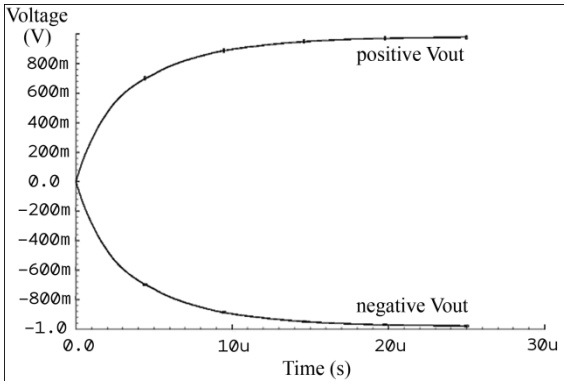

Fig. 10. Output voltage of the multiplier for an input power of -19.1 dBm and R_{load} of 1 MΩ

The DC output voltage of the multiplier as a function of the load presented by the circuit is shown in Fig. 12. The power efficiency of the voltage multiplier circuit is 15.95% from an input power of -19.1 dBm at 1.2 V DC voltage and 1 MΩ effective load resistance obtained from the average current consumption of the digital circuits.

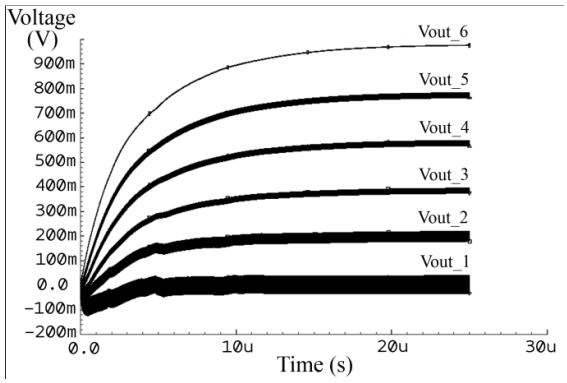

Fig. 11. Output voltage at different stages of the multiplier

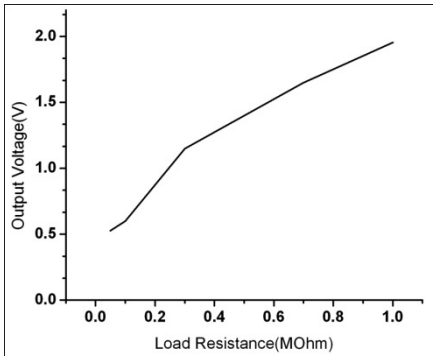

Fig. 12. Output voltage as a function of the load resistance

The provided measurement results and simulation graphs of the present work match closely due to accurate calibration of the CMOS PDK prior to the design. In comparison with the design in Ref. [2], which reported an efficiency of 11%, the efficiency of the design presented in the current paper is enhanced by 5%, and the minimum input power for a 3 V rail–rail DC generation is improved by 42 μW (20.25 μW compared to the reported 63 μW in [2]). The performance comparison of the proposed RFID front-end and the best extant designs is shown in Table 1. The operation ranges of the RFID circuits are expressed in terms of wavelengths instead of frequency for a better evaluation.

Table 1. Performance comparison of RFID voltage multipliers

Ref.	Efficiency	Min. Input Power to Generate 3V	Range
This work	15.95%	20.25μW	37.6 λ
[2]	10.94%	63 μW	21.32 λ
[1] Schottky diodes	14.5%	_	28.2 λ

The regulator consumes 129 nW with a PSNR of -42 dB at the desired frequency. The PSNR of the regulator as a function of frequency is shown in Fig. 13.

The performances of the regulator in terms of the variations in the reference voltage and current with the

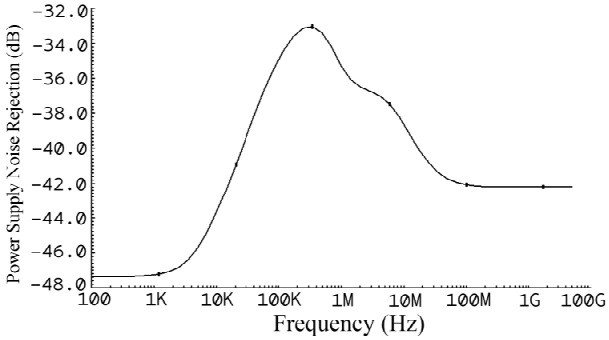

Fig. 13. PSNR of the regulator

change of V_{dd} are shown in Figs. 14 and 15. The regulator presented here is designed to provide a constant 1 V voltage or approximately 0.5 V on each side, regardless of the input power variation.

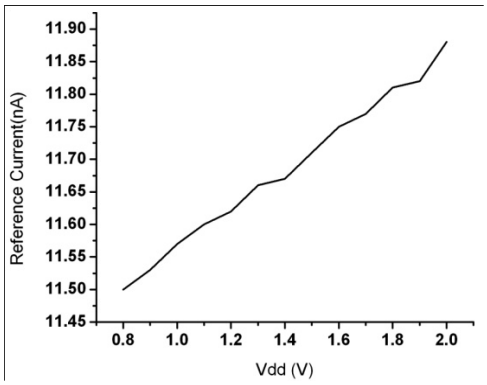

Fig. 14. Reference current as a function of DC voltage variation

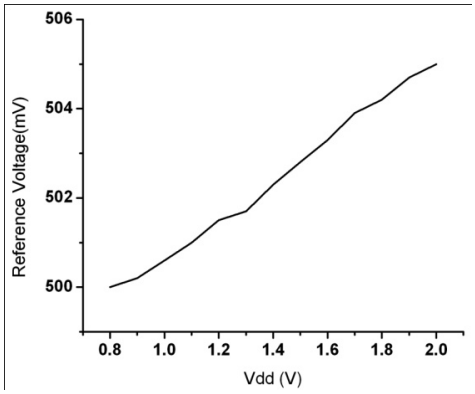

Fig. 15. Reference voltage as a function of DC voltage variation

6. Conclusion

A new architecture for an efficient RF–DC voltage multiplier circuit used in a batteryless RFID transponder has been presented in the present paper. Although the application described in the present paper is mainly focused on RFID tags, the architecture could be used elsewhere, such as in remote sensors or biomedical implants. The circuit was designed in a 0.13 μm digital CMOS process, resulting in a total efficiency higher than 15.95% when presented with an effective load of 1 MΩ.

Acknowledgment

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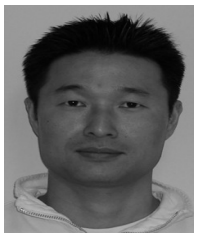
Sotoudeh Hamedi-Hagh was born in Tehran, Iran in 1970. He received his BASc degree in Electrical Engineering from Iran University of Science and Technology, Tehran in 1993, and the MASc and PhD degrees in Electrical and Computer Engineering from the University of Toronto, Toronto, ON, Canada in 2000 and 2004, respectively. He joined the faculty of San Jose State University in 2005 and became an Associate Professor in 2011. He has established and directed the radio frequency integrated circuits lab and curriculum in the Electrical Engineering department. His research interests include high-frequency modeling of planar and 3-D device structures and design of RF and mixed-signal integrated circuits for wireless communication systems using silicon technologies. Dr. Hamedi-Hagh was the recipient of the Best Paper Award at the 2000 Canadian Micronet and the 2004 IEEE Personal, Indoor, and Mobile Radio Communication conferences. He holds two US patents

Maryam Tabesh received her BS degree in Electrical Engineering from Sharif University of Technology, Tehran, Iran in 2005, and her MS degree from San Jose State University, San Jose, CA in 2007. She is currently working toward a PhD degree at the University of California at Berkeley. In 2004 and 2005, she was a Technical Advisor for the Electronic Research Center (ERC) of the Iran University of Science and Technology (IUST) on the feasibility study plan and implementation guideline report for data access to rural and remote parts of the country. During the summer of 2007, she was a Design Engineer with HMicro Inc., Los Altos, CA, where she was involved with RF circuit and antenna design for low-power wireless modules. She is currently an active member of the Berkeley Wireless Research Center (BWRC) at the University of California, Berkeley. Her research interests include microwave and millimeter-wave circuits and phased array systems. Ms. Tabesh was the recipient of the 2006–2007 Society of Women Engineers (SWE) Scholarship and the 2007 Alfred Dixon Memorial Scholarship.



Sooseok Oh received his MS degree in Electrical Engineering from Mississippi State University, MS, USA in 2000. From 2000 to 2006, he was a Circuit Design Engineer in the Microprocessor Development Group, Intel Corporation, Santa Clara, California. He has since been with Silego Technology, Santa Clara, CA working on analog/mixed-signal design for CMOS PLL clock products. He is currently working toward his PhD degree through the Gateway PhD program at San Jose State University and Mississippi State University. His main research activities are focused on analog and radio frequency integrated circuits.

Noh-Joon Park was born in Seoul, Korea in 1968. He received his BS, MS, and PhD degrees in Electronics Engineering from Wonkwang University in 1993, 1995, and 2004, respectively. In 2006, he worked as Research Professor with the Center for Advanced Electric Applications at Wonkwang University, focusing on the design and analysis of EM sensors for partial discharge diagnosis in high-voltage engineering, and on the electronic circuit design for light sources. He joined the Korea Institute of Lighting Technology in 2011, where he is currently employed as a Senior Research Engineer. His research interests are in the areas of LED devices for agriculture and medical application, CMD, power IT, antenna system, channel measurements, and others. He is a member of the KIEEME, KIEE, KIIEE, KICS, KIMICS, KIEES, and IEEK.

Dae-Hee Park was born in 1954 in Korea. He received his BS and MS degrees in Electrical Engineering from Hanyang University, Seoul, Korea in 1979 and 1983, respectively. He obtained his PhD degree from Osaka University, Osaka, Japan in 1989. He worked at the LG Cable Research Institute as a Senior Researcher from 1979 to 1991. He then joined the School of Electrical, Electronics and Information Engineering at Wonkwang University where he is currently employed as Professor. He has also worked as the Director of the "Center for Advanced Electric Application" from 2004 at Wonkwang University. He was at MSU, USA, as a Visiting Professor from 1999 to 2000. He served as the chairman of the College of Engineering in Wonkwang University from 2009 to 2010. He currently serves as the chairman for the next term of Korean IEEME. He also serves as the Chairman of the Organizing Committee of the First International Conference on Advanced Electromaterials. His main research interests are in the areas of insulating materials, CMD, LED light sources, and its applications. He is a member of the KIEEME, KIEE, IEEE and IEEJ.