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Single-Stage Double-Buck Topologies with High Power Factor

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Abstract

This paper presents two topologies for single-stage single-phase double-buck type PFC converters, designed to operate at high power factor, near sinusoidal input currents and adjustable output voltage. Unlike the known buck type PFC topologies, in which the output voltage is always lower than the maximum input voltage, the proposed converters can operate at output voltages higher than the ac input peak voltage. A reduced number of switches on the main path of the current are another characteristic of the two proposed topologies. To shape the input line currents, a fast and robust controller based on a sliding mode approach is proposed. This active non-linear control strategy, applied to these converters allows high quality input currents. A Proportional Integral (PI) controller is adopted to regulate the output voltage of the converters. This external voltage controller modulates the amplitude of the sinusoidal input current references. The performances of the presented rectifiers are verified with experimental results.

Key Words: High power factor, Buck rectifier, Single-phase, Sliding mode controller, Power converter

I. Introduction

The use of industrial and consumer electronic equipment with ac to dc high- frequency switching converters as power supplies has significantly increased in the last few years. Line frequency switched ac to dc power supplies feature simple diode rectifiers needing large dc link capacitors. Diode rectifiers present high harmonic content in the input currents, leading to low input power factor and causing line voltage harmonics and transient disturbances [1], [2]. Therefore, to reduce the impact of the harmonic current injection on the ac network, new standards such as IEEE-519 and IEC 61000-3 have emerged.

To comply with the new standards, high frequency switching mode ac/dc converters with pulse-width modulation (PWM) have been developed. The input current modulation process enables high power factor and minimum harmonic distortion, thus obtaining high quality input currents (close to sinusoidal waveforms) with near unity input power factor. The dominant design of the PWM ac/dc converters, known as power factor correctors (PFC), is the Boost type [3]–[6]. This voltage-source ac-dc converter, which can also be used as inverter, has an ac input filter. As a step-up converter it presents a dc output voltage higher than the ac voltage peak voltage value. Output voltages lower than this value can only be obtained using additional converters or transformers, when using a PFC boost converter. Another disadvantage of the boost type is their inability to limit the switch –on inrush current or the dc-short-circuit current.

Unlike the boost type ac-dc PFC converter, the buck type PFC has the capability to limit the inrush and dc short-circuit currents, but has step-down characteristics, since the output voltage of the rectifier is always lower than the peak voltage value of the input ac sources [7]–[10]. The step-down action can prevent the use of the buck design in some applications. Another disadvantage of buck type PFC design, when compared to the Boost type PFC, is the low efficiency since they usually have a high number of power semiconductors in the ac input current path.

To contribute in overcoming these drawbacks, section II of this paper presents two topologies for single-stage single-phase buck type PFC converter in which the output voltage can be extended beyond the ac input-voltage peak value. Additionally, it is possible to improve the efficiency of these double buck rectifiers, since the number of power semiconductors in the input current path has been reduced. The double buck rectifier operation is presented in section III. The control method (section IV) for the proposed Buck-type ac-dc converter uses a cascade structure. For the inner loop, an input current controller based on a sliding mode approach is proposed. The external voltage control loop includes a proportional plus integral (PI) compensator. To provide near sinusoidal input

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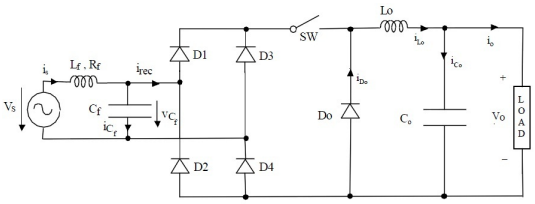
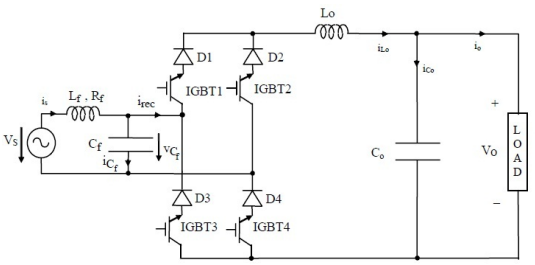
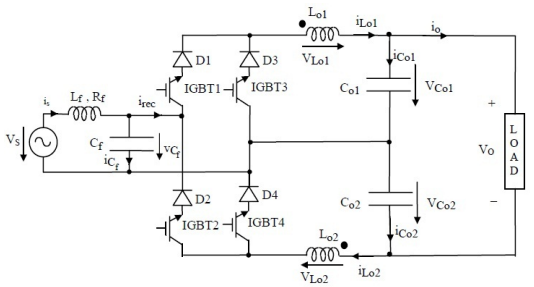


(a) With one turn-off switch.

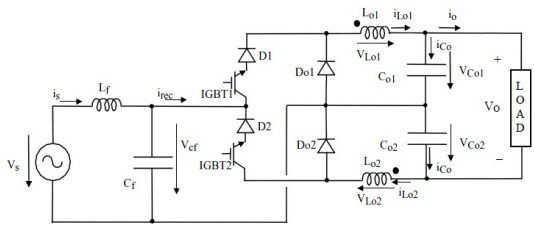


(b) With four turn-off switches.

Fig. 1. Typical single-phase Buck type ac-dc converter topologies.



(a) With four turn-off switches.



(b) With only two turn-off switches.

Fig. 2. Proposed single-phase Buck type ac-dc converter topologies.

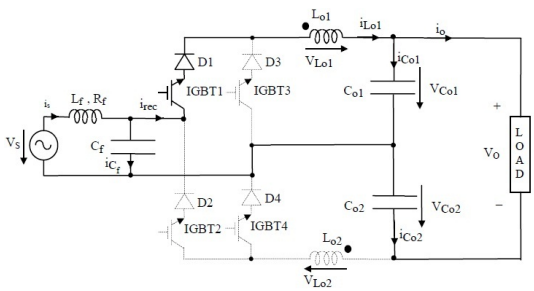


Fig. 3. First stage topologies.

currents, the external loop voltage controller output is the reference amplitude of the sinusoidal current which is the reference of the inner current mode loop. Experimental results from an experimental laboratory set up are presented and discussed (section V).

II. Converter Topologies

Typical single-phase buck type ac-dc converter topologies (Fig. 1) use one turn-off capability switching device and 5 diodes, or four turn-off capability switching devices, such as reverse blocking IGBT, and 4 diodes if the turn-off devices have no reverse voltage capability. The topology from Fig. 1(a) is the simplest, since only one switching device with turn-off capability is used. However, the topology with four turn-off switches (Fig. 1(b)) can be considered advantageous, since the waveform of the ac current has less harmonic distortion, due to the possibility to operate with negative bridge voltages, and the efficiency can be improved if reverse blocking capability turn-off switches are used.

To extend the output voltage range and to reduce the number of turn-off power semiconductors in the input current path, two new topologies, presented in Fig. 2 are proposed. These converters also use an ac filter, four (or two) turn-off switches with bipolar voltage blocking capability, two magnetically coupled inductors and two output capacitors. The two topologies, here termed double buck rectifiers, can limit the inrush and short circuit currents and can present output voltages higher than the ac supply peak value (theoretically limited at two times the peak value, since they are based on two bi-phase converters, each one limited to the ac peak voltage value).

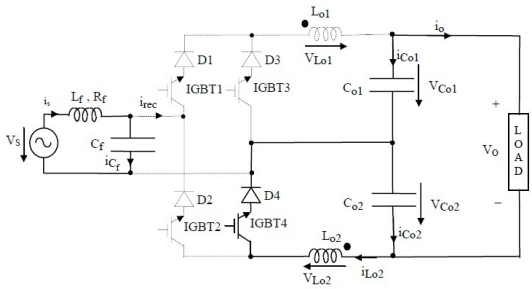
III. Double Buck Rectifier Operation

The operating stages of the double buck rectifier presented in Fig. 2(a) during the positive half cycle of the ac source voltage are described below:

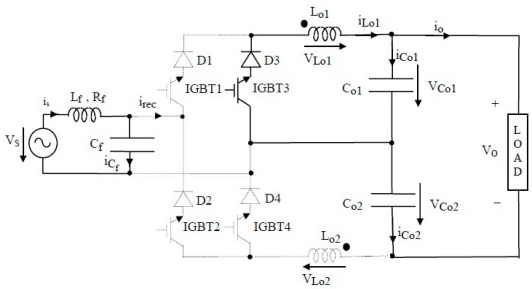
1st Stage (Fig. 3): Switch IGBT1 is turned on and inductor L_{o1} stores energy supplied by the ac source voltage. Therefore, the current in inductor L_{o1} will increase, and if this current is greater than current in inductor L_f, the voltage in capacitor C_f will decrease and current in inductor L_f will increase.

2nd Stage (Fig. 4): Switch IGBT1 is turned off while switches IGBT3 and IGBT4 are turned on. In this stage there are three different possibilities. If voltage V_{Co1} is higher than V_{Co2}, then diode D4 is on and diode D3 is off (Fig. 4(a)). If voltage V_{Co1} is lower than V_{Co2}, then diode D3 is on and diode D4 is off (Fig. 4(b)). If voltages V_{Co1} and V_{Co2} are equal then both diodes are on (Fig. 4(c)). In 1st stage, normally capacitor C_{o1} is charged while capacitor C_{o2} is discharged. Due to this, in this stage the energy stored in inductor L_{o1} is transferred to inductor L_{o2} (L_{o1} is magnetically coupled with L_{o2}) and to the capacitor C_{o2} trough switch IGBT4. Diode D3 is turned off. The voltage in capacitor C_f will increase and current in inductor L_f will decrease. On other hand, capacitor C_{o2} will charge (relatively to C_{o1}). When the voltage in capacitor C_{o2} equals the voltage in capacitor C_{o1}, diode D3 turns on. Half of the stored energy in inductor L_{o2} is transferred to inductor L_{o1} and to capacitors C_{o1} and C_{o2} trough switches IGBT3 and IGBT4. The voltage in capacitor C_f will increase and current in inductor L_f will decrease.

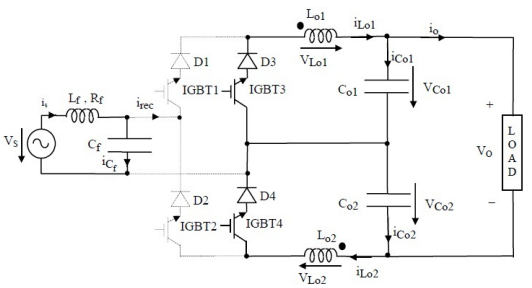
Fig. 5 and 6 show the current waveforms i_{Lo1} and i_{Lo2}. From these figures it is possible to verify the 1st and 2nd stage operation. It is also possible to verify the discontinuity in the DC inductors current due to the magnetic coupling between



(a) Voltage V_{Co1} is higher than V_{Co2}.



(b) Voltage V_{Co1} is lower than V_{Co2}.



(c) Voltages V_{Co1} and V_{Co2} are equal.

Fig. 4. Second stage.

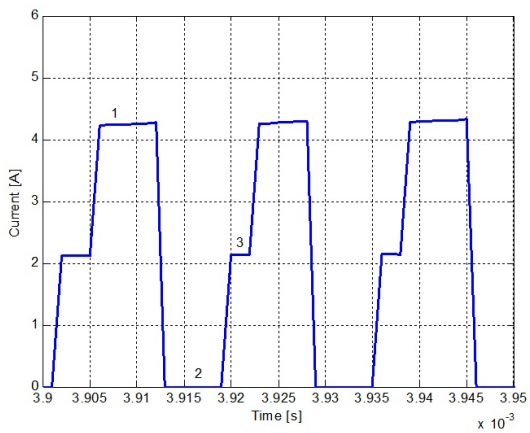


Fig. 5. Inductor current iLo1 (1-1st stage, 2-2nd stage when V_{Co1} is lower than V_{Co2}, 3-2nd stage when V_{Co1} is equal to V_{Co2}).

those inductors. The time zones represented by 1, 2 and 3 are related to the stages presented in Fig. 3, 4(a) and 4(c) respectively.

3rd Stage (Fig. 7): Switch IGBT2 is turned on and the stored energy in inductor L_{o2} is transferred to capacitor C_f. The voltage in capacitor C_f will increase and current in inductor L_f will decrease.

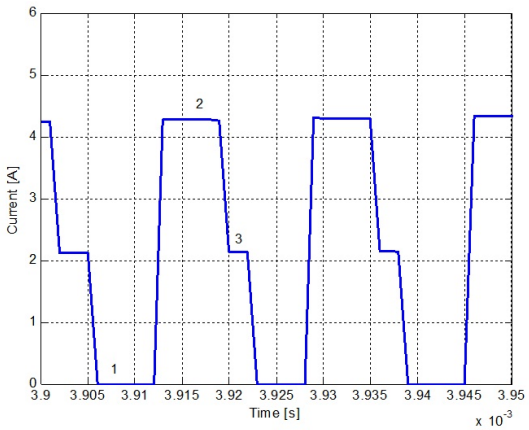


Fig. 6. Inductor current i_{Lo2} (1-1st stage, 2-2nd stage when V_{Co1} is lower than V_{Co2}, 3-2nd stage when V_{Co1} is equal to V_{Co2}).

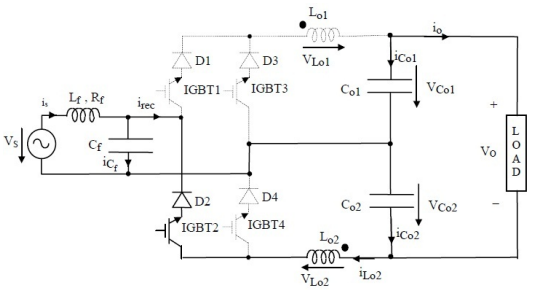


Fig. 7. Third stage.

In the negative half cycle of the ac source voltage there are also three operating stages. However, in the first stage IGBT2 is turned on, instead of IGBT1. In the third stage IGBT1 is turned on.

For the double buck rectifier presented in Fig. 2(b), the operation stages in the positive half cycle of the ac source voltage can also be described by the same three stages. However, while the input voltage capacitor C_f is positive the IGBT2 cannot be turned on, the main stages being only the 1st and 2nd stages. For the negative half cycle, since the input voltage capacitor is normally negative, then diode D1 is reverse biased. In this way, the main stages are only the 2nd and 3rd stages.

IV. Control of the Double Buck Rectifier

In PWM rectifiers, the input ac current dynamics usually must be much faster than the dc output voltage dynamics. Then, it is straightforward to separate the dynamics of the ac input current from the dynamics of the dc output voltage, allowing the use of a cascaded control structure. Therefore, to provide sinusoidal input current, the reference of the inner current loop must be nearly sinusoidal in phase with the input line voltage. Its sinusoidal amplitude will be defined by the voltage controller external loop (Fig. 8). As the ac input current (i_{rec}) of the double-buck switch-mode rectifier is controlled using on-off switches, the use of sliding-mode approach is advantageous, because sliding-mode controllers easily generate the needed discontinuous control actions and can ensure stability, robustness concerning system parameters and non modeling dynamics [11]–[16], being advantageous over constant frequency current mode control.

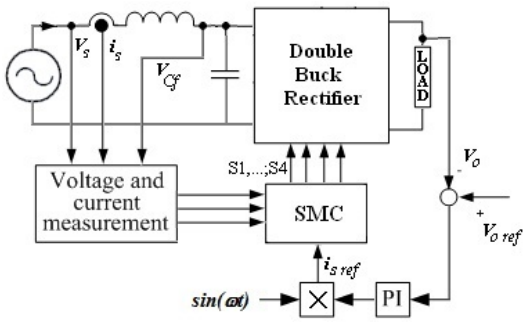


Fig. 8. Control structure of the double-buck rectifier.

Since the dynamics of this converter can be divided into fast motion (input ac current) and slow motion (output dc voltage), the output voltage control of this circuit can be controlled using a PI compensator, with gains selected to provide a stable system with good enough steady-state and dynamic responses.

A. Input current controller

The design method [11]–[15] for the proposed sliding mode current controller consists of two major parts: the design of the sliding surface and the design of the stable and robust switching control law that drives the state of the system towards the sliding surface. From the double-buck rectifier state-space model (1), it can be seen that the active switches only indirectly control the input line current (i_s).

$$\begin{cases} \frac{di_s}{dt} = -\frac{R_f}{L_f} i_s - \frac{1}{L_f} v_{C_f} + \frac{1}{L_f} v_s \\ \frac{dv_{C_f}}{dt} = \frac{1}{C_f} i_s - \frac{\alpha_1}{C_f} i_{L_{o1}} + \frac{\alpha_2}{C_f} i_{L_{o2}} \\ \frac{d\psi_o}{dt} = (\alpha_1 - \alpha_2)\, v_{C_f} - \alpha_3\, v_{C_{o1}} - \alpha_4\, v_{C_{o2}} \\ \frac{dv_{C_{o1}}}{dt} = i_{L_{o1}} - \frac{1}{R_o C_o} V_o \\ \frac{dv_{C_{o2}}}{dt} = i_{L_{o2}} - \frac{1}{R_o C_o} V_o \end{cases} . \quad (1)$$

The variables a_1 to a_4 represent respectively the states of the IGBT 1 to 4 (for the topology presented in Fig. 2(a) and variables a_3 and a_4 represent respectively the states of the diodes Do1 and Do2 for topology presented in Fig. 2(b) (2).

$$\alpha_i = \begin{cases} 1 & \text{, Switch } i \text{ is on} \\ 0 & \text{, Switch } i \text{ is off} \end{cases} , \qquad i = 1,2,3,4. \quad (2)$$

Considering the i_s current to be the controlled output, the input-output linearization of the state-space model (1), allows the following state-space model in the controllability canonical form:

$$\frac{d}{dt}\begin{bmatrix} i_s \\ \theta \end{bmatrix} = \begin{bmatrix} \theta \\ -\frac{R_f}{L_f}\,\theta - \frac{1}{L_f C_f} i_s + \frac{\omega}{L_f} V_{s\max} \cos(\omega t) - \\ -\frac{\alpha_1}{L_f C_f} i_{L_{o1}} - \frac{\alpha_2}{L_f C_f} i_{L_{o2}} \end{bmatrix} \quad (3)$$

where,

$$\theta = \frac{v_s - R_f i_s - v_{C_f}}{L_f}. \quad (4)$$

From (3) and (4) it is possible to conclude that the input line current has a strong relative degree of two [11], [13] (since its second time derivative contains the control variables a_i). So, considering this strong relative degree of the output variable (i_s), and the feedback tracking errors as the state variables ($e_{i_s} = i_{s\,ref} - i_s$; $e_\theta = \theta_{ref} - \theta$), the sliding surface ensuring the robustness of the closed loop system, is:

$$\begin{aligned} S(e_{i_s}, e_\theta) &= (i_{s\,ref} - i_s) + k\,(\theta_{ref} - \theta) = \\ &= (i_{s\,ref} - i_s) + k\left(\frac{di_{s\,ref}}{dt} - \frac{di_s}{dt}\right) \end{aligned} \quad (5)$$

where k ($k > 0$) is a parameter related to the time constant of the desired first order response of the tracking error ($i_{s\,ref} - i_s$).

Using (4) it is obtained

$$\begin{aligned} S(e_{i_s}, e_\theta) = (i_{sref} - i_s) + k\frac{di_{sref}}{dt} - \\ - \frac{k}{L_f}\left(v_s - R_f i_s - v_{C_f}\right). \end{aligned} \quad (6)$$

B. Switching strategy

The switching strategy must guarantee that the tracking error ($i_{s\,ref} - i_s$) trajectory moves towards the origin and stays on the sliding surface from any initial condition. This can be accomplished if the switching strategy enforces the following stability condition:

$$S\ (e_{i_s}, e_\theta)\ \dot{S}\ (e_{i_s}, e_\theta) < 0. \quad (7)$$

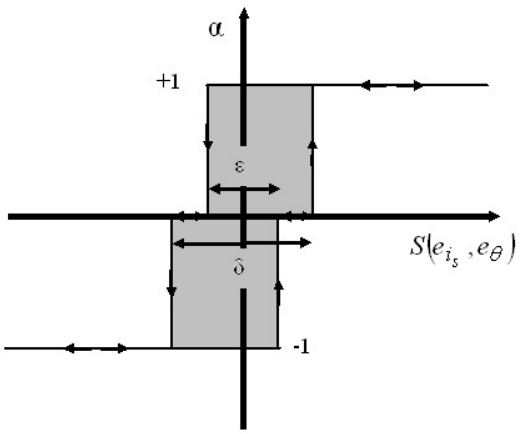
Since the topology presented in Fig. 2(a) has three operation stages, a three level hysteretic comparator with equivalent hysteresis ε and δ (Fig. 9(a)) will be needed to select each one of the 3 stages of the double-buck rectifier, upon the value of $S(e_{i_s}, e_\theta)$. Hysteresis widths are chosen to limit the maximum switching frequency.

For the double buck of Fig. 2(a), if the hysteretic comparator output α is -1 then IGBT 1 is turned on (first stage). If α is zero then IGBT's 3 and 4 are turned on (second stage). Finally, if α is +1 then IGBT 2 is turned on (third stage).

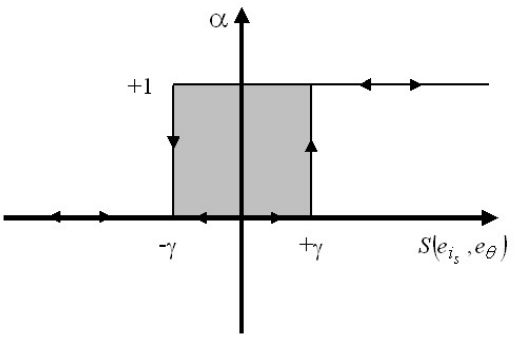
For the double-buck of Fig. 2(b), the stability condition (7) can be accomplished using only a two level hysteretic comparator with hysteresis 2γ(Fig. 9(b)), also dependent on the $S(e_{i_s}, e_\theta)$ value. In this case, if α is zero then IGBT 1 is turned on (first stage). If α is +1 then IGBT 2 is driven on (second stage). Although the IGBT 2 gate signal is on, for the positive half cycle of the ac source voltage, the input capacitor voltage is positive and reverse biases the IGBT 2 series diode, so that only Do1 and Do2 can be on (second stage). Therefore, although there are signals to turn on IGBT1 ($\alpha = 0$) and IGBT2 ($\alpha = +1$), in the positive half cycle only IGBT1 will be in the on state, the converter operating with two stages (first and second stages). Due to symmetry, in the negative half cycle the operating stages will be the second and the third.

C. Output Voltage Controller

To control the converter output voltage, given its slower dynamics, a proportional plus integral compensator (PI) is chosen and sized to have a stable system with good steady-state and dynamic responses. As the input frequency of the system is much lower (50Hz or 60Hz) than the switching



(a) Three level hysteretic comparator.



(b) Two level hysteretic comparator.

Fig. 9. Switching strategy for the rectifiers presented in Figs. 2(a) and 2(b).

frequency, an equivalent simplified model is used to determine the values of the PI compensator parameters. This simplified model considers that the sliding mode current controlled rectifier can be considered as a current controlled current source $I/I_{ref} = K_I/(1+sT_d)$ with gain K_I and time delay T_d ($T_d \approx \pi/\sqrt{L_{o1}C_{o1}}$).

Assuming that the rectifier is conservative, i.e., the input power equals the output power, and near unity input factor the $K_S = I_o/I_{sM}$ value can be obtained by (8).

$$K_S \approx \frac{V_{s\,\max}}{2\,V_o}. \tag{8}$$

The output voltage V_o is controlled by changing the amplitude I_{sM} of the input current. This is done by a linear PI controller (Fig. 8), processing the error between the output voltage reference $V_{o\,ref}$ and the actual output V_o. From the closed loop transfer function of the equivalent diagram, a second order transfer function can be obtained. Cancelling the load pole with the PI zero and using $\sqrt{2}/2$ for the required damping factor of the resulting 2nd order system, equations (9) and (10) can be derived to obtain the K_p and K_I parameters of the PI controller.

$$K_p \approx \frac{C_o}{4\,\zeta^2\,T_d} \tag{9}$$

$$K_i \approx \frac{1}{4\,\zeta^2\,T_d\,R_o}. \tag{10}$$

TABLE I
PARAMETERS OF THE TEST SYSTEM

Description	Value
Lf	5 mH
Cf	15 mF
Lo1, Lo2	1 mH
Co1, Co2	470 mF
Load	10 Ω

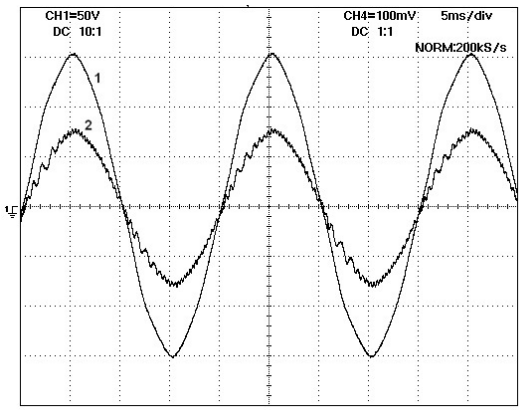


Fig. 10. Experimental result of: 1- input source voltage (50V/Div) and 2 - input line current (1A/Div).

V. EXPERIMENTAL RESULTS

To verify the operation principles and the control algorithms of the proposed double-buck topology a laboratory prototype was implemented. The parameters of the test system are reported in Table I.

Fig. 10 shows an experimental result of the input voltage and line current for the rectifier presented in Fig. 2(a). From this figure it is possible to confirm that the proposed rectifier provides almost sinusoidal input current and high power factor. The input source current is dominated by the main frequency sinusoid and the switching frequency components are greatly attenuated. The total harmonic distortion (THD) of the input line currents is 3.5%. For the four switch converter the THD is 3.2%. The reason for the THD reduction is due to the fully controlled rectifier, since in each half cycle the input current i_{rec} can be positive or negative. Fig. 11 shows an experimental result of the dc inductor current (i_{Lo1}) for the two switches rectifier, where it can be seen the discontinuous mode of operation of this current. This is explained by the magnetic coupling between the dc inductors.

Fig. 12 show the conversion efficiency versus the RMS input line voltage for the circuits with two and four switches. As expected, the efficiency is greater for the converter of the two switches. Increasing the input line voltage the difference of the efficiency of the two converters is reduced.

Fig 13 shows the total harmonic distortion versus RMS input voltage. The harmonic distortion becomes smaller when the input voltage increases. This is a consequence of the small current inside of the dc inductor at the beginning of each half-cycle. When the input voltage increases, the dc inductor current also increases, reducing the distortion at the beginning of each half-cycle. As expected, the THD is smaller for the converter of the four switches.

The power factor characteristics are related with input

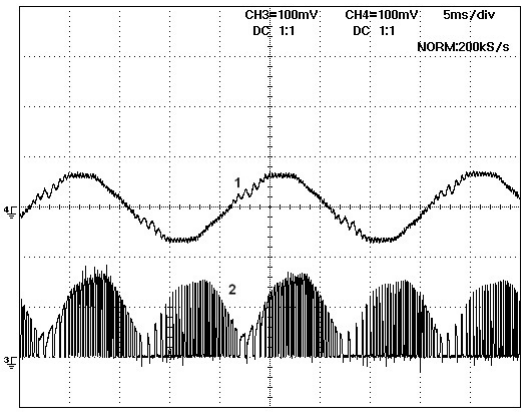


Fig. 11. Experimental result of: 1- input source voltage (50V/Div) and 2 - input line current (1A/Div).

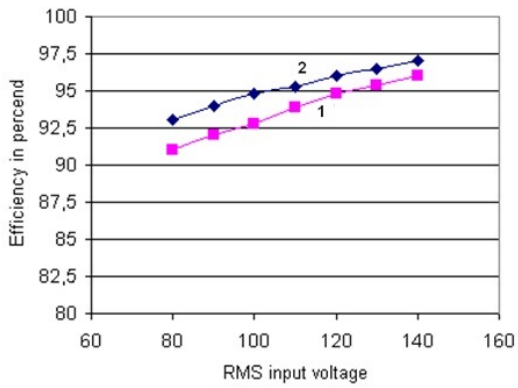


Fig. 12. Comparison of the experimental efficiency results (1– four switches converter, 2- two switches converter).

current THD and displacement. Since the displacement factor is near one, both proposed rectifiers present very high power factors. This high power factor value was obtained even for different duty cycles showing robustness of the control system. For example in [7] the power factor is highly dependent of the duty cycle. At 110 Vrms the power factor of the proposed rectifiers is 0.999, which is a better result when comparing to other approaches such as [9] and [10]. This also shows the effectiveness of this current control system.

The transient characteristics are investigated showing the response to load step variations, in order to analyze the closed loop performance of the proposed topology. Fig. 14 shows the experimental transient responses of the controller for the step change in the load resistor. This figure shows that it is possible to achieve a fast (<200ms) voltage regulation.

VI. Conclusions

Two new topologies for single-stage single-phase double-buck type PFC converters were presented, together with their operation principles. The output voltage wide range, up to twice the peak input voltage, is one of their advantages over the known single-stage Buck rectifiers, whose output voltage is lower than the ac peak value. The proposed double buck topologies present input currents with very low THD. A reduced number of switches on the main current path of the current, leading to relatively high efficiencies are another characteristic of the proposed topologies.

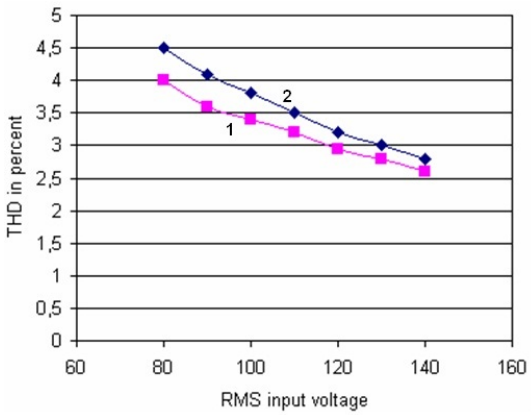


Fig. 13. Comparison of the experimental THD results (1– four switches converter, 2- two switches converter).

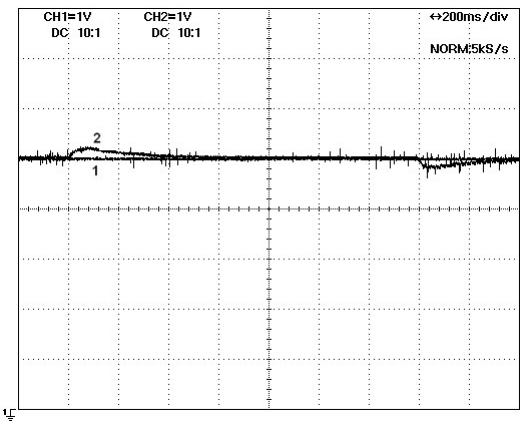


Fig. 14. Experimental results of: 1 - output voltage reference (10V/Div) and 2 - rectifier output voltage(10V/Div).

To control the proposed converters, a separation between fast and slow manifold approach leading to a cascaded controller was considered. For the inner current loop, sliding-mode robust controllers have been designed. For the external voltage loop, a proportional integral controller has been designed and tested. The design of the current and voltage controller parameters has been defined to obtain a high power factor with good output voltage regulation.

Experimental results from a laboratory prototype showed the in phase near sinusoidal input currents, near unity power factors and fast output voltage transient responses. Therefore, these converters are suitable for equipment that must meet stringent power quality standards and widely controllable output voltages.

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