A Four State Rotational Frequency Detector for Fast Frequency Acquisition

Hyeop-Goo Yeo, *Member, KIMICS*

Abstract— **This paper proposes a new rotational frequency detector (RFD) for phase-locked loop (PLL) or clock and data recovery (CDR) applications for fast frequency acquisition. The proposed RFD uses the four states finite state machine (FSM) model to accelerate the frequency acquisition time. It is modeled and simulated with MATLAB Simulink. The functionalities of the proposed RFD are examined and the results are compared to those of a conventional RFD. The proposed RFD's frequency acquisition time is four times faster than that of a conventional one. The proposed RFD incorporated with a phase detector (PD) in PLL or CDR is expected to improve the frequency and phase acquisition performance later greatly.**

Index Terms— **rotational frequency detector (RFD); phase-locked loop (PLL); clock and data recovery (CDR); fast frequency acquisition.**

I. INTRODUCTION

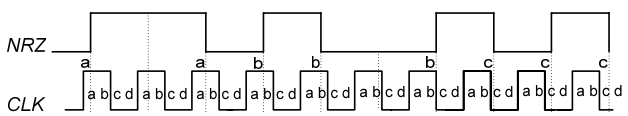
PHASE-LOCKED LOOP (PLL) is a crucial component used in data communications between digital systems and telecommunication systems for the synchronizing of the clock signal as well as synthesizing frequency. In typical, a PLL itself has limited capture range of frequency. Therefore, to achieve wide capture range and fast locking in a clock and data recovery (CDR) system, frequency acquisition aid using frequency detector (FD) is usually incorporated in parallel with PLL. For example, a rotational frequency detector (RFD) using in-phase (I) and quadrature-phase (Q) clocks are commonly used for frequency acquisition in CDR [1], [2].

There are a couple of design issues in PLL that must be taken into consideration. One is the stability issue. Generally, the stability of a PLL is related to the loop filter, thus it is designed to offer an additional system zero which may cause jitter peaking [2]. Second is the frequency and phase locking time. The acquisition in CDR is relatively slow even though the frequency-aid circuit is incorporated [3]. Another important one is noise issue such as a jitter. The jitter can affect the system performances of a high-speed data communications critically, such as a Gps serial data link transceiver [4].

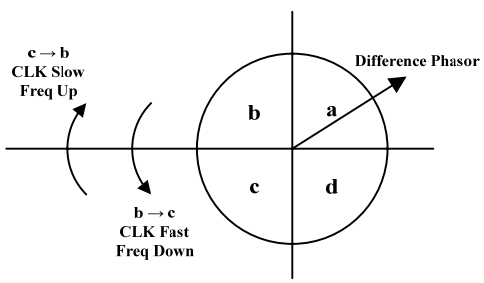
As mentioned, a FD is commonly used to achieve wide frequency capture range and fast frequency acquisition. However, the phase and frequency acquisition is relatively slow even though FD is incorporated with PD in CDR system, which is caused that the required loop bandwidth of the CDR system is much smaller than the tuning range [3]. Therefore, fast frequency acquisition is required to improve the performance of the system.

Fig. 1 shows a conventional RFD circuit. A clock signal is divided into four quadrants (a,b,c,d). They are sampled by incoming non-return-to-zero (NRZ) data and stored in flip-flops (FFs) at every transition of the data. Fig. 1 shows the RFD operations of time domain waveforms and a phasor diagram which represents the relation between the clock and data [5]. The time domain waveforms show an example of fast clock in counter-clockwise transition, b to c, and a phasor diagram representing the difference between clock and data phase. The clockwise rotation of the phasor difference means that the clock is slow and counter-clockwise rotation means vice versa.

For circuit realization, the wideband RFD uses the DET FFs to store the previous states represented as was_b, was_c and compares it to the present states represented as is_b, is_c to determine the direction of phasor rotation.



(a)



(b)

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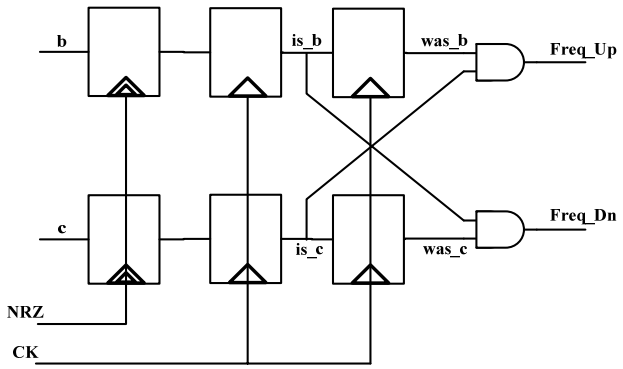
Hyeop-Goo Yeo is with the School of Information & Telecommunications, Hanshin University, Osan, 447-791, Korea (Email: hgyeo@hs.ac.kr)



(c)

Fig. 1. Conventional RFD (a) time domain waveform (fast clock) [5] (b) phasor diagram (c) circuit implementation.

This paper proposes a new RFD using a 4-states finite state machine (FSM) and examines it's functionalities and performances by MATLAB simulation. A RFD is normally incorporated with a phase detector (PD) in PLL or CDR systems to achieve wide capture range. However, this paper only limits to RFD to evaluate the performances of both the proposed and the conventional RFDs for the narrowband CDR applications.

The proposed RFD based on 4-states FSM and the circuit structure will be introduced in the next section. The performances of the proposed 4-state RFD is compared with those of a conventional RFD [1], [2], especially in terms of frequency acquisition. Simulations were performed using MATLAB Simulink which offers fast simulation and good flexibilities in analysis for the functional and performance verification. The proposed 4-state RFD greatly reduces the frequency acquisition time by evaluating the states transitions for frequency up or down four times more than that of a conventional RFD.

II. 4-STATE ROTATIONAL FREQUENCY DETECTOR

Fig. 5 shows the examples of state transition in slow and fast clocks. To define four states (similar to four quadrants, a, b, c, d described in previous section), I and Q clocks are used as a conventional RFD does [1], [2]. The states are determined by locations between the data and quadrature clocks. The states are defined as '00', '01', '10', and '11' in order to each state represent the I and Q clock positions easily, which are sampled at the both edges of NRZ signal respectively as shown in Fig. 2.

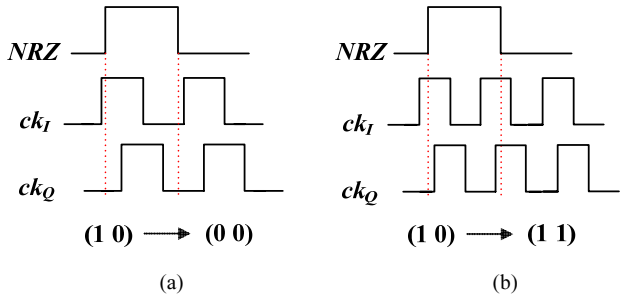


Fig. 2. The examples of the state transitions: NRZ sampling of I/Q clocks (a) slow (b) fast.

Fig. 3 shows the state transitions for slow clock condition and the time domain waveforms of NRZ data, I/Q clocks and Freq_Up/Freq_Dn signals. Assume the RFD loop is open and the clock-like pattern of '0101010101' NRZ data are coming into the RFD to understand state transitions when frequency difference between the data and clock exists. The state starts with (10) and transit to (00), (01), (11), and (10) in succession. There are four transitions during the $1/\Delta f$ period. After $\Delta T=1/\Delta f$, the same transitions will be repeated over. Freq_Up signal will be flagged when every clockwise state transition is occur, which means the clock is slow. The dotted line shows the averaged Freq_Up signal output during the period of Δf. There are four transitions for the proposed 4-state RFD during the period of $\Delta T=1/\Delta f$ while there is just one transition (c to b) for the conventional wideband RFD. As a result, the 4-state RFD produces four pulses during the $\Delta T=1/\Delta f$ period rather than one pulse (diagonal-line marked) as that of the conventional RFD. Therefore, the 4-state RFD is expected to improve frequency acquisition by about four times faster.

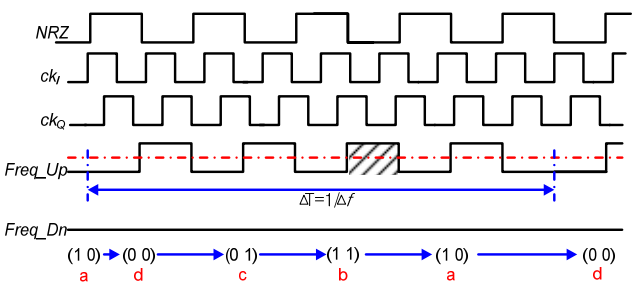


Fig. 3. Rotational state transitions and time domain waveforms of NRZ, I/Q clocks and Freq_Up/Freq_Dn signals.

The state diagram of the proposed 4-state RFD is depicted in Fig. 4. And the resulting state transition table is shown in Table I.

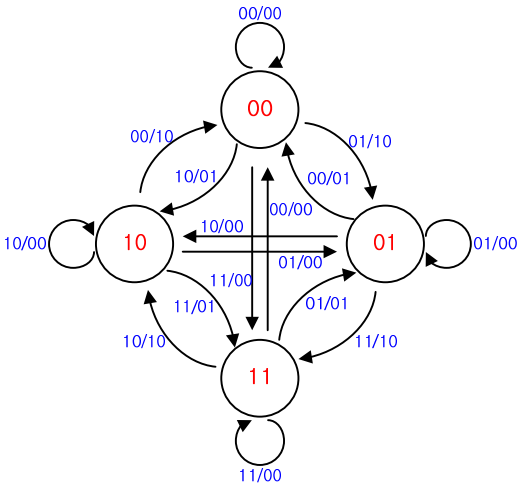


Fig. 4. State diagram of the proposed 4-state RFD.

There are two present states, A, B and inputs states, X_1, X_2, which will determine the next states as described in Table I. Freq_Up is flagged during the clockwise state transition, which means the clock is slow. Similarly, Freq_Dn is flagged during the counter clockwise state transition, which means the clock is fast. Jumping to the opposite state (ex. '01' → '10') cannot give any valid information of the frequency difference thus both Freq_UP and Freq_Dn signals would not be flagged. Also, if the state is not changed from the previous state, both Freq_Up/Freq_Dn would not be active as well as depicted in the state diagram shown in Fig. 4.

TABLE 1.
STATE TRANSITION TABLE OF THE PROPOSED DPD

Present State A(n) B(n)	Input State X_1(n) X_2(n)	Next State A(n+1) B(n+1)	Output Freq_Up /Freq_Dn
0 0	0 0	0 0	0 0
	0 1	0 1	1 0
	1 0	1 0	0 1
	1 1	1 1	0 0
0 1	0 0	0 0	0 1
	0 1	0 1	0 0
	1 0	1 0	0 0
	1 1	1 1	1 0
1 0	0 0	0 0	1 0
	0 1	0 1	0 0
	1 0	1 0	0 0
	1 1	1 1	0 1
1 1	0 0	0 0	0 0
	0 1	0 1	0 1
	1 0	1 0	1 0
	1 1	1 1	0 0

From the state transition table, the next states, $A(n+1)$, $B(n+1)$, are represented as (3), (4), respectively.

$$A(n+1) = X_1 \quad (3)$$

$$B(n+1) = X_2 \quad (4)$$

Also the Freq_Up/Freq_Dn signals are expressed as (4), (5).

$$Freq\_Up = \overline{A}\overline{B}\overline{X}_1X_2 + \overline{A}BX_1X_2 + A\overline{B}\overline{X}_1\overline{X}_2 + ABX_1\overline{X}_2 \quad (4)$$

$$Freq\_Dn = \overline{A}\overline{B}X_1\overline{X}_2 + \overline{A}B\overline{X}_1\overline{X}_2 + A\overline{B}X_1X_2 + AB\overline{X}_1X_2 \quad (5)$$

Fig. 5 shows the proposed 4-state RFD circuit. Double-edge-triggered (DET) flip-flops (FFs) sample ck_I and ck_Q signals using NRZ data. And the sampled states are transferred to the next FFs at every ck_I transition for input states, X1, X2. The states, A, B are also evaluated by every ck_I transition. The resulting states, X_1, X_2, A, B, are used to evaluate Freq_up or Freq_Dn and determine the next states. The logic implementations of Freq_Up/Freq_Dn are shown in Fig. 5(b).

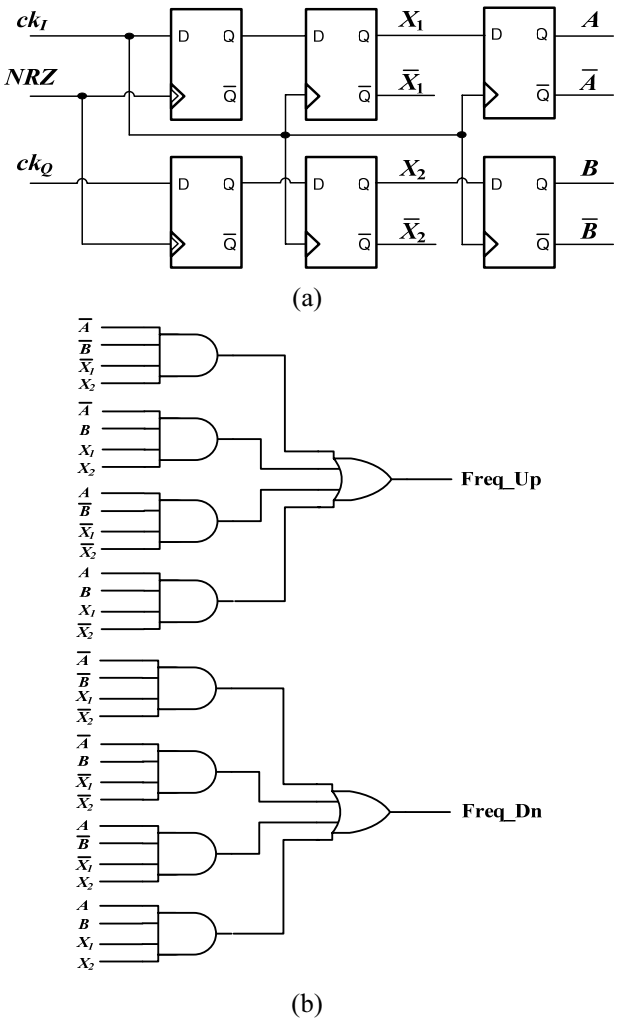


Fig. 5. Proposed 4-state RFD circuits for (a) states (b) outputs (Freq_Up/Freq_Dn)

III. SIMULATIONS

The proposed RFD is modeled with MATLAB Simulink to verify functionalities and performances. Usually, a PLL or a CDR loop includes a PD incorporated with a FD for wide capture range and fast locking. However, this paper only deals with RFD in order to compare the performances between the proposed and conventional RFDs.

Fig. 6(a) shows the RFD loop modeled with MATLAB Simulink. RFD and quadrature clock generator circuits are made by the logics provided by MATLAB Simulink. A continuous VCO is used in the Simulink library. Note that the RFD loop is modeled as 1st-order system [1] as shown in Fig. 6(b). Thus the transfer function, $H(s)$, of RFD is expressed 1st-order system as (6), where $\omega_n=K_{FD}K_{vco}/C_p$.

$$H(s)=\frac{1}{1+s/\omega_n} \tag{6}$$

The simulations are performed mainly with frequency acquisition time in various conditions. The pulse signals generated from Freq_Up/Freq_Dn are accumulated to a loop filter modeled as an integrator. The voltage output from the integrator controls the frequency of the VCO and the quadrature phase clock generator is followed.

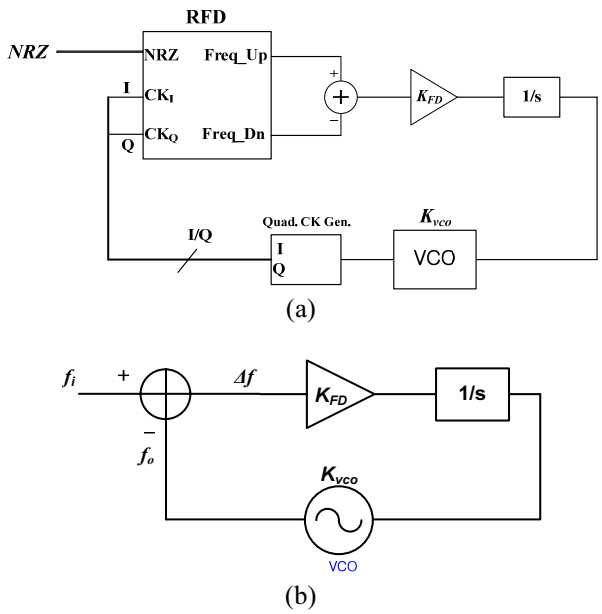


Fig. 6. RFD models: (a) with MATLAB Simulink (b) linear model

Fig. 7 shows the simulation results of the voltage output which controls the frequency of the VCO. Because two RFD have different frequency acquisition schemes, the NRZ pattern of '010101' (clock-like signal) instead of random NRZ data are used for the simulation to evaluate Freq_Up/Freq_Dn every clock period. The data rate of 1Gbps is the reference input, thus the 1GHz clock is required for data recovery.

The simulations are performed under the conditions of $K_{FD}=10^7$V/s, K_{vco}=500MHz/V. The PFD loop starts with the four different VCO frequencies with 700MHz, 900MHz, 1.1GHz, and 1.3GHz. Fig. 8 shows the frequency acquisition behaviors of the different frequency start-up conditions.

As mentioned, the frequency acquisition behavior shows the typical response of the 1st-order system as shown in Fig. 7. In this simulation, the frequency acquisition time is determined by the last Freq_Up or Freq_Dn pulse generation before settled signal.

From the simulation results, the frequency acquisition time of the proposed 4-state RFD is faster by a factor of four compared to that of the conventional wideband RFD, which is well matched with theoretical expectation analyzed in section II. The normalized pull-in range of -34% to +50% for both RFDs is obtained with these simulations.

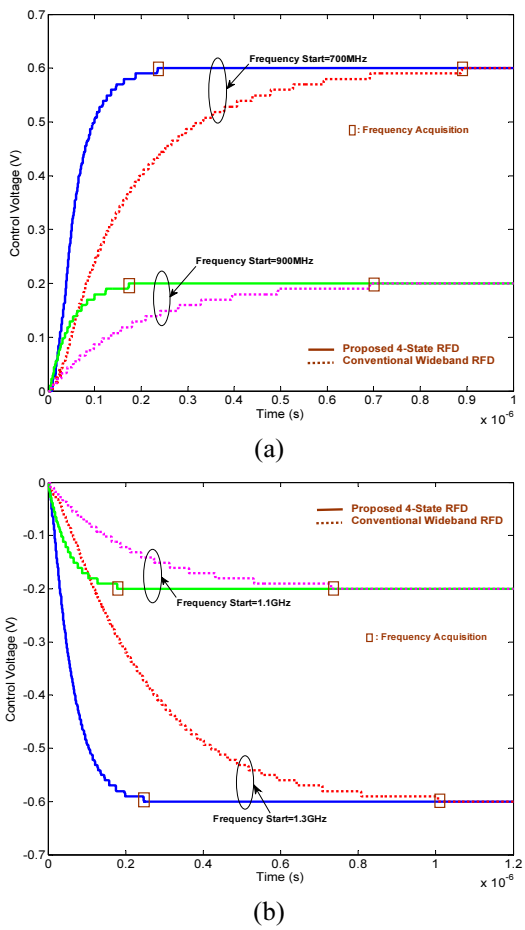


Fig. 7. The comparison of frequency acquisition behaviors for clock patterned NRZ ('010101') input: starting with (b) lower (a) higher frequency than the reference frequency

Similar simulations are performed to verify functionality and to compare the performances under the random NRZ data inputs. Since both the RFDs have different frequency acquisition schemes, the simulations are performed several times for the statistical result. Fig. 8 shows the frequency acquisition behaviors of both RFDs starting with frequency of 700MHz. As shown in Fig. 8, similar frequency acquisition behavior as those of the previous simulations

About four times faster frequency acquisition is obtained compared to that of the conventional wideband RFD from the simulations under random NRZ input in various start frequencies.

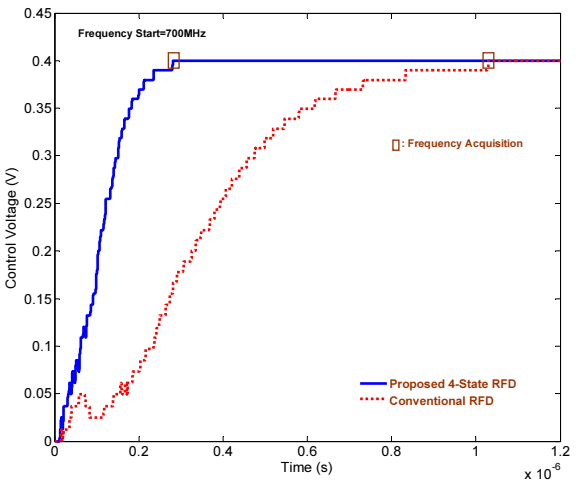


Fig. 8. The comparison of frequency acquisition behaviors between the proposed 4-state RFD and the conventional RFD for random NRZ input: starting with 700MHz.

IV. CONCLUSIONS

This paper proposed a new 4-state RFD which uses 4-states rather than two states as the conventional one has to improve the performance of the CDR system, especially frequency acquisition time. The proposed 4-state RFD's pulse generation efficiency with frequency difference was analyzed. As expected, the simulation results of the proposed 4-state RFD performed by MATLAB Simulink showed that the frequency acquisition performance has been improved by a factor of four compared to that of the conventional RFD without any performance degradation, such as pull-in range.

In conclusion, simulation results verified that the proposed 4-state RFD can be effectively used in PLL or CDR applications that require fast frequency and phase locking. Therefore, the proposed 4-state RFD incorporated with PD will greatly improve the performance of PLL or CDR applications, especially in terms of frequency acquisition time. Moreover, because its architecture is very simple, there is no difficulty in implementing the RFD into conventional technology.

ACKNOWLEDGMENT

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REFERENCES

[1] D.G. Messerschmitt, "Frequency Detectors for PLL Acquisition in Timing and Carrier Recovery," *IEEE Transactions on Communications*, vol. com-27, no. 9, pp. 809-820, Sep. 1979.

[2] L. DeVito, J. Newton, R. Croughwell, J. Bulzacchelli, and F. Benkley, "A 52MHz and 155MHz Clock-Recovery PLL," *ISSCC Dig. Tech. Papers*, pp. 142-143, Feb. 1991.

[3] T.H. Lee, and J.F. Bulzacchelli, "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol. 27, no.12 pp. 1736-1746, Dec. 1992.

[4] B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003.

[5] D. Dalton, K. Chai, E. Evans, M. Ferriss, D. Hitchcox, P. Murray, S. Selvanayagam, P. Shepherd, and L. DeVito, "A 12.5-Mb/s to 2.7-Gb/s Continuous-Rate CDR With Automatic Frequency Acquisition and Data-Rate Readback," *IEEE Journal of Solid-State Circuits*, vol. 40, no.12 pp. 2713-2725, Dec. 2005.

Hyeopgoo Yeo (M'09) received his B.S. and M.S. degrees in electronic engineering from Yonsei University in Seoul, South Korea, in 1991 and 1993, respectively. He also received his M.S. and Ph.D. degrees in electrical and computer engineering from the University of Florida in Gainesville, FL, USA, in 2003 and 2007, respectively. From 1993 to 1999, he worked as a design engineer at Samsung Electronics Co., Ltd, where he performed ASIC cell library and high-speed digital I/O design using various CMOS technologies for gate-array and standard cell. In 2008, Dr. Yeo joined the hardware R&D group at Samsung, where he was involved with mobile hardware design for wireless communications. In March 2009, he joined Hanshin University and he is currently an Assistant Professor. His research interests include high-speed serial link systems, wireless communication systems, and RF/analog circuit design.