# Design of Low Power Capacitive Sensing Circuit with a High Resolution in CMOS Technology

Seung-Min Jung, *Member, KIMICS*

***Abstract*—This paper describes the possibility of a low-power, high-resolution fingerprint sensor chip. A modified capacitive detection circuit of charge sharing scheme is proposed, which reduces the static power dissipation and increases the voltage difference between a ridge and valley more than conventional circuit. The detection circuit is designed and simulated in 3.3V, 0.35μm standard CMOS process, 40MHz condition. The result shows about 27% power dissipation reduction and 90% improvement of difference between a ridge and valley sensing voltage. The proposed circuit is more stable and effective than a typical circuit.**

***Index Terms*— capacitive sensing, detection circuit, low power, high resolution, CMOS, VLSI**

## I. INTRODUCTION

**A** fingerprint is made of a series of ridges and valleys on the surface of the finger. Some research organizations have published papers on semiconductor-based sensing schemes and demonstrated the possibility of a single-chip solution[1-3]. In a capacitive fingerprint sensor, the finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode. These two electrodes are separated by the passivation layer of a silicon chip and air. By measuring the variances of the capacitance according to the distance from the chip surface to the finger's skin, the pattern of a fingerprint, i.e. ridges and valleys, can be obtained. A capacitive fingerprint sensor uses a capacitive sensor array to detect fingerprints. The name 'capacitive' comes from the fact that the finger skin and the sensor electrode produce a capacitor whose capacitance is determined by the distance. The fingerprint sensor chip is composed of the sensing scheme and analog to digital converter for a reference voltage as shown in Fig. 1.

One of the most important performances of a capacitive sensor is the sensitivity capability since the capacitance to be detected is very small of the order of femtofarads. A charge-sharing sensing scheme has a high sensitivity and a simple circuit structure for the restricted pixel area below a sensor plate. Some papers on charge-sharing sensing scheme have been published [4]-[6]. The paper [4] proposed the removing of parasitic capacitance using unit-gain buffer, and paper [5][6] proposed the improvement of difference between a ridge and valley detection voltage using a feedback resistor. Although these methods above are useful in dramatic performance improvement, a static current can exist on a sensing enable phase in these circuits because of a unit-gain buffer and feedback resistor. This paper proposes a modified circuit for reduction of the static power dissipation and increasing the voltage difference between a ridge and valley more than conventional circuit.

In the following sections, the overall architecture and power analysis of the typical capacitive sensing scheme will be discussed (Section II), and conclusions focuses on the proposed detection circuit blocks and simulation results will be presented (Section III).

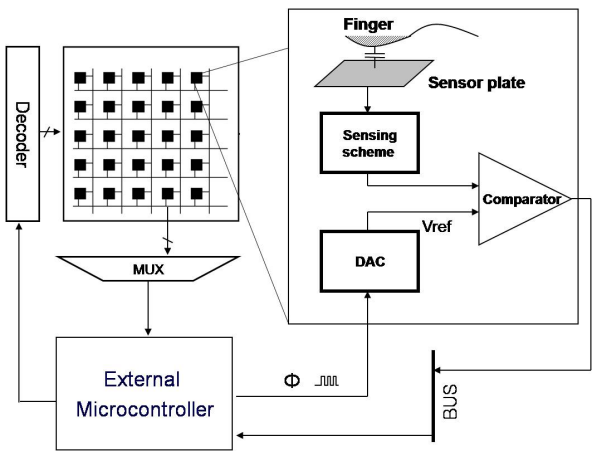



Fig. 1. Sensor chip configuration

## II. CAPACITIVE SENSING SCHEME

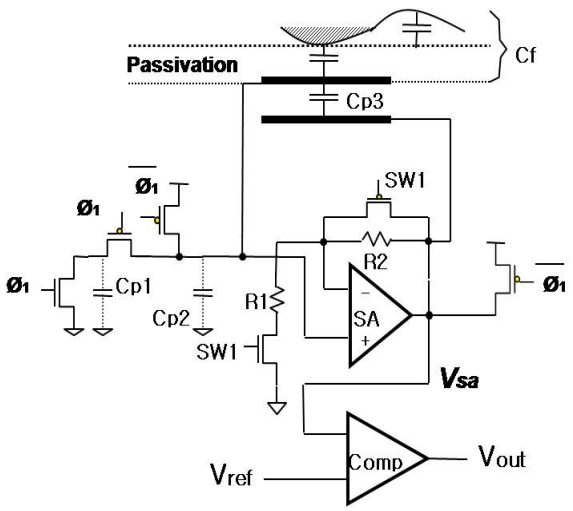
Fig. 2 shows a conventional capacitive charge-sharing sensing scheme and timing diagram[6]. The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode. These two electrodes are separated by the passivation layer of the silicon chip and air. The series-connected capacitor Cf is composed of a capacitor between the metal plate and the chip surface and another one between the chip surface and the finger skin. The

Manuscript received May 2, 2011; revised May 28, 2011; accepted June 7, 2011.

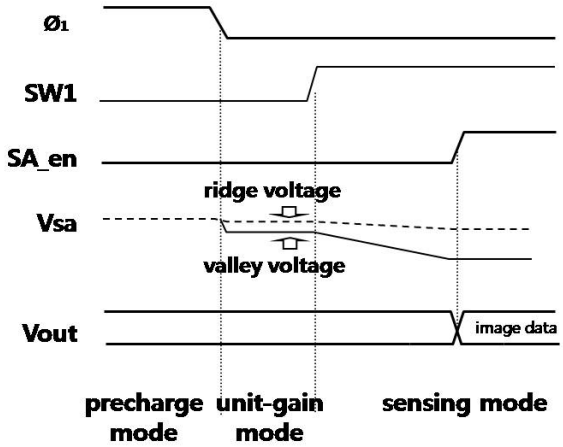
Seung-Min Jung is with the Department of Information Science and Telecommunications Eng., Hanshin University, Osan, 447-791, Korea (Tel: +82-31-379-0661, Mobile: +82-19-286-2571, Email: jasmin@hs.ac.kr)

capacitance of Cf is at its maximum value when a ridge has contact with the passivation layer. As the distance between the chip surface and the finger's skin increases, the capacitance becomes smaller. The variation of capacitance is transferred to output voltage by sensing scheme. The comparator discriminates a ridge and valley by reference voltage, Vref.

In Fig. 2, "SA" is a unit-gain buffer and "Comp" is a comparator. When $Ø_1$ is high and SW1 is low, the operation is in the precharge phase. The node Cp2 and Vsa are precharged to VDD, and node Cp1 is discharged to GND. In this phase, no charge is accumulated in Cp3 because the two electrodes have the same potential. In Cp2 and Cf, the amount of charge stored is Cp2·VDD and Cf·VDD. At the beginning of the unit-gain phase, the charges stored in the precharge are redistributed between the nodes. The SW1 is low and R1 and R2 do not operate. The SA is enabled as a unit-gain buffer in this phase. The SA tracks the voltage change of the node Vsa, which makes the potential difference between the two electrodes of Cp3 zero. Usually, because Cp1 and Cp2 are the parasitic metal routing capacitances, they are much smaller than Cp3. Therefore, we need a circuit to remove the effect of Cp3. From this point of view, an application of SA is an effective method. In the sensing phase, S1 is high and SA operates as an attenuator by R1 and R2 ratio. Fig. 3 shows an equivalent circuit of SA at the sensing phase. The SA is composed of only five MOSFETs for the restricted pixel area below the sensor plate. Through the simulation which is repeated, R1 is 5k and R2 is 1.4 k. The comparator 'Comp' is enabled by the signal 'SA_en' and compares the voltage of Vsa with the external reference voltage Vref. Thus, a binary output according to the finger pattern is produced. SA operates as an attenuator, as well as a unit-gain buffer by handling the switching signal, SW1.




(a) Sensing circuit




(b) Timing diagram

Fig. 2. Conventional capacitive charge-sharing sensing scheme.

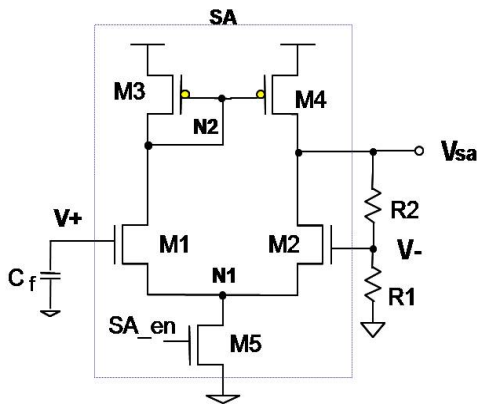



Fig. 3. Equivalent circuit of SA in sensing phase.

The operation and power consumption can be seen by the HSPICE simulation of the cell with condition of 40MHz, 0.35μm typical parameter and 3.3V power supply in Fig. 4. The voltage difference between the contacted point (ridge) and the non-contacted point (valley) is only 610mV in unit-gain phase, but 1720mV after sensing phase. Thereby, the comparator easily discriminates the ridge and valley.

Even though the voltage difference is increased, there is power consumption by the static current. It is caused by the unit-gain buffer and feedback registers. In sensing phase, when the valley voltage Vsa of Fig. 2 and Fig. 3 starts to decrease due to feedback registers in sensing phase, the voltage cannot decrease fast enough. Because SA_en enables to high after Vsa fully discharges to 0 voltage, duration of static current is long. Fig. 4 shows a power dissipation result. The average current is 605 uA in a ridge and 204 uA in a valley at 3.3V, 40MHz operation condition. If the occurrence number of a ridge and valley is same, the average current is 404 uA in general operation.

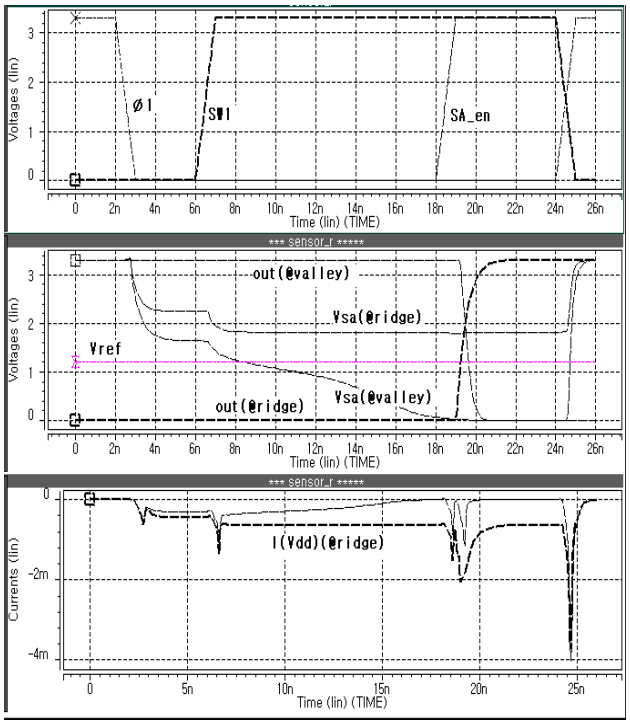
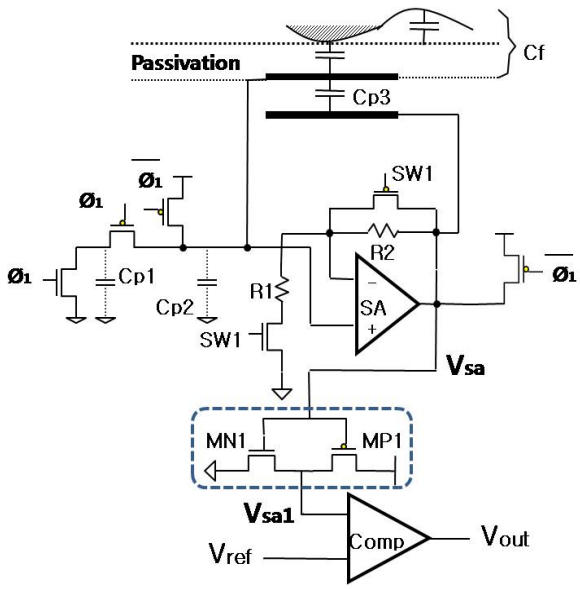



Fig. 4. Simulation result of conventional circuit. (3.3V, 0.35 μm CMOS process typical condition, 40MHz)

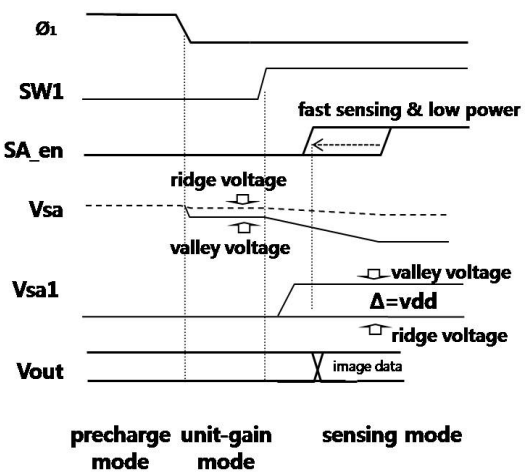
## III. PROPOSED SENSING SCHEME

Fig. 5 shows the proposed capacitive sensing circuit. To accelerate fast sensing of the voltage decrease of Vsa we inserted an inverter with a small size transistor MP1, MN1 into conventional sensing configuration. The width of MN1 transistor is designed more than MP1. Therefore, the logic threshold voltage of the inverter is less than VDD/2 for fast pull-up of Vsa1 in a valley. As a result, we can make fast SA_en enable time. It means reduction of static current duration. The inverter is composed of MN1 of 2μm width and MP1 of 1.5μm for the restricted pixel area below the sensor plate. The area penalty is just 1.5 % of one sensor pixel layout. Fig. 6 shows the function and power dissipation result. In a valley, Vsa1 reaches high voltage fast by the inserted inverter without waiting of slow decrease of Vsa. The average current is 385 uA in a ridge and 203 uA in a valley at 3.3V, 40MHz operation condition. If the number of a ridge and valley is same, the average current is 294 uA in general operation. It means 27% reduction of power consumption.

Vsa1 is comparator input voltage. In proposed circuit, because Vsa1 is fully VDD in a valley and about 0 voltage in a ridge, the voltage difference between a ridge and valley is about VDD in sensing phase. Our method produces about 90% improvement in the voltage difference between ridge and valley. As a result, we can get high-quality images without the influence of the reference voltage(Vref) variation according to a pixel location of the sensor array. The enhancement of the SA's voltage gain may make this design sensitive to process variation. Specially, the output signal is expected from the variation of the parasitic capacitance due to fluctuation in a 0.35μm CMOS process. Thus, we apply the capacitance value of the worst case process. Actually, we designed concerning the process variation.




(a) Modified Sensing circuit




(b) Timing diagram

Fig. 5. Proposed capacitive charge-sharing sensing scheme

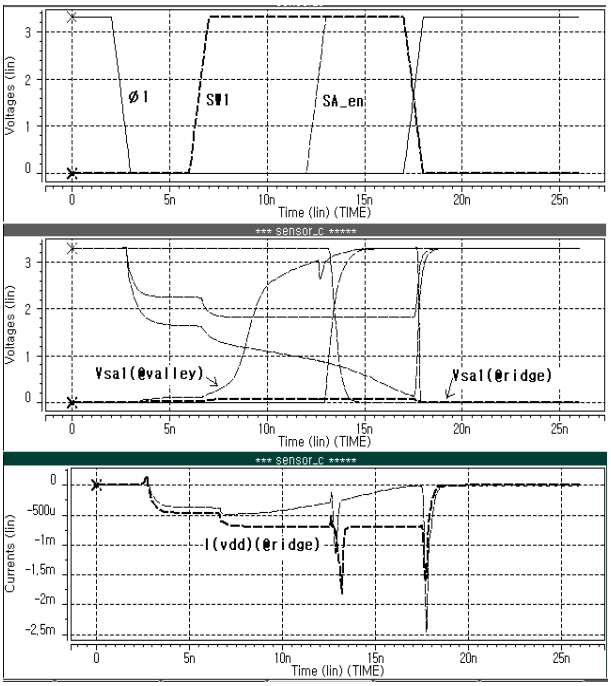



Fig. 6. Simulation result of proposed circuit.
(3.3V, 0.35 μm CMOS process typical condition, 40MHz)

## IV. CONCLUSIONS

This paper proposes a modified hardware scheme of capacitive charge-sharing fingerprint sensors for low power consumption and high image resolution. The conventional sensing scheme minimizes the influences of internal parasitic capacitances and amplifies the voltage difference between the contacted point and the non-contacted point. The voltage difference between a ridge and valley was 1720mV. Even though the voltage difference is increased, there is power consumption by the static current. It is caused by the unit-gain buffer and feedback registers configuration. If the occurrence number of a ridge and valley is same, the average current was 404 uA in general operation.

The modified capacitive detection circuit of charge sharing scheme includes an inverter with a small size transistor to accelerate fast sensing of comparator. The logic threshold voltage of the inverter is less than VDD/2 for fast pull-up of a valley sensing voltage. As a result, we can make fast comparator enable time. It means reduction of static current duration. In addition, because sensing voltage of a valley is fully VDD and about 0 volt in a ridge, the voltage difference between a ridge and valley is about VDD. Proposed circuit reduces the static power dissipation and also increases the voltage difference between a ridge and valley more than conventional circuit. The modified detection circuit is designed and simulated in a 0.35 μm standard CMOS process, 40MHz frequency condition. The result shows about 27% power dissipation reduction and 90% improvement of difference between a ridge and valley sensing voltage. The proposed circuit is more stable and effective than a typical circuit.

In future work, it is planned to layout and perform a post-simulation for a full chip implementation.

## ACKNOWLEDGMENT

This work was supported by Hanshin University Research Grant.

## REFERENCES

[1] Shimamura, T., Morimura, H., Shigematsu, S., Nakanishi, M., Machida, K, "Capacitive-Sensing Circuit Technique for Image Quality Improvement on Fingerprint Sensor LSIs," IEEE J. of Solid-state circuits, vol. 45, No.5, pp 1080 - 1087, May, 2010.

[2] Seung-Min Jung, "Design of Circuit for a Fingerprint Sensor Based on Ridge Resistivity," International Journal of KIMICS, Vol. 6, No. 3, September 2008.

[3] Seung-Min Jung, "A Robust Resistive Fingerprint Sensor," International Journal of KIMICS, Vol. 7, No. 1, March 2009.

[4] J. W. Lee, D. J. Min, J. Y. Kim, and W. C. Kim, "A 600-dpi Capacitive Fingerprint Sensor Chip and Image-Synthesis Technique," IEEE J. of Solid-state circuits, vol. 34, No.4, pp469-475, April, 1999.

[5] Seung-Min. Jung, J.-M. Nam, D.-H. Yang, and M.-K Lee "A CMOS Integrated Capacitive Fingerprint Sensor with 32-bit RISC Microcontroller,'' IEEE Journal of Solid-State Circuits, vol. 40, no. 8, pp. 1745–1750, Aug. 2005.

[6] Jin-Moon Nam, Seung-Min Jung, Moon-Key Lee, "Design and implementation of a capacitive fingerprint sensor circuit in CMOS technology", Sensors and Actuators A: Physical, vol. 135, No. 1, pp. 283~291, Mar. 2007.

**Seung-Min Jung** (M'02) Refer the (IJMICS) International Journal of Maritime Information and Communication Sciences, Vol. 6, No. 1, 2008. He is associate professor in the Information Science and Telecommunications Eng. Department, Hanshin University, Osan, Korea.