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Annealing temperature dependence on the positive bias stability of IGZO thin-film transistors

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The threshold voltage shift (ΔV_{th}) under positive-voltage bias stress (PBS) of InGaZnO (IGZO) thin-film transistors (TFTs) annealed at different temperatures in air was investigated. The dramatic degradation of the electrical performance was observed at the sample that was annealed at 700°C. The degradation of the saturation mobility (μ_{sat}) resulted from the diffusion of indium atoms into the interface of the IGZO/gate insulator after crystallization, and the degradation of the subthreshold slope (*S-factor*) was due to the increase in the interfacial and bulk trap density. In spite of the degradation of the electrical performance of the sample that was annealed at 700°C, it showed a smaller ΔV_{th} under PBS conditions for 10^4 s than the samples that were annealed at 500°C, which is attributed to the nanocrystal-embedded structure. The sample that was annealed at 600°C showed the best performance and the smallest ΔV_{th} among the fabricated samples with a μ_{sat} of 9.38 cm^2/V s, an *S-factor* of 0.46 V/decade, and a ΔV_{th} of 0.009 V, which is due to the passivation of the defects by high thermal annealing without structural change.

Keywords: annealing; IGZO; threshold voltage shift; positive-voltage bias stress

1. Introduction

It has been considered of late that among the alternatives for Si as active channel layers of thin-film transistors (TFTs) are zinc-oxide-(ZnO)-based materials, because of their several merits, such as high mobility, good stability, and good uniformity on a large-area substrate [1–5]. Among the ZnO-based oxide materials, zinc tin oxide [1], hafnium indium zinc oxide [2], aluminum zinc tin oxide [3], and indium gallium zinc oxide (IGZO) [4, 5] have attracted much attention as alternative active channel layers of TFTs [4]. Many researchers have focused on improving the device performance and stability with various process control methods, and it has been known that many fabrication process factors can affect the TFT performance, such as oxygen partial pressure [6,7], sputtering power [6], the composition of each element [8], the contact material for source and drain (S/D) metals [8,9], and the annealing conditions [6,7]. Among these, annealing is a common and significant TFT fabrication process used to improve device performance and stability [6,10]. The annealing conditions include the annealing temperature [10], ambient [11], sequence [12], and time [13]. The effects of the annealing temperature of over 500°C on the TFT performance and stability, however, have not been much investigated.

2. Experiment

A gate insulator (GI) was formed on a highly doped n-type Si substrate, which was used as a gate electrode, with a 100-nm-thick SiO_2 film, using thermal oxidation. A 50-nm-thick channel layer (target: In_2O_3:Ga_2O_3:ZnO=1:1:1 mol%) was deposited on a SiO_2/Si substrate using radio frequency (RF) magnetron sputtering at room temperature, with a power density of 1.39 W/cm^2, a working pressure of 1 mTorr, and a gas mixture ratio of Ar:O_2 = 65:35. The channel layer was photolithographically patterned. Then a-IGZO thin films were annealed in a furnace for 3 h in air, at 400°C, 500°C, 600°C, and 700°C, respectively. Finally, source–drain (S/D) electrodes were formed via direct-current magnetron sputtering with 100-nm-thick indium zinc oxide (IZO) thin films through a shadow mask.

To observe the variation of the crystalline phase with the annealing temperature, 200-nm-thick a-IGZO thin films were deposited on SiO_2/Si substrates, and the crystallization of the films was measured using X-ray diffraction (XRD). High-resolution transmission electron microscopy (HR-TEM) was also performed to investigate the microstructure of the IGZO films.

Positive-voltage bias stress (PBS) was performed with the conditions of a fixed gate-to-source voltage

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$(V_{GS}) = +15$ V and a fixed drain-to-source voltage $(V_{DS}) = 10.1$ V for 10^4 s. During the stress time, the transfer characteristics were measured with the sweeping of V_{GS} from -30 to $+30$ V at a fixed $V_{DS} = 5.1$ V to investigate the variation of the electrical performance for several points during the stress time with stopping bias for data collection.

3. Results and discussion

Figure 1 shows the drain currents (I_D) of the fabricated TFTs corresponding to the sweeping of the V_{GS} from -30 to 30 V. The extracted TFT parameters are listed in Table 1. For the samples that were annealed at 400°C, 500°C, and 600°C, the transfer curves had slightly different characteristics, as shown in Figure 1. In the case of the saturation mobility (μ_{sat}), the sample that was annealed at 400°C showed 5.97 cm^2/V s, and the μ_{sat} of 600°C increased to 9.38 cm^2/V s, which was due to the greater generation of carriers in the 600°C-annealed sample than in the 400°C-annealed sample. On the other hand, for the sample that was annealed at 700°C, the μ_{sat} dramatically decreased compared with the samples that were annealed at under 600°C, which could be attributed to the decreasing indium content and the trapping of the mobile carriers in the grain boundaries described by Levinson's model, similar to the ZnO films [14]. The sample that was annealed at 700°C had a nanocrystalline-embedded structure, as shown in the inset of Figure 2(b).

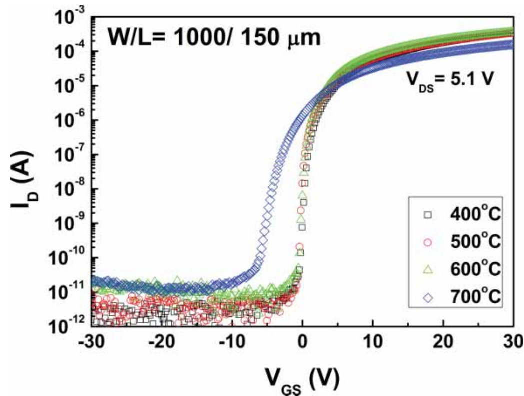

Figure 1. Initial transfer curves of the fabricated samples annealed at 400°C (black square), 500°C (red circle), 600°C (green triangle), and 700°C (blue diamond).

Table 1. Extracted parameters from the transfer characteristics.

	400°C	500°C	600°C	700°C
μ_{sat} (cm^2/V s)	5.97	6.96	9.38	2.39
V_{th} (V)	0.98	0.68	0.59	−4.35
$I_{on/off}$ ratio	8.18×10^9	3.3×10^9	1.51×10^8	1.65×10^6
S-factor (V/decade)	0.48	0.43	0.46	0.92

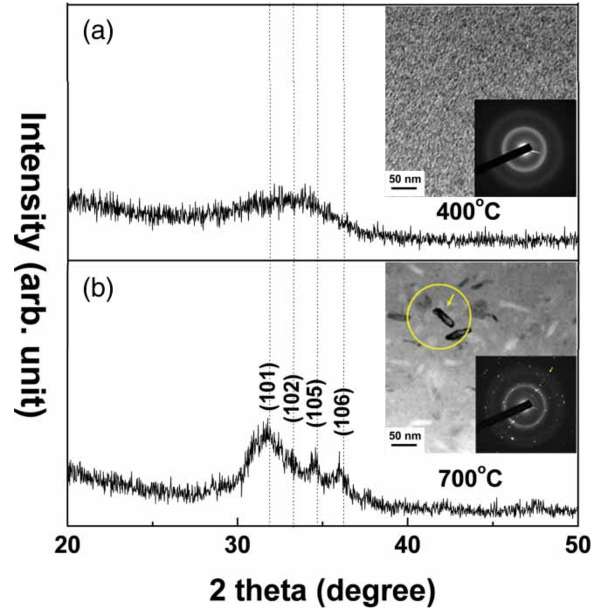

Figure 2. XRD patterns of the samples annealed at (a) 400°C and (b) 700°C (the insets show the HR-TEM image of each sample).

Figure 2(a) and (b) shows the XRD patterns of the IGZO thin films for the samples that were annealed at 400°C and 700°C, respectively. Up to an annealing temperature of 600°C, no peak indicating the crystalline phase was observed, which provided information that the amorphous phase was maintained until at least 600°C. When the film was annealed at 700°C, diffraction patterns with a high full-width at half-maximum of the $In_2Ga_2ZnO_7$ phases (JC-PDS #38-1097) were shown, indicating that crystallization had occurred. The insets of Figure 2 also show the top-view TEM images and the selected-area electron diffraction patterns of the films that were annealed at 400°C and 700°C, respectively. There was no ordered structure showing the crystalline lattice in the film that was annealed at 400°C, as shown in Figure 2(a), indicating that the phase was amorphous. Nanocrystals with 20–30 nm sizes randomly distributed and embedded in an amorphous matrix, however, were monitored in the IGZO film that was annealed at 700°C. An amorphous IGZO thin film with a stoichiometry of $InGaZnO_4$ maintaining the amorphous phase at annealing temperatures as high as 500°C was reported by Nomura et al. [15]. Crystallization of the samples with a stoichiometry of $In_2Ga_2ZnO_7$, however, occurred at 700°C. Recently, the temperature dependency of IGZO thin films (prepared through the solution process) with respect to indium content was investigated [16]. According to the report, as the indium ratio in the IGZO films increased, the energy for crystallization also increased. Hence, the difference in the crystallization temperature of the IGZO films was due to their different compositions.

In the case of the subthreshold slope (*S-factor*), no noticeable difference was observed in the samples that were annealed at 400°C, 500°C, and 600°C, but a dramatic

degradation of the *S-factor* was observed in the sample that was annealed at 700°C, which was due to the increase in the total trap density, including the bulk trap density (N_{bulk}), of the IGZO active layer and the interface trap density (D_{it}) at the interface between the IGZO film and the GI, which can be calculated by using the following equation [17]:

$$N_t = [S\log(e)/(k_B T/q) - 1]\frac{C_i}{q}, \quad (1)$$

where N_t is the total trap density in the semiconductor film and semiconductor/insulator interface, S is the subthreshold slope, k_B is Boltzmann's constant, q is the electronic charge, and C_i is the capacitance of the GI per unit area. According to Equation (1), N_t is proportional mainly to the *S-factor* assuming that all the other parameters are the same, which means that the increase in the *S-factor* resulted from the increase in N_t.

The large negative shift of the threshold voltage (V_{th}) for the sample that was annealed at 700°C (V_{th} of −4.35 V) compared with those for the samples that were annealed at under 600°C, as shown in Table 1, is believed to be associated with the relatively large free-electron concentration (N_d) of the IGZO films. It was reported that a large N_d in a-IGZO could cause an increase in the TFT on-current and a negatively shifted V_{th} [18]. Moreover, the off-current of the oxide TFTs increased due to the conductivity of the neutral active region. The higher N_d could be attributed to Zn exhaustion, as reported by Cho et al. [19]. Hence, the negative shift of V_{th} and the higher off-current for the samples that were annealed at over 700°C are believed to be associated with the relatively large N_d of the IGZO films (N_d was calculated using capacitance–voltage analysis, but the data are not shown here).

Figure 3 shows the evolution of the transfer curves of the samples that were annealed at (a) 400°C, (b) 500°C, (c) 600°C, and (d) 700°C under the gate voltage bias of

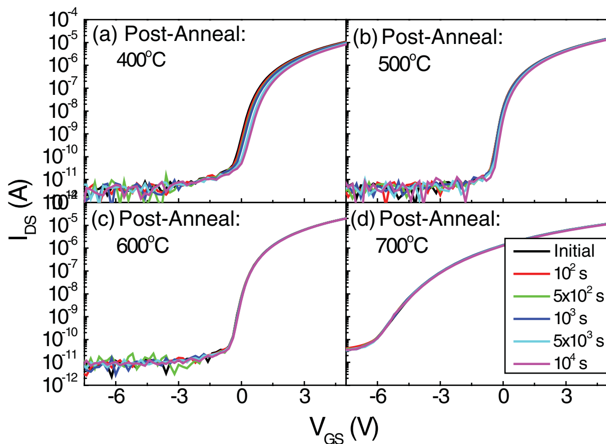

Figure 3. Evolution of the transfer curves of the samples that were annealed at (a) 400°C, (b) 500°C, (c) 600°C, and (d) 700°C under PBS conditions for 10^4 s.

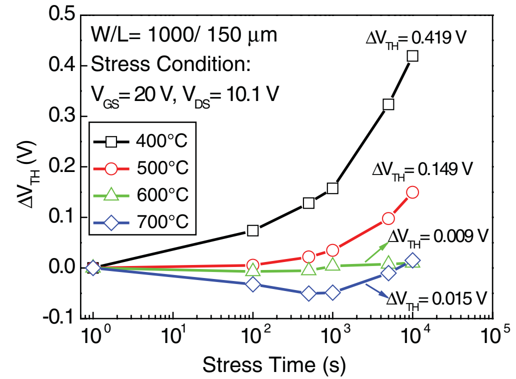

Figure 4. Extracted threshold voltage shifts (ΔV_{th}) of the samples that were annealed at (a) 400°C, (b) 500°C, (c) 600°C, and (d) 700°C from the evolution of the transfer curves shown in Figure 3.

+15 V and the stress time of 10^4 s, respectively. The transfer curves for all the samples moved in the positive direction and showed rigid movement without changes in the *S-factor* and on-current, as shown in Figure 3. According to the previous report by Wager and co-workers [20], the positive shift of V_{th} under PBS conditions can be explained by three mechanisms: (1) charge injection and/or trapping at the IGZO/GI interface and into the GI; (2) deep-level defect creation; and (3) charge trapping in the IGZO thin films. The results of the experiment indicate that the instability of the PBS conditions can be explained by mechanisms (1) and (3) [20]. Mechanism (2) is ruled out because there were no apparent changes in the *S-factor* and on-current, as mentioned in the previous report [19].

Figure 4 shows the extracted values of the threshold voltage shifts (ΔV_{th}) of each sample corresponding to Figure 3. The ΔV_{th} of the sample that was annealed at 400°C was 0.419 V, which showed a much larger shift compared with the other samples. As the annealing temperature was increased, the ΔV_{th} decreased. This was due to the defect passivation effect of the high thermal energy in the IGZO thin films generated during the deposition, as previously reported [11]. Especially, the sample that was annealed at 600°C showed a ΔV_{th} of 0.009 V, which was an extremely low value. This means that high-temperature annealing can effectively decrease defects and improve the stability under PBS conditions. Although the 700°C-annealed sample showed inferior electrical performance compared with the other samples, its ΔV_{th} (0.015 V) under 10^4 s was comparable with that of the 600°C-annealed sample, but it showed better stability than the samples that were annealed at 400°C and 500°C, supposedly due to the nanocrystalline-embedded structure of the IGZO thin film.

4. Conclusion

Bottom-gated InGaZnO (IGZO) TFTs were fabricated using a highly doped n + Si substrate, and the instability of the fabricated TFTs under PBS conditions for 10^4 s

annealed at different temperatures in air was investigated. The electrical performance of the sample that was annealed at 700°C showed a dramatic degradation compared with those of the samples that were annealed at 400°C, 500°C, and 600°C. The degradation of the μ_{sat} resulted from the diffusion of indium atoms into the GI interface after crystallization, and the degradation of the *S-factor* was due to the increase in the interfacial and bulk trap density. A smaller ΔV_{th} was shown under PBS conditions, however, compared with the samples that were annealed at 400°C and 500°C, presumably due to the nanocrystalline-embedded structure of the IGZO thin film. The sample that was annealed at 600°C showed the best performance and the smallest ΔV_{th} among the fabricated samples, which can be explained by the defect passivation effect of high-temperature annealing.

Acknowledgements

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