474 Journal of Electrical Engineering & Technology Vol. 6, No. 4, pp. 474~483, 2011
DOI: 10.5370/JEET.2011.6.4.474

Enhancement of Power System Transient Stability and Power Quality Using a Novel Solid-state Fault Current Limiter

A. R. Fereidouni*, B. Vahidi†, T. Hoseini Mehr and M. Garmroodi Doiran***

Abstract – Solid-state fault current limiters (SSFCL) in power systems are alternative devices to limit prospective short circuit currents from reaching lower levels. Fault current limiters (FCL) can be classified into two categories: R-type (resistive) FCLs and L-type (inductive) FCLs. L-type FCL uses an inductor to limit fault level and is more efficient in suppressing voltage drop during a fault. In contrast, R-type FCL is constructed with a resistance and is more effective in consuming the acceleration energy of generators during a fault. Both functions enhance the transient stability of the power system. In the present paper, a novel SSFCL is proposed to enhance power system transient stability and power quality. The proposed SSFCL uses both functions of an L-type and R-type FCL. SSFCL consists of four diodes, one self-turn-off IGCT, a current-limiting by-pass inductor (L), and a variable resistance parallel with an inductor for improvement of power system stability and prevention of over-voltage across SSFCL. The main advantages of the proposed SSFCL are the simplicity of its structure and control, low steady-state impedance, fast response, and the existence of R-type and L-type impedances during the fault, all of which improve power system stability and power quality. Simulations are accomplished in PSCAD/EMTDC.

Keywords: Solid-state fault current limiter, Transient stability, Power system, Fault current

1. Introduction

As electric power systems have become more complicated, fault levels are becoming larger due to increasing electric power demand. To increase the reliability of power supply, electric power systems are interconnected to one another to share electric power. However, once a fault occurs, the fault current also comes from the interconnected grids. The interconnection of the power system is restricted to a certain extent such that the fault current will not exceed the capacity of the circuit breaker (CB). Furthermore, the interconnection allows the rejection of the fault point from the power system by the CB to avoid the expansion of the influence of the fault when it occurs [1].

With the increasing demand for electric power, power systems are becoming larger and more interconnected. As a consequence, fault current increases and transient stability problems become more serious. Hence, to maintain the stability of the power system, replacing the substation equipment, changing the system configuration, or installing a fault current limiter become necessary at a certain point [2]. To overcome the high fault current, traditional methods have been used in the last decades. Current-limiting fuses, series reactors, or high-impedance transformers replace or modify the parameterization of existing equipment (such as transformers, CBs, etc.) and adjust the system for new fault duty and FCL. However, some of these alternatives may create other problems, such as loss of power system stability, high cost, and increase in power losses, which may ultimately lead to decreased operational flexibility and lower reliability [3]−[6].

FCL is a good option for limiting fault current and maintaining the stability of a power system [6],[7] because the application of FCL in electric power systems can suppress the amplitudes of short-circuit fault currents and enhance power system stability and voltage quality [8].

FCLs can be classified into R-types (resistive) and L-types (inductive) by current-limiting impedance. An L-type FCL is more effective in suppressing voltage drop during a fault, and limits the AC component of fault current better than the other type. In contrast, an R-type FCL is more effective in consuming the acceleration energy of generators at the fault [1].

In the past few years, many kinds of fault current-limiting devices have been developed in accordance with the development of power electronics, magnet technology, and superconducting materials [9]−[12].

Superconducting FCL has emerged as an alternative to limit prospective short-circuit currents to lower levels and improve power system reliability and stability by reducing the fault current. Three configurations of superconductor-

† Corresponding Author: Dept. of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran. (vahidi@aut.ac.ir)
* Dept. of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran. (fereidouni_aut@aut.ac.ir, mehdi_ garmrudi @yahoo.com)
** Dept. of Electrical Engineering, Isfahan University of Technology, Isfahan, Iran (hoseini.mehr124@gmail.com)
Received: November 24, 2010; Accepted: April 28, 2011

based fault current-limiting devices are available. This type of FCL is useful for bringing the superconductor into its off-state; however, it has several disadvantages that manifest either in the external sources or magnetic fields. The superconducting device takes a long time to cover from its fault current-limiting properties because the coolant must be cooled back to its pre-fault temperature. These materials ensure the cost-efficiency and reliability of the cooling system for the superconductor, which needs to be cooled to the temperature of helium. The cooling system requires maintenance from time to time because it can sometimes produce poisonous gases when overheated [13].

Because cooling technologies are still in their infancy stage, they often succumb to frequent breakdowns. Moreover, the commercial deployment of these technologies has not yet been accomplished; thus, only a few countries have this type of technology [14].

The present paper proposes to use SSFCL to limit prospective short-circuit currents to lower levels and improve the reliability and stability of power systems. We propose and investigate a solid-state FCL (SSFCL) that has excellent features of both the L-type and R-type FCL. The proposed SSFCL consists of four diodes, one self-turn-off IGCT, a current-limiting bypass reactor (L), and a variable resistance parallel with current limitting reactor. The most beneficial quality of the proposed configuration is the simplicity of its structure and control, low steady-state impedance, fast response, and high impedance fault. Furthermore, the configuration takes a very short time to cover, from its fault current limiting to its pre-fault, is both economical, and is readily available. In the present paper, we mainly provide a theoretical analysis on improving power system transient stability using the proposed SSFCL, which is capable of consuming excessive acceleration generator power, increasing stability limit of the system, and enlarging the stability region after the short circuit.

A simulation study on one-machine infinite bus system, including the proposed SSFCL, is performed in accordance with the laboratory scale test system [15]. The effects of the SSFCL unit on the transient stability of the power system and power quality is investigated and evaluated.

2. Configuration of the New SSFCL

The configuration of the new single-phase SSFCL is shown in Fig. 1. The configuration comprises a self-turn-off device IGCT (T); four diodes D1, D2, D3, and D4; a current-limiting impedance L; and a variable resistance $R_{variable}$. SSFCL improves the operation of the SCR bridge-type FCL with bypass reactor in Fig. 2 [16] by substituting power switches T1, T2, T3 and T4 with four diodes D1, D2, D3, and D4. The aim of this process is to simplify the circuit and DC reactor (L1) with a self-turn-off device IGCT (T). Attaching variable resistance $R_{variable}$ in parallel with the current-limiting impedance and removing the voltage-limiting element (Zno) are also part of the process. The self-turn-off device IGCT is used as a fast solid-state switch to discontinue a current instantly upon receiving a turn-off signal. Current-limiting bypass reactor (L) and variable resistance ($R_{variable}$) are used to pass the fault current when the solid-state switch interrupts and decreases a fault current, enhancing power system stability and power quality. Variable resistance prevents over-voltage, which can probably be caused by a sudden interruption of current.

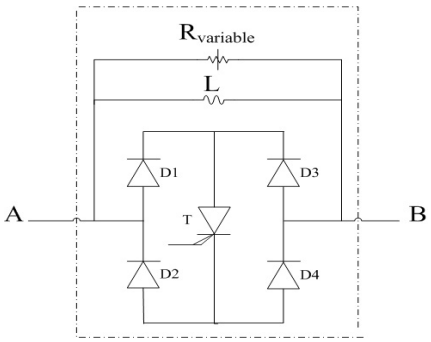


Fig. 1. Configuration of the proposed single-phase SSFCL

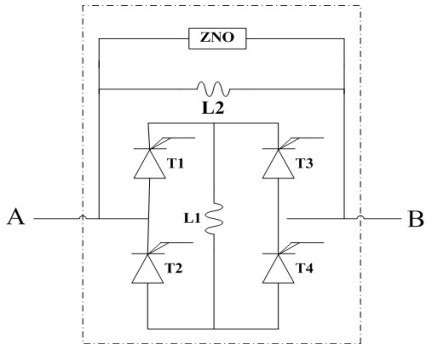


Fig. 2. SCR bridge-type FCL with bypass reactor [16]

Fig. 3 shows the three-phase SSFCL scheme that can be acquired after being set up using one single-phase SSFCL in every phase line. The benefits of this scheme are a simple control method, independence of operation, and convenience of selected location, among others. However, 12 diodes and 3 IGCT devices are needed for this particular scheme, which is not economical.

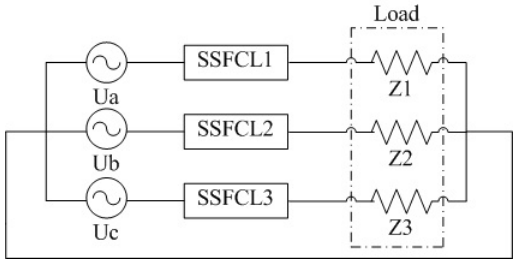


Fig. 3. Three-phase SSFCL composed of a single-phase unit

To simplify the system and decrease the volume, the weight and cost of the SSFCL and compact structure of the three-phase SSFCL shown in Fig. 4 are recommended.

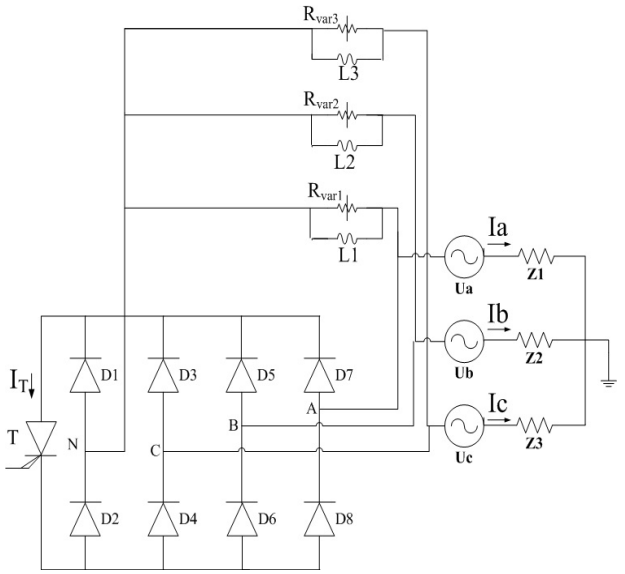


Fig. 4. Configuration of the proposed three-phase SSFCL

The proposed three-phase SSFCL consists of 8 diodes D1–D8, 3 bypass reactors L1−L3, and 3 variable resistances R_{var1}–R_{var3}, which are parallel with bypass reactors L1−L3, respectively, and one IGCT device T.

3. Concept of Proposed SSFCL

In the steady state, the self-turn-off device IGCT (T) is turned on and all current flows through the diodes. When a fault occurs, the self-turn-off device IGCT (T) is switched off, thereby forcing most of the current to flow through the inductor and variable resistance branch. As shown in Figs. 5(a) and 5(b), variable resistance has high impedance, whereas I_{FCL-LR} is more than a certain value (varistor current) and has low resistance while the I_{FCL-LR} is less than the varistor current; these states are called OFF and ON modes in the present paper. When a fault occurs, the SSFCL is in the waiting mode, and the current of the SSFCL is lower than the varistor current. Therefore, the variable resistance is in ON mode and the current passes via the variable resistance and reactor. The SSFCL is in the current-limiting mode [Fig. 5(b)] while the current of the SSFCL is more than the varistor current. Therefore, the variable resistance is in OFF mode and the current passes via a reactor. The absolute value alternately varies more and less during a cycle. During one cycle, although current is more than the varistor current (variable resistance: OFF), the current does not flow through the variable resistance. Because the peak of the line current [i.e., I_{FCL-LR}] is restricted by the inductance of the SSFCL, the SSFCL works as an L-type FCL. Although I_{FCL-LR} is lower than the varistor current (variable resistance: ON), the current also flows through the variable resistance; thus, the resistor consumes the energy. The SSFCL works as an R+L-type FCL. Consequently, the proposed SSFCL has the current-limiting characteristics of both L-type and R-type FCLs.

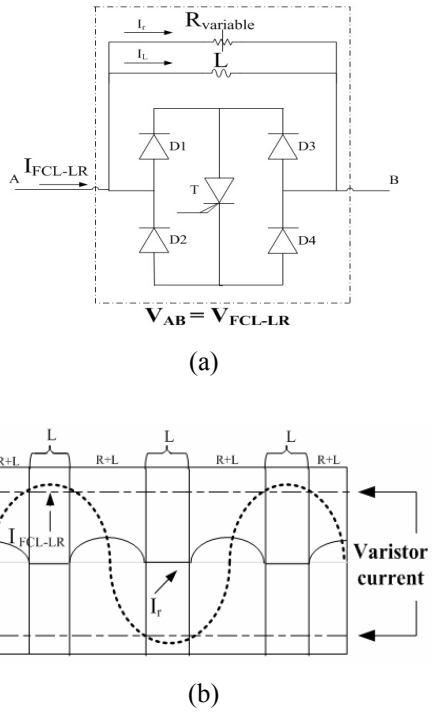


Fig. 5. Schema of (a) the proposed SSFCL and (b) operation principle in current-limiting mode

3.1. Sequence of Operation of Variable Resistance

The sequence of operation of this variable resistance is shown in Fig. 6. A description is also provided.

Before beginning the simulation, the variable resistance is initialized with an initial impedance value $R_{initialize}$ = High. The simulation is then begun to monitor the current magnitude and rate of current change during the entire simulation time. After achieving a steady-state operating point, a three-phase-to-ground fault is inserted into the system, which is external to the SSFCL. As soon as the fault is inserted, the magnitude of the line current jumps instantaneously and achieves a new steady-state value while the fault is present. However, to ensure that there is a fault in the transmission system and that the impedance is not falsely triggered, the rate of current change is also monitored. A fault changes the rate instantaneously. After setting the necessary flags, variable resistance is ramped down to low resistance. While the fault current is present in the varistor current (-VC < I < +VC), the SSFCL works as an L+R-type FCL. As soon as the fault current becomes more than +VC and lower than –VC, variable resistance is ramped up to high resistance, and SSFCL begins to work as

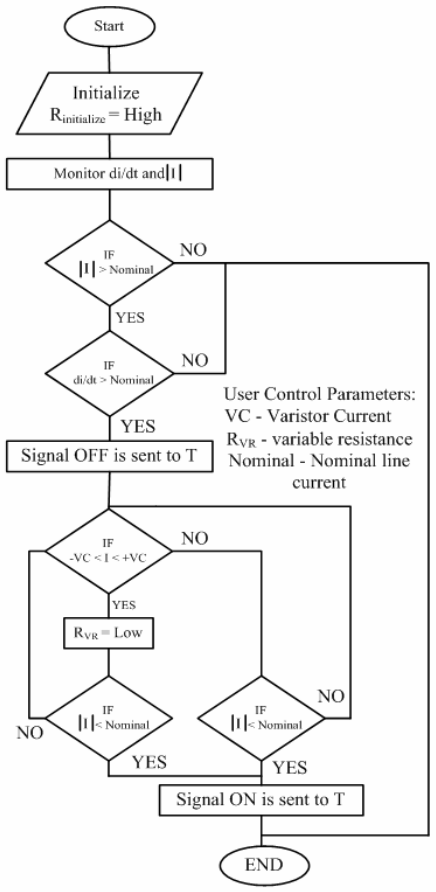


Fig. 6. Sequence of activation for variable resistance

an L-type FCL. After the fault is cleared, the variable resistance is ramped up to the initial resistance; this cycle occurs whenever there is a fault.

3.2. Proposed SSFCL Activation Timing

Timing the operation of the FCL trigger is of paramount importance when modeling any devices. The activation time of an FCL can be a function of its physical properties or user settable parameters via a relay or built-in timers. Fig. 7 shows the proposed SSFCL activation-timing diagram.

As Fig. 7 shows, a fault is inserted at the time of fault. The magnitude of the line current immediately increases and the "magnitude flag" is raised. The "rate of change flag" is also asserted because the rate at which the line current changes is non-zero. While fault current is in between –VC < I < +VC, the variable resistance of the SSFCL is ramped down to low resistance such that the limiting current and variable resistance can proceed (L+R-type SSFCL). As soon as the fault current becomes more than +VC and lower than –VC, the variable resistance is ramped up to high resistance such that the limiting current proceeds (L-type SSFCL). Once the fault is cleared, the variable resistance is ramped up to initial resistance.

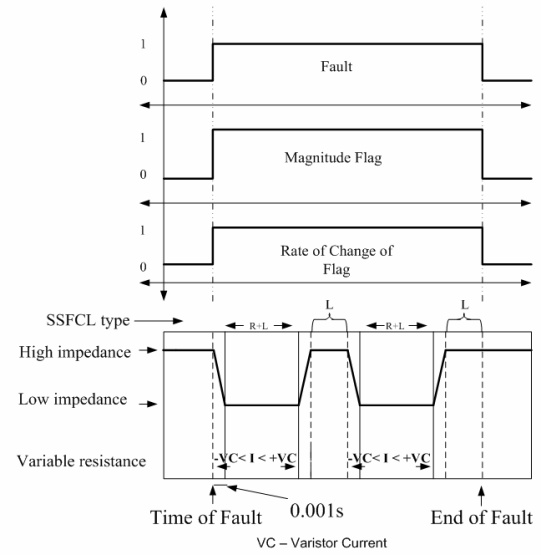


Fig. 7. Proposed SSFCL activation-timing diagram

4. Modeling and Simulation

4.1. Model Power System

A simulation model of the proposed SSFCL based on experimental results is performed by PSCAD (power system computer-aided design). Using the SSFCL model, power system simulation studies are carried out in one-machine infinite bus system with parallel transmission lines that correspond to a laboratory scale experimental system (Fig. 8). The rating capacity is 120 MVA, rating voltage is 13.8 kV, and frequency is 60 Hz. The three-phase, four-pole synchronous generator is expressed by a 7-order model based on Park's equation. The CB1 and CB2 that simulate CB are closed in the initial location. A three-line grounded fault (3LG) is simulated at the terminal of the lower line (fault line) by closing the SW. After a while, the fault line is rejected by opening CB1 and CB2, and this time interval is called "clearing time." Meanwhile, the "reclosing time" occurs when CB1 and CB2 are reclosed to become the initial condition. During reclosing time, the SW is opened to clear the fault. The SSFCL is installed at the generator side bus in both lines. Simulation studies are performed under the

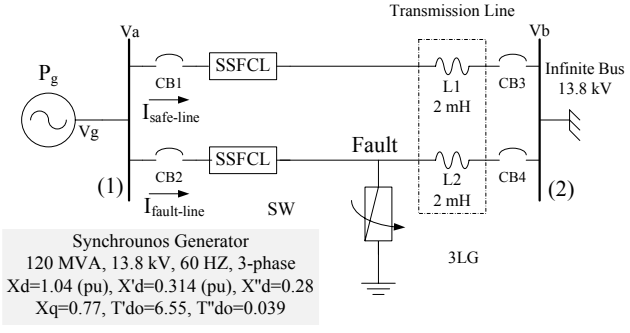


Fig. 8. Simulation model system including the proposed SSFCL

conditions of 3LG fault with reclosing time of 900 ms and fault-clearing time of approximately 100 ms.

Transient stability analysis is performed by combining the solution of algebraic equations. This solution describes the network with a numerical solution of differential equations, which in turn describe the motion of the machine rotor. In these studies, the synchronous generator is represented by a voltage source behind a transient reactance X'_d. During transient conditions, the generator internal voltage remains constant in magnitude but changes its angle (δ). This angle corresponds to the angle between the generator internal voltage and infinite bus voltage. The mechanical power, P_M, which is supplied by the turbine, also remains constant. These simplified assumptions, which correspond to neglect, excitation, and speed governor systems, are considered valid if transient simulation time is under 1 s. The two lines are equal and are characterized by reactance X_L (X_{L1} = X_{L2}). When the system operates in normal conditions, the SSFCL presents zero impedance. During fault conditions, the SSFCL is represented by impedance Zsc, which characterizes the final resistance or inductance presented by SSFCL device. The non-linear differential equation, also called swing equation, describes the motion of the synchronous machine rotor:

$$\frac{2H}{\omega_0}\ddot{\delta} + D\dot{\delta} + P_G(\delta) = P_M \tag{1}$$

$$\dot{\delta} = \omega_r - \omega_0 \tag{2}$$

where H is the inertia constant, ω_0 is the rated synchronous speed, D is the damping factor, and P_G is the electrical machine power. The electrical machine power is a function of angle δ and depends on network topology. These functions must be characterized for the three stages that constitute the executed transient stability studies.

4.1.1. Before Fault

Before the fault, the system operates in a steady state or equilibrium state characterized by voltage $\hat{V}$, with power supplied $\hat{S}$ to the infinite bus. Generator internal voltage $\hat{E}$ ($\hat{E} = \hat{E}e^{j\delta}$) is determined by the instant generator power given by

$$P_G(\delta) = \frac{E.V}{X'_d + \frac{X_L}{2}}\sin(\delta) \tag{3}$$

4.1.2. During Fault

The fault is a three-phase symmetrical fault placed at power line L_2 after the CB, which is near Bus 1, and occurs at t = T_1. Considering the power system circuit represented in Fig. 8, the use of an inductive SSFCL design leads to the following generator power:

$$P_G(\delta) = 0 \tag{4}$$

However, in the case of a resistive SSFCL design, the generator power is

$$p_G(\delta) = R_{SC}.\frac{E^2}{R_{SC}{}^2 + X'^2_d} \tag{5}$$

Considering the power system circuit represented in Fig. 9, the equivalent circuit during the fault is demonstrated, where Z_{sc} characterizes the final SSFCL resistance or reactance.

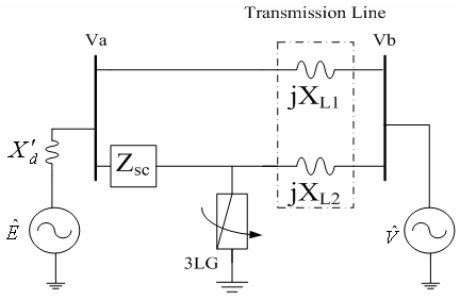


Fig. 9. Equivalent circuit during fault condition considering the SSFCL located in the feeder position of line L2

Applying the delta-wye transformation to the impedances occurring among Buses 1 and 2 and the fault point 3 lead to

$$Z_3 = Z_1 = \frac{X_L.Z_{SC}}{Z_{SC} + 2X_L} \;\; ; \;\; Z_2 = \frac{(X_L)^2}{Z_{SC} + 2X_L} \tag{6}$$

The equivalent circuit of Fig. 4 can be reduced to the one represented in Fig. 10 because $\hat{Z}_{th}$ and $\hat{V}_{th}$ denote Thévenin's impedance and voltage source equivalents, respectively.

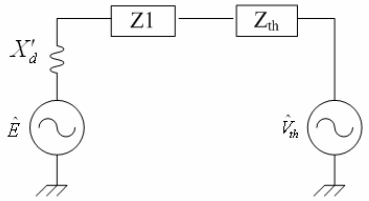


Fig. 10. Equivalent circuit reduced.

Thévenin's impedance and voltage source are determined using the following relations:

$$\hat{Z}_{th} = \frac{\hat{Z}_3.\hat{Z}_2}{\hat{Z}_3 + \hat{Z}_2} \tag{7}$$

$$\hat{V}_{th} = \hat{Z}_3.\frac{\hat{V}}{\hat{Z}_3 + \hat{Z}_2} = \hat{V}_{th}e^{j\alpha_{th}} \tag{8}$$

The generator power is given by

$$P_G(\delta) = \frac{\hat{E}^2}{Z_a}\cos(\Phi_a) - \frac{\hat{E}.V_{th}}{Z_a}\cos(\delta - \alpha_{th} + \Phi_{th}) \quad (9)$$

where

$$\hat{Z}_a = \hat{Z}_1 + \hat{Z}_{th} + jX'_d = Z_a e^{j\Phi a} \quad (10)$$

4.1.3. After Fault

The fault is cleared at t = T_2 by opening CB2 and CB4. The instant generator power is given by

$$P_G(\delta) = \frac{E.V}{X'_d + X_{L1}}\sin(\delta) \quad (11)$$

4.2. Simulation

Stable operation of the power system network is dependent on the balance of mechanical and electro-magnetic forces that keep the generators synchronized. When a power system is in normal condition, there is equilibrium between the consumed and produced power in this power system. When a large disturbance such as a short circuit or line tripping appears, this situation of synchronous equilibrium may momentarily or permanently damp oscillations, depending on the case. Thus, the power system transient stability problem is then determined to assess whether the power angle of the generator is able to keep or reach a new satisfactory steady-state operating point following the fault [17].

If the proposed SSFCL is used in the power system during a fault, theory and simulation results show that the transient stability of the system can be enhanced. Fig. 11

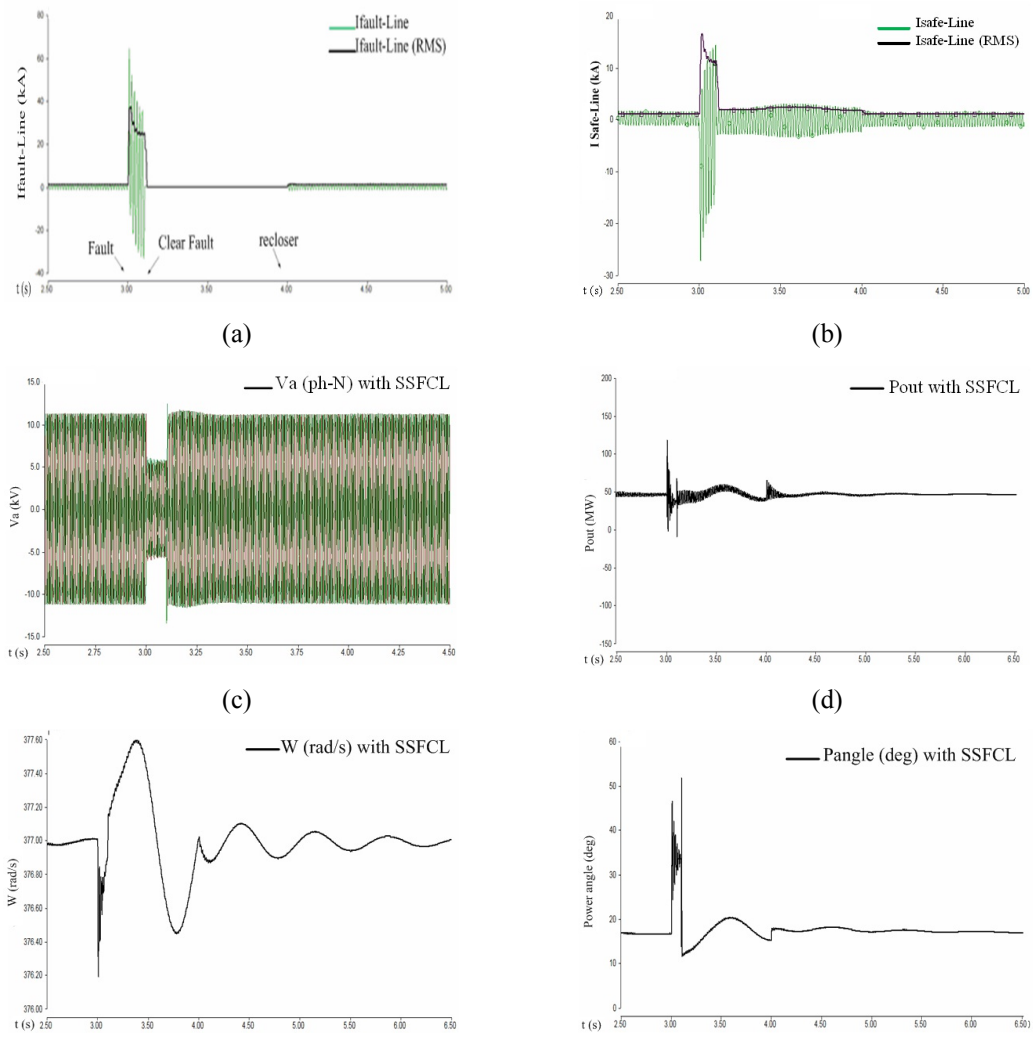


Fig. 11. Simulation result of (a) fault-line current, (b) safe-line current, (c) generator voltage, (d) output power, (e) rotor angle, and (f) rotor angle velocity of the generator of model SSFCL at the current-limiting operation (P_G = 50 MW, clearing time = 100 ms, 3LG fault)

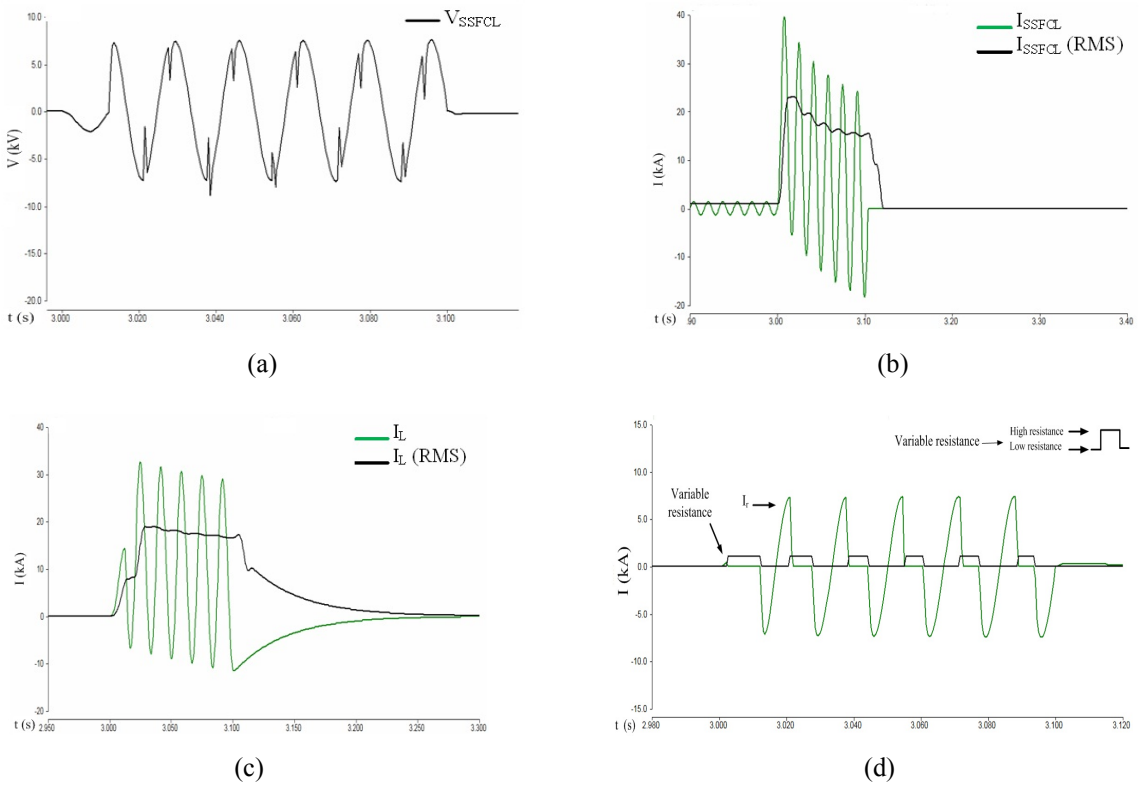


Fig. 12. The simulation results of (a) the voltage across the SSFCL, (b) current through the SSFCL, (c) current through the current-limiting reactor (L), and (d) current through the variable resistance (P_G = 50 MW, clearing time = 100 ms, 3LG fault)

shows a typical simulation result throughout the procedure: (from top to bottom) (a) fault-line current (kA), (b) safe-line current (kA), (c) generator voltage (kV), (d) output power of generator (MW), (e) rotor angle (deg), and (f) rotor angle velocity of the generator (rad/s). The operating conditions for the simulation are as follows: output power is 50 MW and clearing time is set at 100 ms. The fault occurs at 3 s and is cleared at 3.1 s. The fault line is reclosed at 4 s (Fig. 8). The SSFCL in the fault line works to restrict the current. In this case, the generator returns to the initial condition stably after the switching procedure. When the clearing time is longer, the generator steps out of and loses the synchronism.

Fig. 12 shows the A-phase voltage and currents of the proposed SSFCL in the simulation results shown in Fig. 11: (from top to bottom) (a) Voltage across the SSFCL (kV), (b) current through the SSFCL (kA), (c) current through the current-limiting reactor (L) (kA), and (d) current through the variable resistance (kA). Although all currents contain DC components, the SSFCL model operates according to the principle. Each time the current becomes less than the varistor current, the variable resistance goes into ON mode and the current sees through the variable resistance.

5. Results and Discussion

5.1. Current-limiting Performance

Fig. 13 shows the fault current of A phase with the SSFCL ($I_{\text{Fault-Line with SFCL}}$) and without the SSFCL ($I_{\text{Fault-Line without SFCL}}$) (Fig. 4). Although the RMS value of the fault current reaches nearly 30 kA without any SSFCL, the value is restricted less than 16 kA with the SSFCL. The capability of the SSFCL to restrict the fault current is not reduced by adding variable resistance.

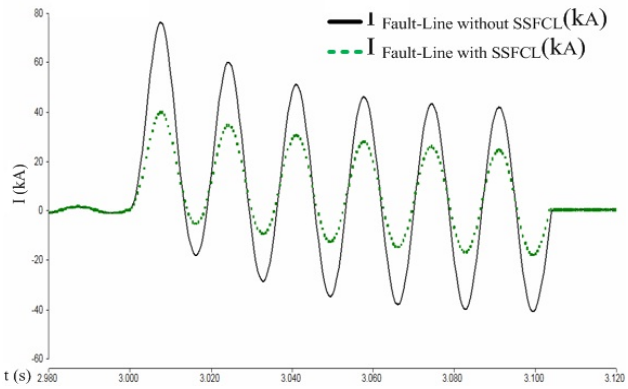


Fig. 13. Current through the A-phase line during the fault with SSFCL and without SSFCL (kA).

5.2. Voltage Drop Suppression During the Fault

The RMS value of Va in Fig. 8 with the SSFCL is approximately 0.7 PU during the fault (Fig. 14), whereas it is only 0.1 PU without any SSFCL. The ability of the SSFCL to suppress voltage drop is not degraded by attaching the variable resistance in parallel. Moreover, the surge voltages observed at the beginning of the current-limiting performance with SSFCL without variable resistance are eliminated with the SSFCL with variable resistance.

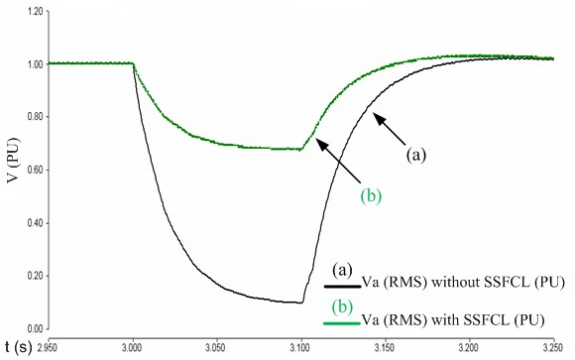


Fig. 14. RMS value of terminal voltage of generator (PU)

5.3. Effect of Energy Absorbed in Variable Resistance on Power System Stability, Load Angle, and Angular Velocity

Critical clearing time depends on the acceleration energy, which is the difference between the mechanical input energy and output electric energy of the generator at the fault. Fig. 15 shows the generator power during the fault. The electric energy transferred to the infinite bus is small without SSFCL because the generator voltage is low. However, the SSFCL suppresses the voltage drop; thus, the electric power can be transferred to a certain extent through the abovementioned transmission line. Moreover, the electric energy is consumed in the variable resistance of the SSFCL, and the acceleration energy is greatly diminished. Hence, critical clearing time with SSFCL is longer than that without the SSFCL or the SSFCL without variable resistance.

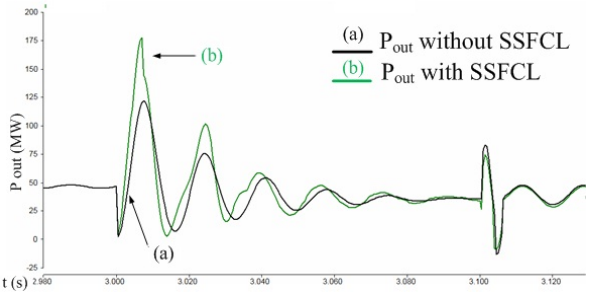


Fig. 15. The generator output change during the fault with 100 ms clearing time for the two cases (MW)

Fig. 16 shows the relation of the load angle and angular velocity. After initial operation, the system becomes stable at approximately 16.6 (deg) load angle and 120 π angular velocity. In steady-state normal operation, the three-phase fault breaks the synchronism of the load angle to over 90 (deg), which is the maximum load angle that the machine can sustain. After the fault, the machine goes out of control; however, is able to find a stable point at 98 (deg) through a hypothetical controller. The SSFCL is installed after the initial operation; thus, the system becomes stable at about 16.6 (deg) load angle and 120 π angular velocity. In the steady-state normal operation, when a fault occurs in three phases, the load angle maintains synchronism at 32 (deg), which is under the maximum load angle.

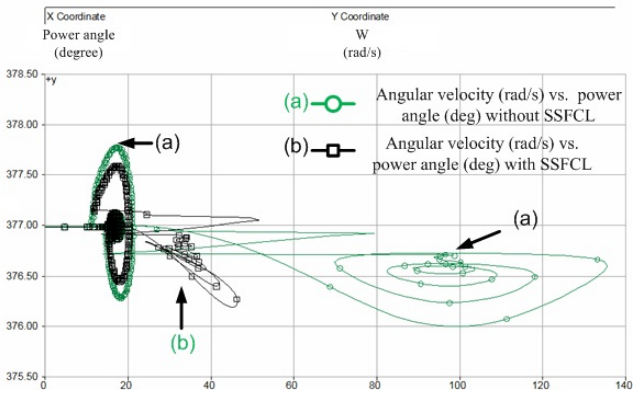


Fig. 16. Angular velocity vs. power angle graph in case of a three-phase fault in the model power system where (a) the SSFCL is not installed and (b) the SSFCL is installed

The rotor angular velocity of the generator at critical clearing time is shown in Fig. 17 in two cases: with SSFCL and without SSFCL. The generator accelerates most during the fault without the SSFCL and accelerates least with the SSFCL. Therefore, the proposed SSFCL enhances the stability of the power system by restraining the change of angular velocity.

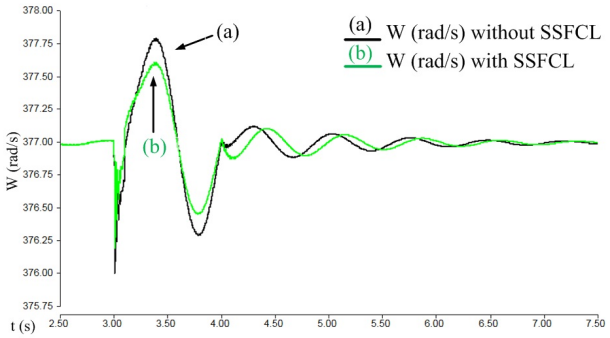


Fig. 17. The rotor angular velocity in two cases (rad/s)

The proposed SSFCL characterizes both the L-type and R-type FCLs.

6. Conclusion

A novel SSFCL is proposed in the present paper. The studies conducted in the present paper show the effect of a proposed SSFCL on power transient stability and power quality. Through the present study, the proposed SSFCL is demonstrated to restrict fault current and to protect the synchronization of generators. The capability of this SSFCL to diminish fault currents has an effect on synchronism. The SSFCL more efficiently protects synchronization, with three lines to a ground fault, compared with a system with any SSFCL. The first objective of an FCL is to protect devices such as CBs. However, if SSFCLs are installed in systems, other side effects are produced, as shown in the present study. We have considered a simple power system in the perspective of stability. The simulation study was performed to investigate power system characteristics of the proposed SSFCL, which consists of four diodes, one self-turn-off IGCT, a current-limiting by-pass reactor (L), and a variable resistance in parallel L. The present study had two goals: improve power system stability and prevent over-voltage across the SSFCL. The SSFCL consumes excessive energy in the variable resistance during the fault. The SSFCL has current-limiting characteristics of both the L-type and R-type FCLs. To determine how the voltage drop suppression and energy consumption feature of the proposed SSFCL influence power system stability, various parameters of power system were investigated. The proposed SSFCL has excellent characteristics in improving power system stability once the effects of voltage drop suppression and excessive energy consumption during the fault have manifested.

References

[1] Y. Shirai, K. Furushiba, Y. Shouno, M. Shiotsu, and T. Nitta, “Improvement of Power System Stability by Use of Superconducting Fault Current Limiter with ZnO Device and Resistor in Parallel,” *IEEE Transaction on Applied Superconductivity*, Vol. 18, No. 2, June 2008.

[2] Masaki Yagami, Junji Tamura, “Enhancement of Transient Stability Using Fault Current Limiter and Thyristor Controlled Braking Resistor,” *Power Tech*, 2007 IEEE Lausanne.

[3] Lin Ye, LiangZhen Lin and Klaus-Peter Juengst, “Application Studies of Superconducting Fault Current Limiters in Electric Power System,” *IEEE Trans. on Applied Superconductivity*, Vol. 12, No1, pp. 900−903, March 2002.

[4] Thomas P.Sheahen, “Introduction to High-Temperature Superconductivity,” *Plenum Press*, New York and London.

[5] W. Paul, M. Chen, M. Lakner, J. Rhyner, D. Braun, W. Lanz, M. Kleimaier, “Superconducting Fault Current Limiter Applications, technical and economical benefits, simulations and test results,” *CIGRÉ session* 2000, no 13−201.

[6] M.E. Almeida, C.S. Rocha, J.A. Dente, P.J. Costa Branco, “Enhancement of Power System Transient Stability and Power Quality using Superconducting Fault Current Limiters,” *Lisbon*, Portugal, March18−20, 2009.

[7] A. J. Power, “An Overview of Transmission Fault Current limiters,” Fault Current Limiters - A look at Tomorrow, *IEE Colloquium* on June 1995, pp 1/1−1/5.

[8] Takahiro Nomura, Mitsugi Yamaguchi and Satoshi Fukui et al, “Single DC reactor Type Fault Current Limiter for 6.6KV Power System,” *IEEE Trans. On Applied Superconductivity*, Vol.11, No.1, March 2001:2090−2093.

[9] R. F. Giese et al., “Assessment study of superconducting fault current limiters operation at 77K,” *IEEE Trans. Power Delivery*, vol. 8, no. 3,pp. 1138–1147, July 1993.

[10] R. K. Smith et al., “Solid state distribution current limiter and circuit breaker application requirements and control strategies,” *IEEE Trans. PWRD*, vol. 8, no. 3, pp. 1155–1164, July 1993.

[11] E. Thuries et al., “Toward the superconducting fault current limiter,” *IEEE Trans. Power Delivery*, vol. 6, pp. 801–808, Apr. 1991.

[12] M. Chen et al., “Fabrication and characterization of superconducting rings for fault current limiter application,” vol. 282–287, 1997.

[13] Gurjeet singh malhi, “Studies of fault current limiters for power systems protection", August, 2007.

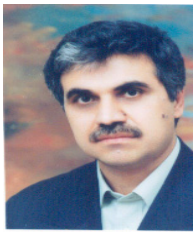
[14] Manish Verma, "A comprehensive overview, behavioral model and Simulation of a Fault Current Limiter ", June 29, 2009.

[15] K. Furushiba and Y. Shirai et al., “Power system characteristics of the SCFCL in parallel with a resistor and a ZnO device,” *IEEE Trans. Applied Superconductivity*, vol. 17, no. 2, pp. 1915–1918, June 2007.

[16] Zhengyu Lu, Daozhuo Jiang and Zhaolin Wu, “A New Topology of Fault-Current Limiter and Its Parameters Optimization.” *IEEE Power Electronics Specialists Conference*, PESC03.

[17] J. Machowski, Power System Dynamic and Stability: John Willey & sons press, 1997.

Alireza Fereidouni was born in Behshahr, Iran, in 1987. He received his B.Sc. degree in Electrical Engineering from Babol University of Technology, Babol, Iran, in 2009. He is currently an M.Sc. student in the Department of Electrical Engineering at Amikabir University of Technology, Tehran, Iran. His research interests are power system stability and protection, power electronics, and high voltage.



Behrooz Vahidi, was born in Abadan, Iran, in 1953. He received his B.S. degree in Electrical Engineering from Sharif University of Technology, Tehran, Iran, in 1980, his M.S. degree in Electrical Engineering from Amirkabir University of Technology, Tehran in 1989, and his Ph.D. degree in Electrical Engineering from the University of Manchester Institute of Science and Technology, Manchester, UK in 1997. From 1980 to 1986, he worked in the field of high voltage as a Chief Engineer. Since 1989, he has been with the Department of Electrical Engineering of Amirkabir University of Technology where he is currently a Professor. Prof. Vahidi is a senior member of IEEE. His main research interests are high voltage, electrical insulation, power system transient, lightning protection, and pulse-power technology. He has authored and co-authored more than 220 papers and 5 books on high-voltage engineering and power systems.

Tahoura Hoseini Mehr was born in Babol, Iran, in 1987. She received her B.Sc. degree in Electrical Engineering from Babol University of Technology, Babol, Iran, in 2009. She is currently an M.Sc. student in the Department of Electrical Engineering at Isfahan University of Technology, Isfahan, Iran. Her research interests are power electronics, electrical machines, and power system control and protection.

Mehdi Garmroodi Doiran was born in Tehran, Iran in 1986. He received his B.Sc. degree in Electrical Engineering from Sharif University of Technology, Tehran, Iran, in 2009. He is currently an M.Sc. student in the Department of Electrical Engineering at Amirkabir University of Technology, Tehran, Iran. His research interests are power system control and protection, power electronics, and power system transient stability.