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Accuracy Analysis of Extraction Methods for Effective Channel Length in Deep-Submicron MOSFETs

Ju-Young Kim, Min-Kwon Choi, and Seonghearn Lee

Abstract—**A comparative study of two capacitance methods to measure the effective channel length in deep-submicron MOSFETs has been made in detail. Since the reduction of the overlap capacitance in the accumulation region is smaller than the addition of the inner fringe capacitance at zero gate voltage, the capacitance method removing the parasitic capacitance in the accumulation region extracts a more accurate effective channel length than the method removing that at zero gate voltage.**

Index Terms—**MOSFET, effective channel length, capacitance, extraction, overlap, fringe**

I. INTRODUCTION

The effective channel length L_{eff} is determined by several capacitance methods using the gate-to-channel capacitance C_{GC}. For accurate extraction of C_{GC}, the extrinsic parasitic capacitance C_p outside the channel area should be eliminated from the measured gate capacitance C_G. Conventionally, the method removing C_p determined by C_G in the accumulation region at highly negative V_{GS} and another method removing C_p at V_{GS} = 0 V have been previously proposed to extract C_p [1-4]. By comparing these capacitance methods, it has been reported that the zero V_{GS} method is more accurate than the accumulation method as compared to the resistance method using long-channel MOSFETs with the mask gate length L_g of 2 – 10 μm [1, 2]. However, the resistance method may result in serious errors in the L_{eff} extraction of deep-submicron LDD MOSFETs with halo or pocket implants. As L_g is scaled down, C_p extraction errors of two methods are largely varied, because the inner fringe capacitance C_{if} contribution to C_p at V_{GS} = 0 becomes larger. Thus, the previous comparison results [1-4] may be invalid in deep-submicron MOSFETs.

Therefore, in this paper, using a reference method based on the intrinsic gate-bulk capacitance C_{GBI} measurements that do not need C_p extraction with unavoidable errors, the accuracy of two methods to extract L_{eff} in deep-submicron MOSFETs is compared and all internal components of C_p are analyzed in detail.

II. EXTRACTION

Using a SOLT(short-open-load-through) calibration method [5], On-wafer S-parameters were measured on bulk N-MOSFETs with 16 gate fingers of different L_g (=0.13, 0.18, 0.25 and 0.35 μm) and 2.5 μm unit finger width at V_{DS} = 0V with varying V_{GS} under common source-bulk configuration. The accurate de-embedding procedure using 'open' and 'short' test patterns was performed to remove pad and interconnection parasitics from the measured S-parameters [6].

In the low-frequency (LF) region, C_G can be determined by:

$$C_G = 2C_{GD} = (-2/\omega)\mathrm{Imag}(Y_{12})_{LF} \quad (1)$$

under the assumption of $C_{GD} = C_{GS}$ at V_{DS} = 0 V for MOSFETs with the symmetric drain and source structure. To satisfy the inversion condition of $V_{GS} > V_{TH}$ = 0.4 V,

Manuscript received May 9, 2011; revised May 31, 2011.
Department of Electronic Engineering, Hankuk University of Foreign Studies, San 89, Wangsan-ri, Mohyun-myun, Yongin, Kyungki-do 449-791, Korea
E-mail : shlee@hufs.ac.kr

$(-2/\omega)\mathrm{Imag}(Y_{12})$ data at V_{GS} = 0.5 V in Fig. 1 are used for the extraction of C_G. Fig. 2 shows C_G as a function of V_{GS} at different L_g to be used for extracting C_p.

In the conventional method based on C_p in the accumulation region, C_p values at various L_g are determined from measured C_G at V_{GS} = -1.5 V in Fig. 2 under the assumption of the flat band voltage V_{fb} = -1.5 V. The values of C_{GC} at various L_g are extracted by subtracting C_p at the same L_g in Fig. 2 from measured C_G at V_{GS} = 0.5 V. From the x-intercept of C_{GC} versus L_g at V_{GS} = 0.5 V in Fig. 3, ΔL (= L_g – L_{eff}) using the accumulation method is extracted to be 0.0509 μm.

In another conventional method to extract ΔL based on C_p at V_{GS} = 0 V, C_{GC} values at various L_g are extracted by subtracting C_p of C_G at V_{GS} = 0V in Fig. 2 from measured C_G at V_{GS} = 0.5 V. Using this zero V_{GS} method, ΔL of 0.0757 μm that is much larger than that of the accumulation method is determined from the x-intercept of C_{GC} versus L_g at V_{GS} = 0.5 V in Fig. 3.

In order to compare the accuracy of these conventional methods [1-4], a reference method [7] based on a V_{GS}-dependent curve of extracted C_{GBI} to extract the metallurgical channel length L_{met} is performed as follows:

The total gate-bulk capacitance C_{GB} at V_{DS} = 0 V is determined by [7]

$$C_{GB} = (1/\omega)\mathrm{Imag}(Y_{11} + 2Y_{12})_{LF} \tag{2}$$

Since C_{GBI} is masked at $V_{GS} > V_{TH}$, the extrinsic gate-bulk capacitance C_{GBE} is accurately extracted by measuring C_{GB} of Eq. (2) at V_{GS}=0.5 V > V_{TH}=0.4 V. Thus, C_{GBI} at $V_{GS}<V_{TH}$ is determined by $C_{GB} – C_{GBE}$. The V_{GS}-dependent data of the source-drain overlap and depletion length $L_{OD}(=2L_{ov}+2L_{de})$ where L_{ov} is the source/drain overlap length and L_{de} is the source/drain depletion length are extracted from the x-intercepts of the regression lines for C_{GBI} versus L_g in Fig. 4. The metallurgical channel length reduction ΔL_{met} (= L_g – L_{met}) is determined by $2L_{ov}$ = 0.0577 μm at V_{GS} = –1.5 V where the decreasing rate of L_{OD} with increasing $|V_{GS}|$ is maximum [7]. This value of V_{GS} = –1.5 V is the boundary voltage between the accumulation and

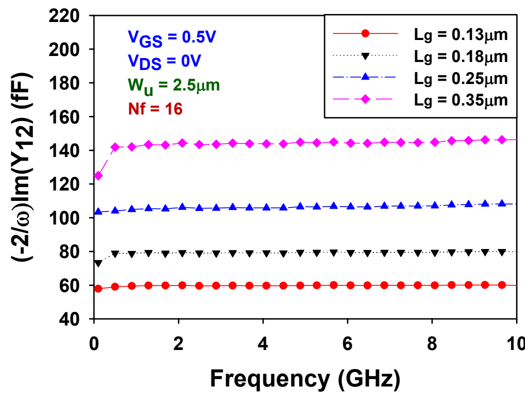

Fig. 1. Measured $(-2/\omega)\mathrm{Imag}(Y_{12})$ vs. frequency at various L_g.

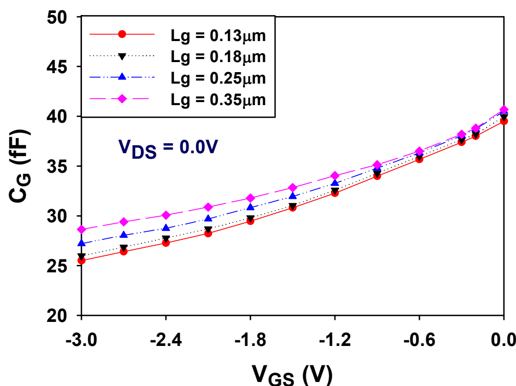

Fig. 2. The V_{GS}-dependence of C_G at various L_g.

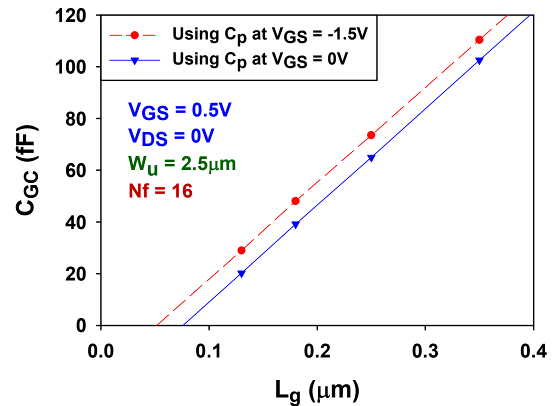

Fig. 3. Extracted C_{GC} versus L_g using conventional methods.

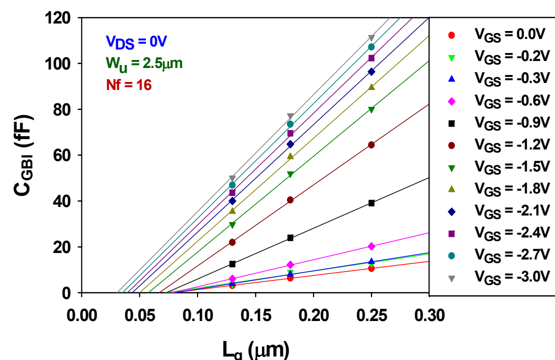

Fig. 4. Extraction data of C_{GBI} versus L_g at different V_{GS}.

depletion regions, verifying the previous assumption of V_{fb} = -1.5 V. This method is used as a reference for the accuracy analysis because C_p extraction with unavoidable errors is not required.

As a result, much closer ΔL to ΔL_{met} is obtained for the accumulation method than the zero V_{GS} one. This indicates that the accumulation method is more accurate for extracting L_{eff} in deep-submicron MOSFETs than the zero V_{GS} one.

III. Analysis

In order to find the exact cause for the better accuracy of the accumulation method than the zero V_{GS} one, all internal components of C_p determined by these methods are accurately extracted.

In the inversion region, C_p is defined as C_{ov} + C_{of} where C_{ov} is the source-drain overlap capacitance and C_{of} is the outer fringing capacitance. Using the linear regression of C_G versus L_g, C_p is extracted by finding C_G at $L_g = 2L_{ov}$ where C_{GC} disappears. Thus, C_p at V_{GS} = 0.5 V is extracted to be 32.5 fF in Fig. 5. As shown in Fig. 2, C_G increases slightly with increasing L_g at negative V_{GS}, because of the increase of C_{of}. Thus, in Fig. 5, C_p values at $L_g = 2L_{ov}$ to keep the same C_{of} as that in the inversion region are extracted to be 30.0 fF and 39.3 fF at V_{GS} = -1.5 V and V_{GS} = 0 V, respectively.

Since C_{of} is independent of V_{GS}, the C_p variation of ΔC_p = 2.5 fF from V_{GS} = 0.5 V to V_{GS} = -1.5 V is attributed to the decrease of C_{ov} caused by the expanded depletion width of n^- overlap region at more negative V_{GS}. However, the inner fringe capacitance C_{if} is added to C_p (=C_{ov} + C_{of}) at V_{GS} = 0 V, because the bottom of the gate is not screened from the inner side wall of the source/drain overlap regions due to the absence of the inversion or accumulation layers under the gate oxide [8]. Since C_{ov} keeps constant at positive V_{GS} due to the accumulation of n^- overlap region, ΔC_p of 6.7 fF from V_{GS} = 0.5 V to V_{GS} = 0 V is due to the addition of C_{if} at V_{GS} = 0 V. Thus, the error of the accumulation method due to the C_{ov} reduction is smaller than that of the zero V_{GS} method due to the addition of C_{if}.

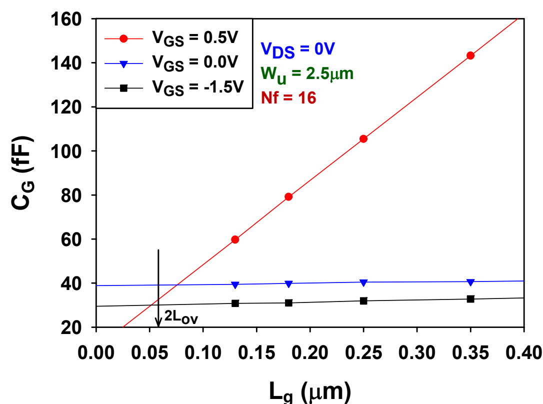

Fig. 5. Measured data and regression line of C_G versus. L_g at different V_{GS}.

IV. Conclusions

As compared with the C_{GBI} method without C_p extraction with unavoidable errors, it is found that the accumulation method is more accurate in extracting L_{eff} in deep-submicron MOSFETs than the zero V_{GS} one. This result is justified by analyzing all internal components of extrapolated C_p at $L_g = 2L_{ov}$.

Acknowledgments

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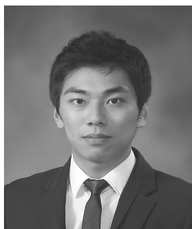
Ju-Young Kim was born in Seoul, Korea, in 1983. He received the B.S. degree in electronic engineering in 2010 from the Hankuk University of Foreign Studies, Yongin, Korea, where he is currently working toward the M.S. degree in electronic engineering in the Department of Electronic Engineering.
His current research work is focused on RF CMOS device characterization and modeling.



Min-Kwon Choi was born in Seoul, Korea, in 1983. He received the B.S. degree in electronic engineering in 2010 from the Hankuk University of Foreign Studies, Yongin, Korea, where he is currently working toward the M.S. degree in electronic engineering in the Department of Electronic Engineering.
His research areas are RF CMOS compact modeling and parameter extraction for RF circuit design.

Seonghearn Lee was born in Junjoo, Korea, in 1962. He received the B.E. degree in electronic engineering in 1985 from Korea University, Seoul, Korea, and the M.S. and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis, in 1989 and 1992, respectively. His doctoral dissertation work involved the design, fabrication, and parameter extraction of AlGaAs/GaAs heterojunction bipolar transistors.
From 1992 to 1995, he was a Senior Member of the Research Staff with the Semiconductor Technology Division, Electronics and Telecommunications Research Institute, Taejon, Korea, where he worked on the development of polysilicon emitter bipolar transistors and Si/SiGe/Si heterojunction bipolar transistors. Since 1995, he has been with the Department of Electronic Engineering, Hankuk University of Foreign Studies, Yongin, Korea, where he is currently a Professor. Since 1996, he has carried out research on RF CMOS and bipolar modeling and parameter extraction for the RF circuit design in wireless communications applications. His research interests are in the field of design, modeling, and characterization of silicon and compound semiconductor devices for use in high-frequency integrated circuits.
Prof. Lee is a senior member of the IEEE Electron Devices Society and a member of the Institute of Electronics Engineers of Korea. He received the HUFS Excellence in Research Award from the Hankuk University of Foreign Studies, in 2001, 2003, and 2004. He has been listed in *Who's Who in the World* and *Who's Who in Asia*.