A 6b 1.2 GS/s 47.8 mW 0.17 mm^2 65 nm CMOS ADC for High-Rate WPAN Systems

Hye-Lim Park*, Yi-Gi Kwon*, Min-Ho Choi*, Younglok Kim*, Seung-Hoon Lee*, Young-Deuk Jeon, and Jong-Kee Kwon****

Abstract—**This paper proposes a 6b 1.2 GS/s 47.8 mW 0.17 mm^2 65 nm CMOS ADC for high-rate wireless personal area network systems. The proposed ADC employs a source follower-free flash architecture with a wide input range of 1.0 V_{p-p} at a 1.2 V supply voltage to minimize power consumption and high comparator offset effects in a nanometer CMOS technology. The track-and-hold circuits without source followers, the differential difference amplifiers with active loads in pre-amps, and the output averaging layout scheme properly handle a wide-range input signal with low distortion. The interpolation scheme halves the required number of pre-amps while three-stage cascaded latches implement a skew-free GS/s operation. The two-step bubble correction logic removes a maximum of three consecutive bubble code errors. The prototype ADC in a 65 nm CMOS demonstrates a measured DNL and INL within 0.77 LSB and 0.98 LSB, respectively. The ADC shows a maximum SNDR of 33.2 dB and a maximum SFDR of 44.7 dB at 1.2 GS/s. The ADC with an active die area of 0.17 mm^2 consumes 47.8 mW at 1.2 V and 1.2 GS/s.**

Index Terms—**ADC, 65 nm, flash, GS/s, low power**

I. INTRODUCTION

With the increased multimedia service and the spread of portable devices, the demand for high-speed data communication based on wireless networks has been increased. As a result, the high-rate wireless personal area network (WPAN) systems such as IEEE 802.15.3 for communication between fixed and portable electronic devices within about 10-meter area have been widely developed. Particularly, the analog-to-digital converters (ADCs) for the ultra wide band (UWB) communication system with a data transfer rate of 480 Mbps require a resolution of 6b and a conversion rate exceeding 1 GS/s with low power and small chip area, simultaneously.

On the other hand, the ADC designs in nanometer-scale CMOS technologies encounter several limitations such as insufficient voltage headroom, switch linearity degradation, low amplifier gain, and high offsets [1, 2]. Especially, a reduced input signal range and high comparator offsets at a low supply voltage affect the overall performance of high-speed ADCs [3-5]. In case of flash-type ADCs commonly used for high speed conversion with a sampling frequency exceeding several hundreds of MHz, comparators determines most of the overall ADC power dissipation since the number of comparators is exponentially increased with a resolution. The design targets of comparators are based on resolution, operating speed, input signal range, and offsets caused by device mismatch. The comparator offsets are proportional to the square of A_{Vt} and A_β, the device mismatch parameters of threshold voltage and mobility, and inversely proportional to the size of MOS transistor [3]. Although the device mismatch parameters have been improved considerably in the latest process technologies, the offsets by device mismatch have been rather increased due to the reduced size of MOS transistors [4]. Moreover, the input signal range has been decreased due to the reduced voltage headroom [1] while

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the parasitic capacitance of MOS transistors has been increased with a shrinking gate oxide thickness. As a result, the design targets of comparator tend to be more and more rigorous in a scaled-down process. Therefore, high-speed flash ADCs based on a lot of comparators have little benefits for power consumption in advanced CMOS technologies [3].

A few of flash ADCs based on a digital calibration have been recently reported partly to solve the problems [4, 6]. Comparators are designed with a minimum size to reduce the overall ADC power consumption while the increased offsets are calibrated by digital techniques. However, a long calibration time is needed to calibrate many comparators and the required chip area is increased with complicated digital logic circuits. On the other hand, time-interleaved successive approximation register (SAR) type ADCs primarily based on digital circuits have been widely developed for high-speed ADCs [7-9]. Since a single SAR ADC has only one comparator, power dissipation can be greatly reduced. However, each ADC needs external high-frequency clocks and extra calibration logic to reduce mismatch between channels.

This work proposes a low-power 6b 1.2 GS/s 65 nm flash ADC without any calibration scheme. The proposed ADC does not employ front-end source followers with a 1.0 V_{p-p} wide input range at a 1.2 V supply to minimize the effect of comparator offsets and to reduce power consumption. The source follower-free track-and-hold circuits (T/Hs), the differential difference amplifiers (DDAs) with active loads in pre-amps of comparator, and the distributed and output averaged layout scheme are employed to handle a wide-range input with low distortion. The three-stage cascaded latches eliminate the digital code errors caused by a time delay in digital combinational logic while the two-step bubble correction logic removes comparator bubble code errors.

This paper is organized as follows. The proposed ADC architecture is discussed in Section II while Section III describes a detailed circuit implementation. Measured performances are summarized in Section IV and Section V concludes the paper.

II. Proposed ADC Architecture

The proposed ADC for high-rate WPAN systems is based on a full flash architecture to obtain a 6b resolution and a 1.2 GS/s sampling rate as illustrated in Fig. 1.

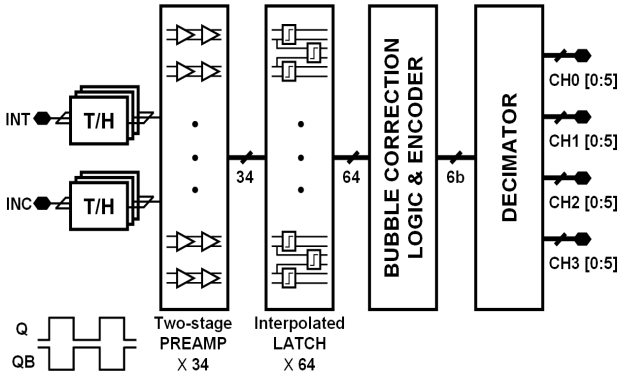


Fig. 1. Proposed 6b 1.2 GS/s 65 nm CMOS ADC.

The distributed T/Hs without source followers are employed for stable operation at GS/s level with low power while the outputs from each T/H are combined together to average the output difference caused by device mismatch. The interpolation technique reduces power consumption and chip area. The proposed ADC decides 5b from 34 pre-amps and obtains an extra 1b with 64 interpolated digital latches. Furthermore, the input capacitance of the ADC is reduced by interpolation so that the sampling capacitor can be maximized for the low kT/C noise. The specified total input capacitance in this work is 2 pF. The comparator pre-amps are based on a two-stage amplifier for a high DC gain while the clock-free DDA is employed in the first stage of each pre-amp for GS/s operation. The encoder circuit with the quasi-Gray coding scheme and bubble correction minimizes digital code errors. The on-chip decimator down-samples digital outputs by a maximum factor of sixteen with 4 channels to minimize high-frequency noise coming from the measurement board and to meet the system timing requirements.

III. Circuit Implementation

1. High-speed Passive Track-and-hold Circuit (T/H)

The proposed 6b 1.2 GS/s 65 nm ADC needs a high-speed T/H to achieve a 6b-level accuracy even at a Nyquist input frequency of 600 MHz. Of various T/H architectures, the T/H composed of sampling capacitors, sampling and dummy switches, and source followers has been commonly employed. In the conventional T/H, the switch and clock feed-through errors during the mode transition from sampling to holding and the signal distortion caused by the source followers degrade the

overall ADC linearity [10]. Particularly, the source followers show a critical signal distortion with an increasing input signal range and dissipate more power with an increasing sampling rate.

In this work, a passive T/H without using source followers, as illustrated in Fig. 2, reduces the signal distortion of a GS/s-level wide-range input of 1.0 $V_{p\text{-}p}$ with low power dissipation. The input capacitance of the passive T/H is designed to have a required system specification of 2 pF while the number of pre-amps is halved by employing the well-known interpolation technique [11].

The clocks, QD and QDB, for the T/H are slightly delayed with inverters, compared to the latch clocks, Q and QB, for comparator latches accurately to latch a held input at 1.2 GS/s just before the T/H is tracking a new input. The clock feed-through errors are minimized with the properly sized dummy switches while the non-linearity of analog input switches in a nanometer-scale technology is reduced by using the MOS transistors with a low-threshold voltage.

On the other hand, when the T/H is laid out, the different line lengths from the T/H to each comparator can cause different line parasitic components and degrade the ADC linearity. The prototype ADC divides the T/H into three sub-blocks considering a system complexity while the output difference of the locally distributed three T/Hs is averaged out by combining the outputs of each T/H together, as shown in Fig. 3. The proposed layout scheme improves the T/H accuracy considerably.

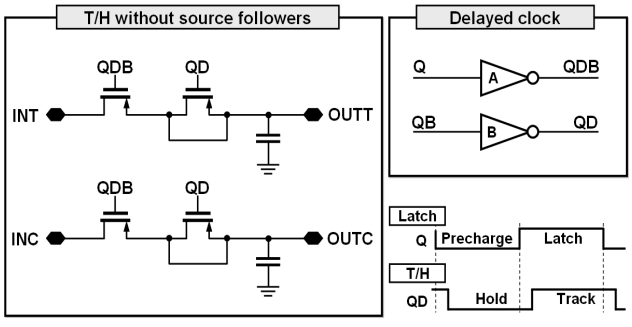


Fig. 2. T/H and delayed clocks without source followers.

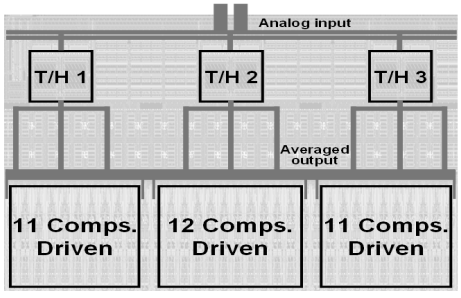


Fig. 3. Distributed and output averaged layout in the T/H.

2. High-speed Comparator with a Wide Input Range

The comparator for high-speed flash ADCs commonly consists of pre-amp and latch. The DDA as illustrated in Fig. 4 has been used as the first-stage pre-amp of a high-speed comparator since it operates at high speed without the glitch noise and gain reduction due to sampling switches and capacitors [10, 12]. At the output of the DDA, passive resistors or diode-connected MOS transistors are usually employed to obtain the required DC gain and bias voltage.

The DC gain and output bias voltage of the pre-amp in Fig. 4 are calculated as Eqs. (1, 2), respectively, while the required input signal range is derived as Eqs. (3, 4) to operate all the transistors in the saturation region.

$$A_{0,DDA} \approx -g_{m,MN1} R_{D1} \tag{1}$$

$$V_{DC,TN1} = V_{DC,TP1} = V_{DD} - I_{MN5} R_{D1} \tag{2}$$

$$V_{G,MN1} < V_{DC,TN1} + V_{thn,MN1} \tag{3}$$

$$V_{G,MN1} > V_{G,MN5} + \sqrt{\frac{I_{MN5}}{k_n'(W/L)_{MN1}}} \tag{4}$$

Although a large load resistance increases the DC gain, it also lowers the output bias voltage resulting in a limited input signal range. Therefore, the input signal

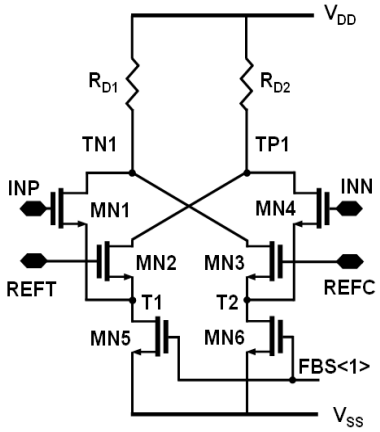


Fig. 4. Conventional differential difference amplifier (DDA).

range used for high-speed flash ADCs has been usually limited to about a half of a supply voltage [10, 13-15]. The proposed ADC employs a comparator of Fig. 5(a) to handle a wide-range input signal of 1.0 $V_{p\text{-}p}$ at a 1.2 V supply voltage. The first pre-amp is a DDA while the second pre-amp is a conventional amplifier with active loads. The output of the comparator latch is connected to cascaded digital latches as shown in Fig. 5(b).

The proposed two-stage pre-amp achieves the required DC gain for a 6b accuracy at an operating speed of 1.2 GS/s. The pre-amp output consists of PMOS transistors connected in a diode and PMOS transistors operating as a current source [16]. The DC gain and output bias voltage of the first-stage pre-amp are derived as Eqs. (5, 6), respectively, while the input signal range is determined by Eqs. (3, 4). Thus the required design target of the pre-amp can be obtained by properly sizing input and diode-connected transistors with the bias voltages, FBS<0:1>, controlled. The second-stage pre-amp is designed in the same procedure. As shown in the shaded voltage (LTV) are partially employed in the comparator box of Fig. 5(a), the MOS transistors with a low-threshold to achieve high enough voltage headroom and reduced parasitic capacitances at the nodes TN1 and TP1.

$$A_{0,DDA} \approx -\frac{g_{m,MN1}}{g_{m,MP1}} = -\frac{\sqrt{k_n'(W/L)_{MN1} I_{MN5}}}{\sqrt{2k_p'(W/L)_{MP1}(I_{MN5}-I_{MP2})}} \quad (5)$$

$$V_{DC,TN1} = V_{DC,TP1} = V_{DD} - |V_{thp,MP1}| - \sqrt{\frac{2(I_{MN5}-I_{MP2})}{k_p'(W/L)_{MP1}}} \quad (6)$$

The comparator drives the back-end bubble correction logic for encoding and error correction, as shown in Fig. 6, while the comparator holds its output during a maximum half clock period. Two cascaded latches, latch1 and latch2, are inserted between the differential comparator latch and the bubble correction logic for robust operation since the delay time of the combinational logic is very critical at 1.2 GS/s with this specific 65 nm CMOS. During the first clock period, the first cascaded latch1 tracks and holds the comparator latch output, while the second cascaded latch2 tracks the output of the first cascaded latch1. During the next clock period, the second cascaded latch2 holds the previous

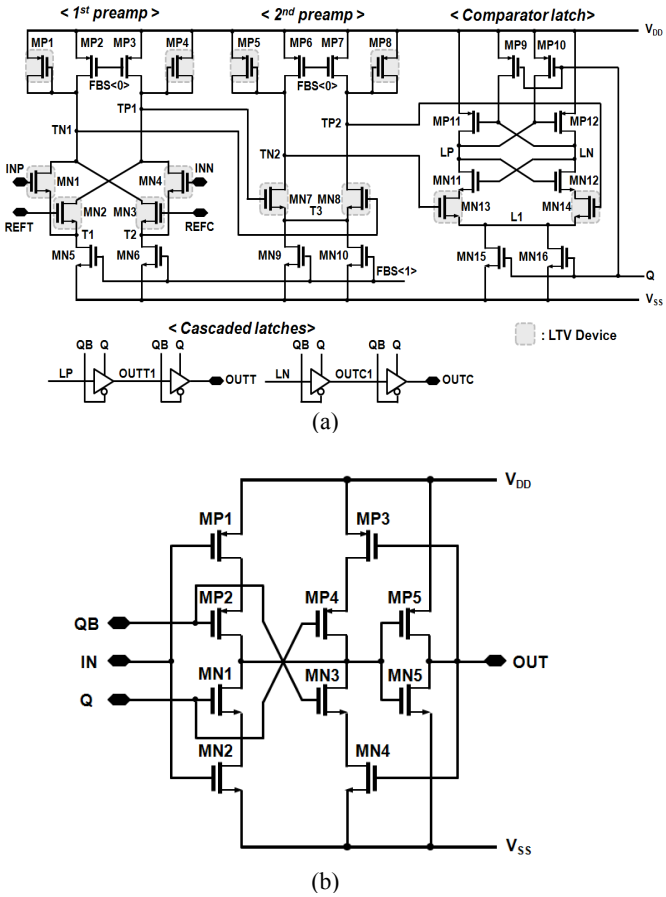


Fig. 5. (a) Proposed high-speed comparator with a wide input range and (b) Digital cascaded latch circuit.

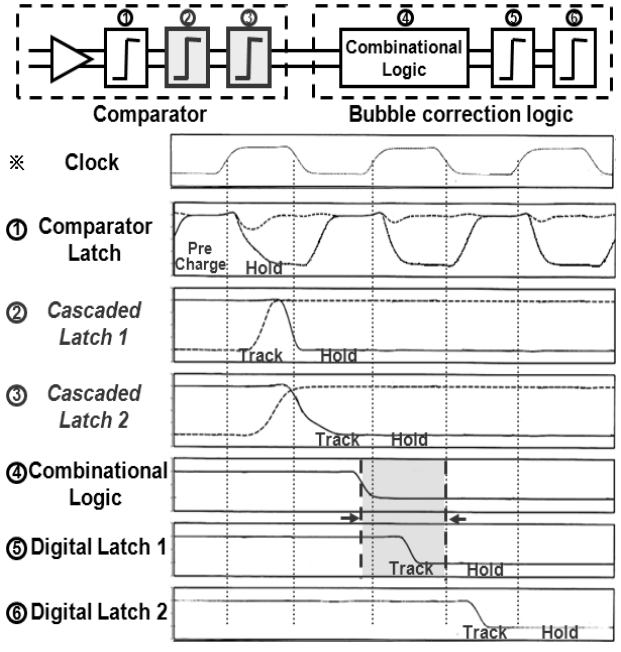


Fig. 6. Simulated comparator based on cascaded latches.

latch output and the digital latch1 in the bubble correction logic tracks the output of the combinational logic. On the other hand, the valid output of the combinational logic is applied to the digital latch1 before the digital latch1 tracks the output of the combinational logic. In other words, a sufficient setup time is secured with the extra cascaded latches for a stable high-speed operation without errors.

3. Encoder for Error Correction

The proposed ADC implements bubble correction logic to remove comparator bubble code errors as illustrated in Fig. 7 [17]. The bubble correction logic in a two-step voting process can correct maximum three consecutive bubble code errors. While the ADC is encoding the thermometer code to the binary code at 1.2 GS/s, digital code errors can occur by ripple propagation and glitch energy. The Gray code has been commonly used to minimize the digital code errors. However, the Gray code has a long gate delay due to complicated logic gates. In the proposed ADC, the quasi-Gray code with simple logic gates is employed to minimize the digital code errors and to reduce the gate delay [10].

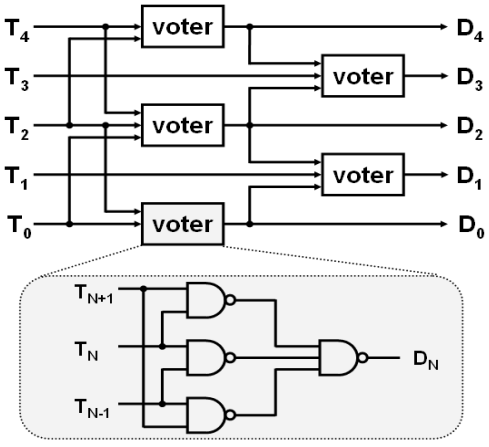


Fig. 7. Bubble correction logic in a two-step voting process.

IV. Prototype ADC Measurements

The prototype 6b 1.2 GS/s flash ADC is implemented in a 65 nm CMOS process. The ADC and internal clock buffers occupy an active die area of 0.17 mm^2 and 0.006 mm^2, as shown in Fig. 8, and dissipates 47.8 mW and 6.2 mW, respectively, at 1.2 V and 1.2 GS/s.

As demonstrated in Fig. 9, the measured differential non-linearity (DNL) and integral non-linearity (INL) are within 0.77 LSB and 0.98 LSB, respectively. At a clock frequency of 1.2 GHz, the measured signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 30.3 dB and 41.7 dB, respectively, with a 600 MHz input, as plotted in Fig. 10. The measured digital outputs are down-sampled by a factor of sixteen based on the on-chip decimator.

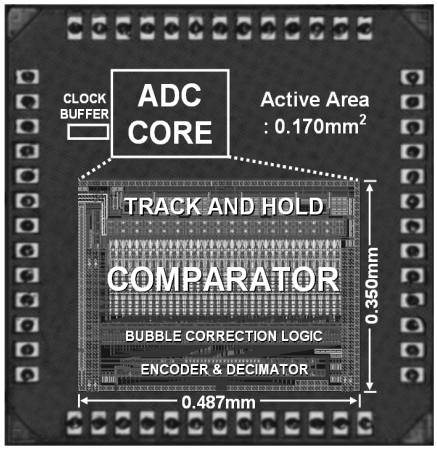


Fig. 8. Die photograph and layout of the prototype 6b 1.2 GS/s ADC (0.487 mm × 0.350 mm).

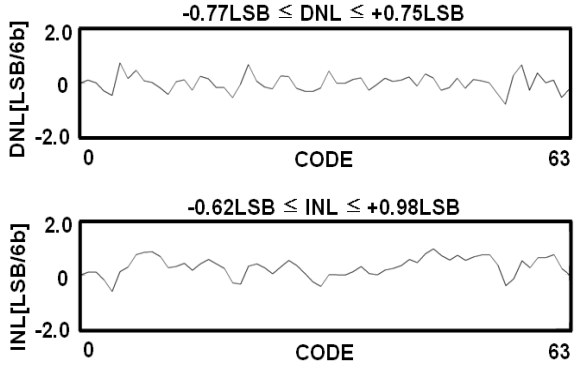


Fig. 9. Measured DNL and INL of the prototype ADC.

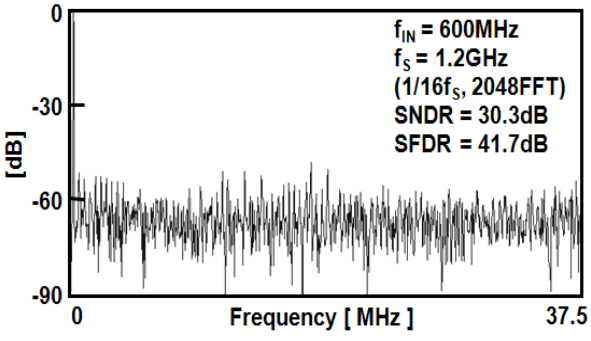
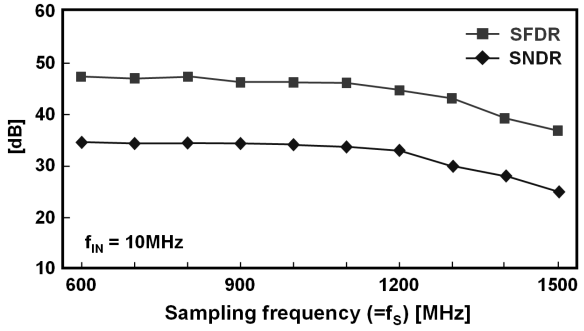


Fig. 10. Measured FFT spectrum of the ADC (1/16f_S down sampled).

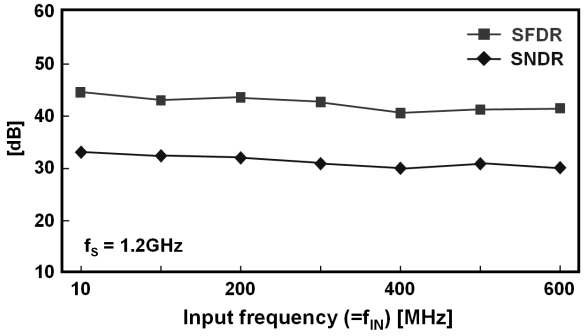
The SNDR and SFDR of Fig. 11(a) are measured with different sampling frequencies up to 1.5 GS/s at a 10 MHz input signal. The SNDR and SFDR are maintained over 33.2 dB and 44.7 dB, respectively, up to 1.2 GS/s. The SNDR and SFDR of the ADC are maintained above 30.3 dB and 40.8 dB, respectively, up to the Nyquist input frequency of 600 MHz at a 1.2 GHz sampling rate as shown in Fig. 11(b).

The overall ADC performance is summarized in Table 1 and the recently reported 6b flash ADCs with a sampling clock rate exceeding 0.8 GS/s are compared with the proposed ADC in Table 2. The figure of merits (FoM) is defined as Eq. (7). The proposed 6b 1.2 GS/s CMOS ADC has an input range of 1.0 V_{p-p} at a supply voltage of 1.2 V and dissipates low power without any extra calibration circuit.

$$FoM = \frac{Power}{2^{ENOB} \times f_S} \tag{7}$$



(a)



(b)

Fig. 11. Measured SFDR and SNDR of the ADC versus (a) f_S and (b) f_{IN}.

Table 1. Performance summary of the prototype ADC

Resolution	6bits
Conversion Rate	1.2GSample/s
Process	65nm CMOS
Supply	1.2V
Input Range	1.0Vp-p
DNL	-0.77LSB / +0.75LSB
INL	-0.62LSB / +0.98LSB
SNDR	33.2dB (at f_{IN}=10MHz) / 30.3dB (at f_{IN}=600MHz)
SFDR	44.7dB (at f_{IN}=10MHz) / 41.7dB (at f_{IN}=600MHz)
ADC Core Power	47.8mW
Active Die Area	0.170mm^2 (= 0.487mm × 0.350mm)

Table 2. Performance comparison of the recently reported 6b 1 GS/s level flash ADCs

	Speed (GS/s)	Supply (V)	Input range (V_{p-p})	Power (mW)	SNDR (dB)	FoM (pJ/conv)	Process (CMOS)
This work	1.2	1.2	1.0	47.8	33.2	1.07	65nm
[4]	0.8	1.2	-	12	35.7	0.30	65nm
[14]	0.9	3.3	1.0	300	35.8	6.62	0.35um
[13]	1.2	1.5	1.0	160	36.1	2.56	0.13um
[12]	1.3	1.8/2.5	-	600	33.2	12.36	0.25um
[10]	1.3	3.3	1.6	545	34.9	9.23	0.35um
[15]	1.6	1.8	0.8	85	35.2	1.13	0.18um
[16]	1.6	1.8	1.0	350	35.8	4.34	0.18um

V. CONCLUSIONS

This work describes a 6b 1.2 GS/s 65 nm CMOS flash ADC for high-rate WPAN systems such as the IEEE 802.15.3 standard. Several circuit design techniques are employed to achieve the required specifications in a 65 nm CMOS process. The distributed and output-averaged T/Hs without source followers and the DDA-based pre-amps with active loads properly handle a 1.0 V_{p-p} input signal at a 1.2 V supply with low distortion and low power dissipation. The interpolation technique minimizes the input capacitance and chip area while the cascaded latches and the encoder based on bubble correction, and the quasi-Gray coding scheme are employed for robust error-free operation at 1.2 GS/s. The prototype ADC implemented in a 65 nm CMOS demonstrates a

measured DNL and INL within 0.77 LSB and 0.98 LSB, respectively. The ADC with an active die area of 0.17 mm^2 shows a maximum SNDR and SFDR of 33.2 dB and 44.7 dB, respectively, and a power dissipation of 47.8 mW at 1.2 V and 1.2 GS/s.

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