Design of 1-Kb eFuse OTP Memory IP with Reliability Considered

Jeong-Ho Kim, Du-Hwi Kim, Liyan Jin, Pan-Bong Ha, and Young-Hee Kim

***Abstract*—In this paper, we design a 1-kb OTP (One-time programmable) memory IP in consideration of BCD process based EM (Electro-migration) and resistance variations of eFuse. We propose a method of precharging BL to VSS before activation of RWL (Read word-line) and an optimized design of read NMOS transistor to reduce read current through a non-programmed cell. Also, we propose a sensing margin test circuit with a variable pull-up load out of consideration for resistance variations of programmed eFuse. Peak current through the non-programmed eFuse is reduced from 728 μA to 61 μA when a simulation is done in the read mode. Furthermore, BL (Bit-line) sensing is possible even if sensed resistance of eFuse has fallen by about 9 kΩ in a wafer read test through a variable pull-up load resistance of BL S/A (Sense amplifier).**

***Index Terms*—eFuse, OTP, electro-migration, variable pull-up resistance**

I. INTRODUCTION

NVM (Non-volatile memory) for power management IC (PMIC) is generally eFuse (Electrical fuse) type or antifuse type OTP (One-time programmable) memory which is small-area and does not require optional processes instead of EEPROM or flash memory [1, 2]. The OTP memory of antifuse type is programmed by electrically shorting with a breakdown mechanism when a high voltage is applied to thin gate oxides [3]. In contrast, the OTP memory of eFuse type is programmed by flowing an over-current through the eFuse using VIO (I/O voltage) voltage [4]. The eFuse-type OTP memory is generally applied to perform analog trimming as a small-density memory.

As shown in Fig. 1, a conventional eFuse cell consists of an eFuse link, a program NMOS transistor with large channel width (MN1) which can flow large current, and a read NMOS transistor with small channel width (MN2) which can reduce read current in the read mode. The width of eFuse link using an n-poly silicon gate is 0.18 μm, the minimum width of 0.18 μm BCD process.

In the conventional BL S/A (Bit-line sense amplifier), BL is precharged to VDD before reading out an eFuse cell. In case of reading a non-programmed eFuse cell, RWL (Read word-line) is activated from 0 V to VDD and VDD, namely the precharging voltage of the BL, is discharged to 0 V through the read NMOS transistor and the eFuse link. Then, the eFuse link can be blown by the EM (Electro-migration) phenomenon since large-density current can flow the eFuse link of narrow width. Fig. 2

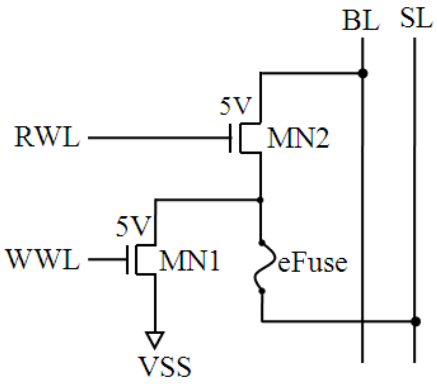

Fig. 1. Circuit of eFuse OTP memory cell.

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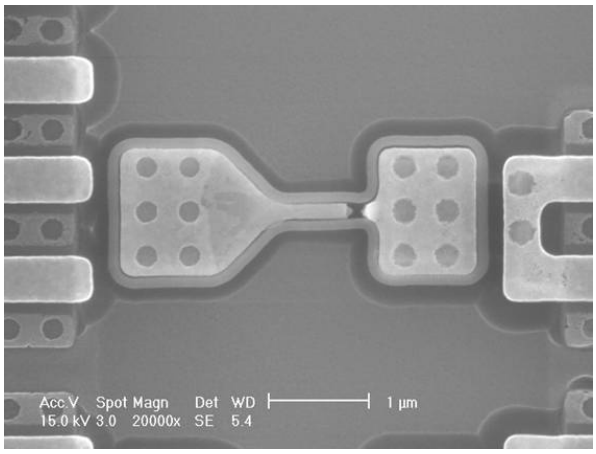

Fig. 2. SEM image of the failed eFuse link by EM.

shows a SEM image of a failed eFuse by EM in reading a non-programmed cell. Also, the resistance of programmed eFuse can vary below the minimum resistance that can be sensed during use in the field when the eFuse link is programmed with its resistance around the minimum resistance. Then, a data sensing failure can happen as well. Thus, it is required to design eFuse-type OTP memory IPs in consideration of sufficient reliability such as EM and data retention characteristics in PMICs.

In this paper, we propose a method of precharging BL to VSS before activation of RWL and an optimized design of the read NMOS transistor to reduce read current through the non-programmed cell. Also, we propose a sensing margin test circuit with a variable pull-up load out of consideration for resistance variations of programmed eFuse. Peak current through a non-programmed eFuse is reduced from 728 µA to 61µA when a simulation is done in the read mode. Also, there is no problem in data sensing by using a variable pull-up load of BL S/A out of consideration for resistance variations of programmed eFuse even if the sensed resistance is at least 9 kΩ lower than the sensible resistance of programmed eFuse designed with a target value of 16 kΩ in the normal read mode although it is 25 kΩ during the wafer read test. Test chips for the 1-kb OTP memory IP designed with Dongbu HiTek's 0.18 µm BCD process is in the making.

II. CIRCUIT DESIGN

Table 1 shows bias voltage conditions at various nodes for various operation modes of an eFuse OTP cell.

Table 1. Each node bias voltage of an eFuse OTP memory cell at each operation mode

	Program Mode		Read Mode	
WWL	VIO		0	
RWL	0		VDD	
DIN	0	1	×	×
SL	0	VIO	0	0
BL	Floating	Floating	0	VDD
DOUT	×	×	0	1
eFuse	Unblown	Blown	Unblown	Blown

Selected WWL (Write word-line) in the program mode is activated to VIO in the program mode. The eFuse link of the OTP memory cell is separated from BL since non-selected WWLs are kept to 0 V in the program mode. If we apply VDD to DIN and a pulse to PGM, SL (Source-line) and WWL are applied with VIO. This then allows the programming current to flow through the eFuse and MN1. Therefore, the eFuse is programmed and is in the highly resistive state. Also, the resistance of the eFuse is invariant for the non-programmed cell since DIN is applied with 0 V and SL is kept to 0 V. In contrast, only one RWL decoded by RA[6:0] is activated to VDD after BL is precharged to 0 V in the read mode. In case of a non-programmed eFuse cell, a current path is made between the MN2 and the eFuse link, BL is kept to 0 V and DOUT outputs a logic value of '0'. In contrast, a programmed eFuse cell has a highly resistive state and DOUT outputs a logic value of '1' since BL is pulled up to VDD by the pull-up load transistor.

As a chip measurement result, the selected RWL is activated from 0 V to VDD and VDD voltage, the precharging voltage of BL, becomes discharged to 0 V through the read NMOS transistor with the channel width of 5 µm and the eFuse link in reading out a non-programmed eFuse cell. Then, peak current through the eFuse is 728 µA as shown in Fig. 3. Also, the eFuse link can be blown by the EM phenomenon if large-density current flow the eFuse link of narrow width like the SEM image of a failed eFuse by EM as in Fig. 2.

In this paper, we propose a method of precharging BL to VSS before activation of RWL and an optimized design of read NMOS transistor to reduce read current through a non-programmed cell. Major specifications of the designed 1-kb eFuse OTP memory are in the following. The cell array of 1 kilo bits is arranged in 128

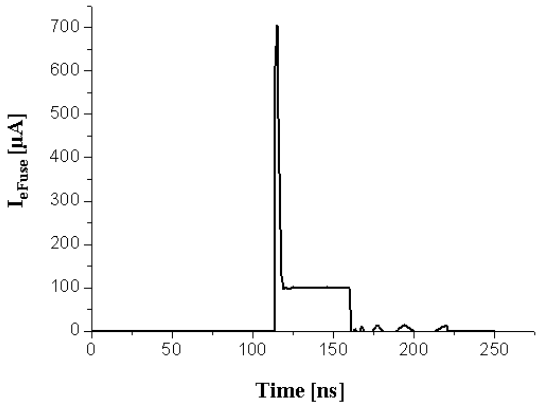

Fig. 3. Current waveform through an eFuse in the read mode after simulation.

rows × 8 columns. The two supply voltages that are used are: logic supply voltage VDD (=1.8 V) and I/O interface voltage VIO (=5 V). There are three operation modes: program, read, and stand-by modes. This OTP is programmed bitwise and read out byte by byte. The program voltage and program time are 5 V and 200 μs, respectively.

As shown in Fig. 4, the designed 1-kb eFuse OTP memory consists of an eFuse OTP memory cell array of 128 rows × 8 columns, a row decoder selecting one of 128 WLs by decoding the row address bus RA[6:0], a SL driver, a DOUT (Data output) buffer, and a control logic that supplies internal control signals which are suitable for either the program or read mode. This is based according to the control signals (RD and PGM). The SL driver consists of eight driving circuits and drives one selected SL by decoding the column address CA[2:0]. The BL S/A outputs a digital datum through DOUT[7:0] by sensing a datum coming from BL[7:0]. The bits vary in accordance to their programmed states.

Fig. 5 shows an eFuse OTP cell array of 128 rows × 8 columns. The cell array is divided into two sub-arrays of 64 rows × 8 columns. One of the sub-arrays is selected by a row address RA6.

Fig. 6(a) shows the conventional BL S/A circuit using the BL VDD precharging scheme. In the read mode, BL precharges to VDD since MP0 turns on by a short pulse of PRECHARGE signal before RWL is activated. If the RWL is activated, BL connected to a programmed cell with a logic value of '1' keeps VDD since the eFuse cell is in the highly resistive state while the BL is discharged to 0V through the read NMOS transistor and the eFuse link for the programmed cell with a logic value of '0'. Then the eFuse can be blown by the big discharging current when the BL is discharged to 0 V. Thus, we precharges the BL to VSS before activation of the RWL like a S/A of the BL VSS precharging scheme as shown in Fig. 6(b) in this paper. The BL is, therefore, pulled up to VDD in case that a programmed eFuse cell is accessed while it keeps a precharging level of VSS in case that a non-programmed eFuse cell is accessed. By precharging of the BL to BSS before activation of the RWL like this and reducing the width of read NMOS transistor for the eFuse cell from 5 μm to 1.0 μm, we can reduce the peak current through the eFuse in the read mode. Also, if SAENb (Sense amplifier enable) is activated to 0 V after a datum of the eFuse OTP cell is transferred to the BL sufficiently, a negative-level sensitive D latch senses

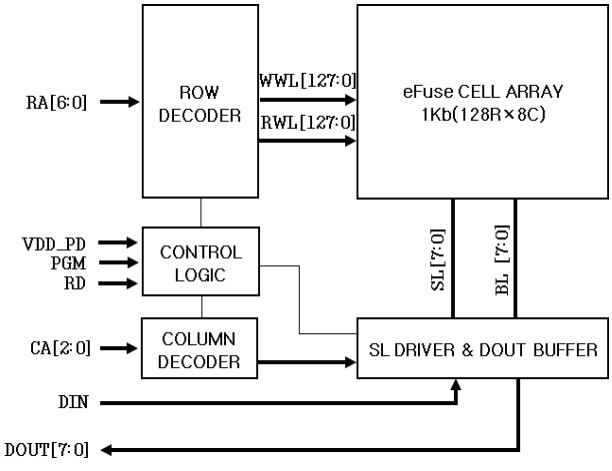

Fig. 4. Block diagram of 1-kb eFuse OTP memory IP.

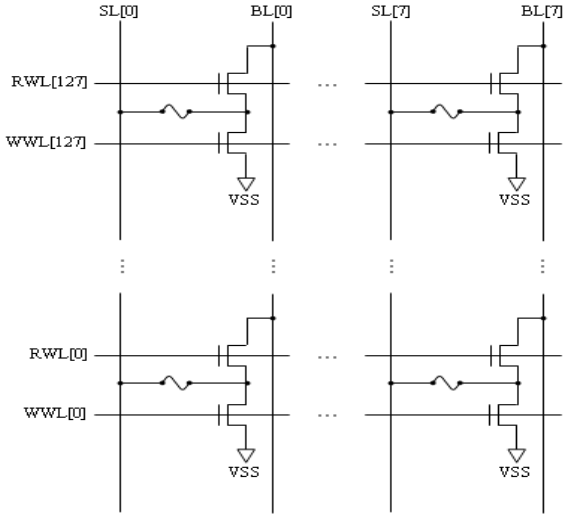

Fig. 5. eFuse OTP memory cell array of 128 rows × 8 columns.

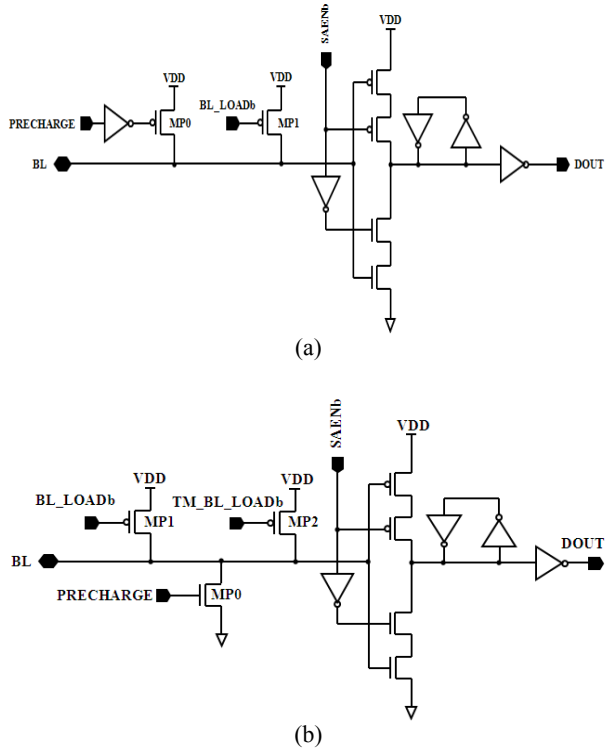

Fig. 6. BL S/A circuits. (a) BL VDD precharging scheme and (b) BL VSS precharging scheme.

either VDD or 0 V and outputs the read datum to DOUT.

The resistance of programmed eFuse can vary below the minimum resistance that can be sensed by the BL S/A in Fig. 6(a) during use in the field when the eFuse link is programmed with its resistance around the minimum resistance. Then, a data sensing failure can happen. Thus, we propose a sensing margin test circuit with a variable pull-up load as shown in Fig. 6(b) out of consideration for resistance variations of programmed eFuse in this paper. A pull-up transistor MP2 for the test read mode is added to a pull-up load transistor MP1 for the normal read mode in Fig. 6(a). As Fig. 6(a) is not a variable pull-up loading scheme, TM_BL_LOADb signal is not required. After an eFuse is programmed, we test if the eFuse is programmed normally by turning on MP2 in Fig. 6(b). In the normal read mode used in the field, BL can sense a normal datum of '1' although the resistance of eFuse varies lower since the pull-up resistance is raised by making only MP1 in Fig. 6(b) turned on. On the contrary, there is no problem if the pull-up resistance varies higher. This means increasing the sensing margin. Thus, we take only the case the resistance of programmed eFuse goes lower under consideration.

III. Simulation Results

We designed a 1-kb eFuse OTP memory IP with Dongbu HiTek's 0.18 μm BCD process. Fig. 7 shows simulation results of BL voltages in the conventional and proposed BL precharging scheme in the read mode under the following conditions: VDD=1.8 V, VIO=5 V, Temperature=25 ˚C, and TT model parameters. We can see that BL signals are precharged to VDD and VSS by the PRECHARGE signal in Figs. 7(a) and 7(b), respectively. In Fig. 7(b), the BL signal is pulled up by the BL_LOADb signal. In addition, Fig. 8 shows the pulled-up BL voltage waveform by the TM_BL_LOADb signal in the test read mode for the BL S/A with a variable pull-up load.

Fig. 9 shows a simulation result for read current of a non-programmed cell. The peak current is reduced form 728 μA to 61 μA through the proposed BL VSS precharging scheme and downsizing of the read NMOS transistor. In Table 2, we compare peak currents through a non-programmed eFuse in the read mode with respect to VDD voltages, temperatures, and model parameters of

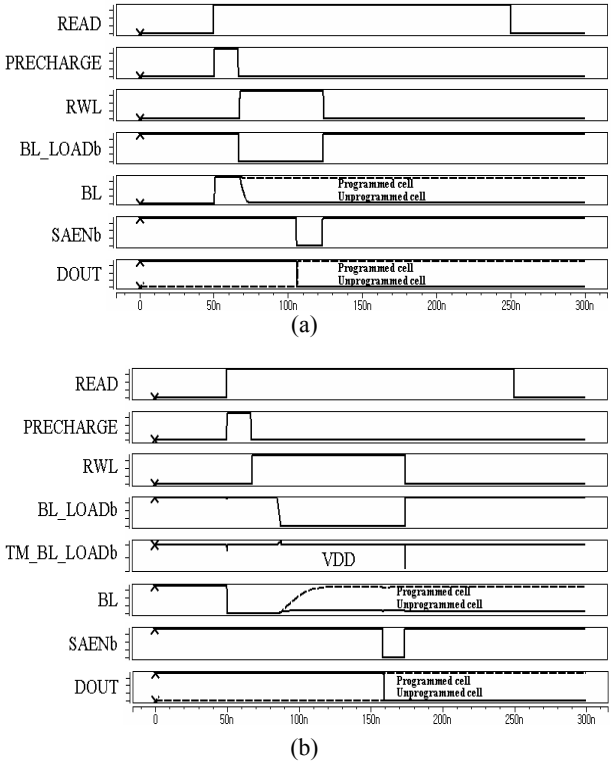

Fig. 7. Simulation results of BL voltages in correspondence of the BL precharging schemes in the read mode. (a) Conventional scheme and (b) Proposed scheme.

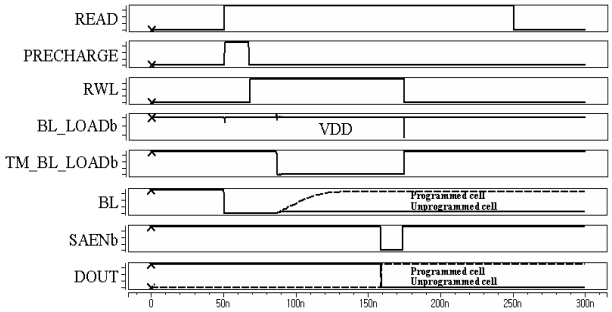

Fig. 8. Simulation result in the test read mode for the BL S/A with a proposed variable pull-up load.

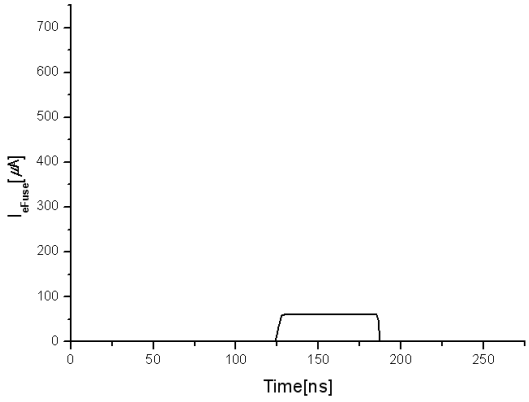

Fig. 9. Simulation result of read current of a non-programmed cell in the designed 1-kb eFuse OTP memory IP.

Table 2. Comparison of peak currents through a non-programmed eFuse in the read mode with respect to VDD voltages, temperatures, and model parameters of MOS transistors between the conventional IP and the proposed IP

IP	VDD	Temp.	SS[μA]	SF[μA]	TT[μA]	FS[μA]	FF[μA]
Conventional IP	1.62 V	-40 ˚C	271	312	368	423	486
		25 ˚C	248	286	337	384	447
		125 ˚C	219	258	299	336	401
	1.8 V	-40 ˚C	363	419	476	536	607
		25 ˚C	331	381	430	485	558
		125 ˚C	279	334	374	417	491
	1.98 V	-40 ˚C	468	526	582	647	728
		25 ˚C	343	476	529	580	665
		125 ˚C	351	411	454	500	587
Proposed IP	1.62 V	-40 ˚C	17.4	30.4	24.5	19.8	34.4
		25 ˚C	16.2	27.3	22.4	15	30.9
		125 ˚C	15.3	24.7	21.9	19.6	27.6
	1.8 V	-40 ˚C	26	41.8	35.5	29.4	47.1
		25 ˚C	23.2	36.8	31.3	25.9	41
		125 ˚C	21.2	32.3	27.8	25.8	38.1
	1.98 V	-40 ˚C	36.5	54.8	47.6	35.6	61
		25 ˚C	32.1	47.5	41.5	33.6	53.5

MOS transistors between the conventional IP and the proposed IP. The peak currents are 728 μA for the conventional IP and 61 μA in the proposed counterpart.

With the S/A circuit using the variable pull-up load in Fig. 6(b), the respective resistances which can be sensed in the test read and normal read mode are 25 kΩ and 16 kΩ when a simulation is done. In this case, normal sensing is possible even in the field unless the resistance of eFuse falls below 16 kΩ.

Fig. 10 shows a simulation result of BL readout times with respect to OTP memory densities baed on the proposed scheme. We can see that the readout time

Table 3. Simulation result of eFuse sensing resistances in the normal and test read mode

Operation Mode	VDD	Temp.	SS	SF	TT	FS	FF
Normal Read Mode	1.62 V	-40 ˚C	22 kΩ	11 kΩ	17 kΩ	25 kΩ	13 kΩ
		25 ˚C	24 kΩ	12 kΩ	19 kΩ	27 kΩ	15 kΩ
		125 ˚C	26 kΩ	15 kΩ	21 kΩ	28 kΩ	17 kΩ
	1.8 V	-40 ˚C	17 kΩ	9 kΩ	14 kΩ	19 kΩ	11 kΩ
		25 ˚C	20 kΩ	11 kΩ	16 kΩ	21 kΩ	13 kΩ
		125 ˚C	22 kΩ	14 kΩ	18 kΩ	23 kΩ	15 kΩ
	1.98 V	-40 ˚C	14 kΩ	9 kΩ	12 kΩ	15 kΩ	10 kΩ
		25 ˚C	17 kΩ	11 kΩ	14 kΩ	17 kΩ	11 kΩ
		125 ˚C	19 kΩ	13 kΩ	16 kΩ	19 kΩ	14 kΩ
Test Read Mode	1.62 V	-40 ˚C	35 kΩ	17 kΩ	27 kΩ	38 kΩ	21 kΩ
		25 ˚C	41 kΩ	21 kΩ	30 kΩ	41 kΩ	24 kΩ
		125 ˚C	47 kΩ	26 kΩ	35 kΩ	44 kΩ	27 kΩ
	1.8 V	-40 ˚C	27 kΩ	16 kΩ	22 kΩ	29 kΩ	17 kΩ
		25 ˚C	32 kΩ	19 kΩ	25 kΩ	31 kΩ	20 kΩ
		125 ˚C	37 kΩ	24 kΩ	29 kΩ	36 kΩ	24 kΩ
	1.98 V	-40 ˚C	23 kΩ	14 kΩ	19 kΩ	23 kΩ	15 kΩ
		25 ˚C	27 kΩ	17 kΩ	22 kΩ	26 kΩ	18 kΩ
		125 ˚C	31 kΩ	22 kΩ	26 kΩ	30 kΩ	22 kΩ

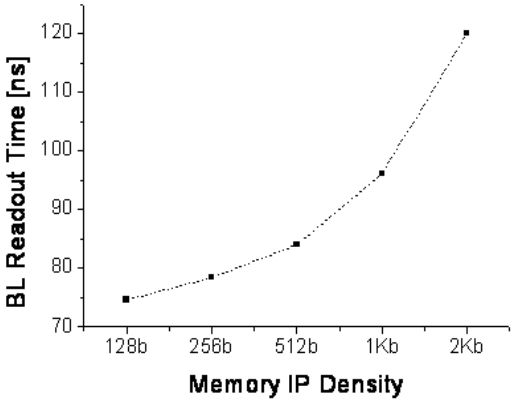

Fig. 10. Simulation result of BL readout times with respect to memory densities.

increases as the memory density does. This does not affect the speed of OTP memory.

Fig. 11 shows the layout image of the designed 1-kb eFuse OTP memory IP with the 0.18μm BCD process. The layout size is 283.565 μm × 524.180 μm.

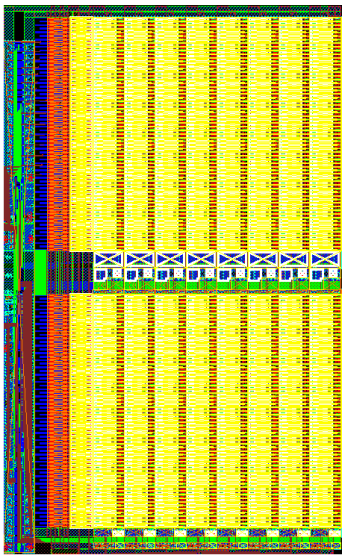

Fig. 11. Layout picture of the designed eFuse OTP IP with the 0.18 μm BCD process.

IV. CONCLUSIONS

It is required to design eFuse-type OTP memory IPs in consideration of sufficient reliability such as EM and data retention characteristics in PMICs.

In this paper, we proposed a method of precharging BL to VSS before activation of RWL and an optimized design of read NMOS transistor to reduce read current through a non-programmed cell. Also, we proposed a sensing margin test circuit with a variable pull-up load out of consideration for resistance variations of programmed eFuse.

Peak current through the non-programmed eFuse was reduced from 728 μA to 61 μA when a simulation was done in the read mode. Also, there was no problem in data sensing by using a variable pull-up load of BL S/A out of consideration for resistance variations of the programmed eFuse even if the sensed resistance was at least 9 kΩ lower than the sensible resistance of programmed eFuse designed with a target value of 16 kΩ in the normal read mode although it was 25 kΩ during the wafer read test.

ACKNOWLEDGMENTS

This work was sponsored by ETRI System Semiconductor Industry Promotion Center, Human Resource Development Project for SoC Convergence.

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