A Low Noise and Low Power RF Front-End for 5.8-GHz DSRC Receiver in 0.13 μm CMOS

Jaeyi Choi*, Shin-Hyouk Seo*, Hyunwon Moon, and Ilku Nam***

Abstract—**A low noise and low power RF front-end for 5.8 GHz DSRC (Dedicated Short Range Communication) receiver is presented. The RF front-end is composed of a single-to-differential two-stage LNA and a Gilbert down-conversion mixer. In order to remove an external balun and 5.8 GHz LC load tuning circuit, a single-to-differential LNA with capacitive cross coupled pair is proposed. The RF front-end is fabricated in a 0.13 μm CMOS process and draws 7.3 mA from a 1.2 V supply voltage. It shows a voltage gain of 40 dB and a noise figure (NF) lower than 4.5 dB over the entire DSRC band.**

Index Terms—**CMOS, DSRC, low noise, low power, RF front-end**

I. INTRODUCTION

The dedicated short range communication (DSRC) system provides a communication between on board unit (OBU) and road side equipment (RSE) within a short range communication area. The electronic toll collection system (ETCS) is an application of DSRC system using 5.8 GHz ISM band and it provides driver's convenience by eliminating traffic congestion. Korea and Japan currently adopt the 5.8 GHz DSRC system using amplitude shift keying (ASK) modulation.

There are previously published literatures for the 5.8 GHz DSRC transceiver [1-7]. Most of them composed of hybrid modules, which are implemented in SiGe-BiCMOS process, are not compatible with CMOS digital modems [2-6]. Moreover, they used numerous external components, resulting in an increased cost and chip size.

Recently, the trend of DSRC receiver design is to reduce chip size, cost, and power consumption, and to increase system feature and integration. Therefore, a low power low cost CMOS DSRC transceiver that can be integrated with a digital modem is necessary for this system.

In this work, a CMOS RF front-end for the DSRC receiver is presented. The RF front-end is composed of a single-to-differential two-stage low noise amplifier (LNA) and a Gilbert down-conversion mixer. The DSRC RF front-end is implemented in a 0.13 μm CMOS process. Section II describes the proposed balanced single-to-differential balun-LNA. The RF front-end circuits for DSRC receiver are described in Section III. Section IV presents the measurement results. Finally, Section V concludes this paper.

II. PROPOSED BALANCED SINGLE-TO-DIFFERENTIAL BALUN-LNA

Typically, a differential LNA is preferred in RF SoC (system on a chip) but this needs passive baluns to convert single-ended signal to differential signal. Passive baluns are too bulky to be integrated on a chip [8]. Therefore, it is desirable to use a single-ended input differential output LNA with high gain and low NF.

Fig. 1(a) shows the conventional single-ended input differential output LNA. It adopts the common source (CS) amplifier with common gate common source (CGCS) balun as the single-to-differential converter.

The small signal equivalent circuit of Fig. 1(a) is

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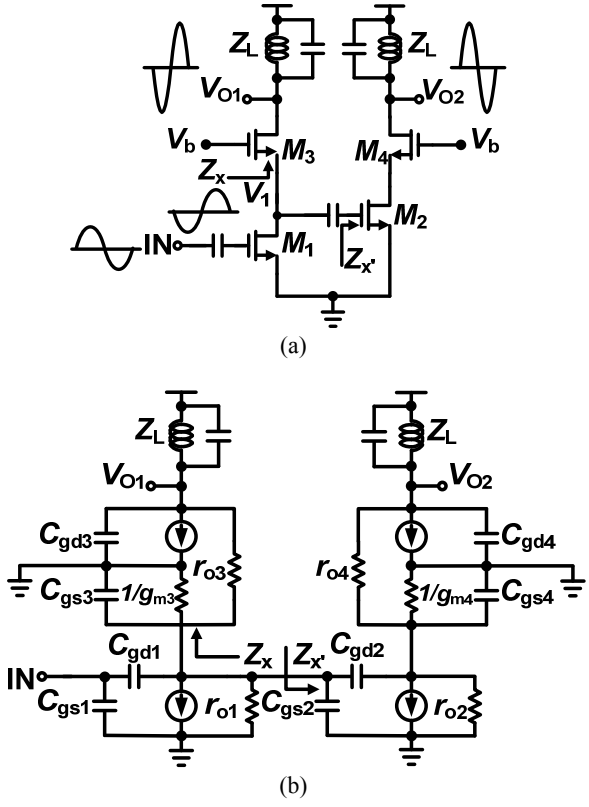


Fig. 1. (a) Conventional single-to-differential balun-LNA, (b) Its equivalent circuit.

illustrated in the Fig. 1(b). The ac output voltage signal of Fig. 1(b) can be represented as follows:

$$V_{O1} = \frac{(1+g_{m3}r_{o3})Z_L}{(1+sC_{gd3}r_{o3})Z_L + r_{o3}} V_1 \tag{1}$$

$$\text{and} \quad V_{O2} = -\frac{(g_{m2} - sC_{gd2})r_{o2}r_{o4}}{\dfrac{(1+sC_{gd4}r_{o4})Z_L + r_{o4}}{(1+g_{m4}r_{o4})Z_L} A - r_{o2}} V_1 \tag{2}$$

$$\text{where} \quad V_1 = -\frac{(g_{m1} - sC_{gd1})(r_{01} \| Z_x \| Z_{x'})}{sC_{gd1}(r_{01} \| Z_x \| Z_{x'}) + 1} V_{in} \quad \text{and}$$

$$A = \{(sC_{gd2} + sC_{gs4} + g_{m4})r_{o2}r_{o4} + r_{o2} + r_{o4}\} .$$

The impedance (Z_L) of the *LC* resonance load at the operating frequency is large. At the resonance frequency, if the size ratio of the transistors (M_1~M_4) of Fig. 1(a) is properly chosen, the balanced output signals (V_{O1} and V_{O2}) can be obtained as shown in Fig. 2(a). However, if

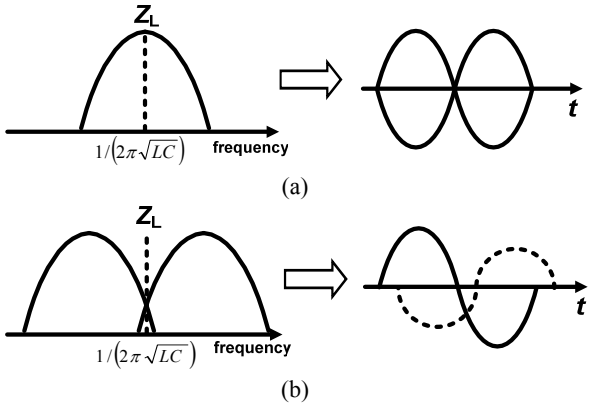


Fig. 2. Output signals of the conventional single-to-differential amplifier. (a) Balanced output signal when the LC resonance frequency is $1/(2\pi\sqrt{LC})$, (b) Unbalanced output signal when the LC resonance frequency varies.

LC load resonance frequency varies and then the impedance (Z_L) of the *LC* load is lower, the single-ended input differential output LNA has the unbalanced output signals with amplitude and/or phase mismatches. To compensate the unbalanced output signals, an *LC* calibrator can be adopted. The *LC* calibrator compares the resonance frequency of the *LC* load in Fig. 1(a) with the reference frequency from a frequency synthesizer, generates the up and down signal through a frequency comparator, and adjusts capacitance of the *LC* load to set the *LC* resonance frequency within the allowable frequency difference between the resonance frequency of the *LC* load and the reference frequency. However, the *LC* calibrator has the drawbacks of complex circuits and increased silicon area.

Therefore, the simple capacitive cross-coupled balancing technique is proposed [9]. The single-to-differential converter with capacitive cross-coupled pair is shown in Fig. 3. If V_{1+} and V_{1-} in Fig. 3 are unbalanced signals, V_{1+} and V_{1-} can be expressed as follows:

$$V_{1+} = \sin(2\pi ft) \tag{3}$$

$$V_{1-} = (1+\Delta_{err})\sin(2\pi ft + \pi + \phi_{err}) \tag{4}$$

where Δ_{err} represent the amplitude error and ϕ_{err} represent phase error, respectively. Without the capacitive cross-coupled network, V_{out+} and V_{out-} are unbalanced signals.

V_{out+} and V_{out-} in Fig. 3 can be expressed as

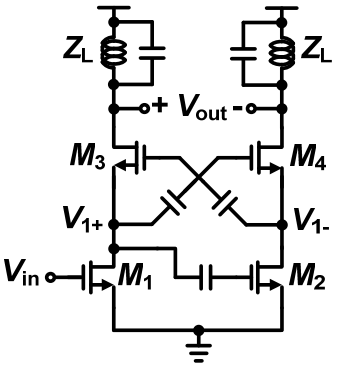


Fig. 3. Proposed single-to-differential balun-LNA with capacitive cross-coupled pair.

$$V_{out+} \approx g_m \sin(2\pi ft) + g_m(1+\Delta_{err})\sin(2\pi f + \phi_{err}) \quad (5)$$

$$V_{out-} \approx -g_m \sin(2\pi ft) - g_m(1+\Delta_{err})\sin(2\pi f + \phi_{err}) \quad (6)$$

respectively.

From Eq. (5) and Eq. (6), the simple capacitive cross-coupled network can compensate the amplitude and phase mismatch.

Fig. 4 shows the simulated gain and phase mismatch versus the load capacitance variation of the conventional single-to-differential balun-LNA of Fig. 1(a) and the proposed single-to-differential balun-LNA of Fig. 3. Because the variation of the impedance (Z_L) of the *LC* load is greatly influenced by the load capacitance variation including the parasitic capacitance, the load capacitance variation is considered in the simulation. As expected from Eq. (5) and Eq. (6), the simple capacitive cross-coupled network improves the balancing characteristics

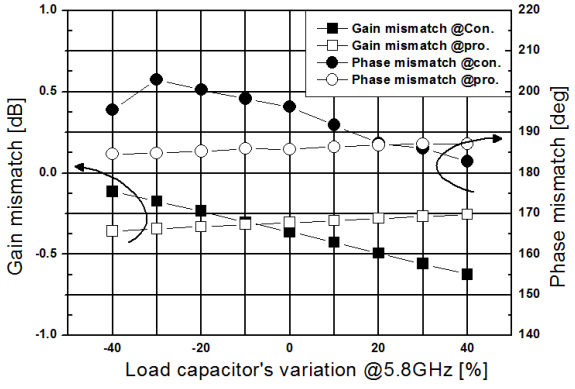


Fig. 4. Gain/phase mismatch versus load capacitance variation of the conventional single-to-differential balun-LNA and proposed single-to-differential balun-LNA.

regardless of the impedance variation of the *LC* resonance load.

In addition, the capacitive cross-coupled pair can reduce the noise contribution of the cascode transistor M_3 and M_4 by g_m boosting effect.

III. RF FRONT-END CIRCUITS FOR DSRC

Fig. 5 shows the simplified schematic of two-stage LNA for the DSRC receiver. To obtain low NF and high gain, the LNA consists of the proposed single-to-differential converter and a differential capacitive cross-coupled cascode amplifier. Because the *LC* tuning is required for high gain, the switched capacitor array is used for variable capacitance. The LNA includes the variable gain function. By changing the value of the load resistors R_1 and R_2, the LNA covers 18 dB gain range with a 6 dB gain step.

The simplified schematic of the designed down-conversion mixer is shown in Fig. 6. The Gilbert mixer is used as a down-conversion mixer. Differential LO signal is provided from the LO generation block such as VCO, divider, and LO buffer circuit [10]. IF frequency of 10 MHz is chosen for the DSRC receiver. A first order *RC* low pass filter, of which 3 dB bandwidth is

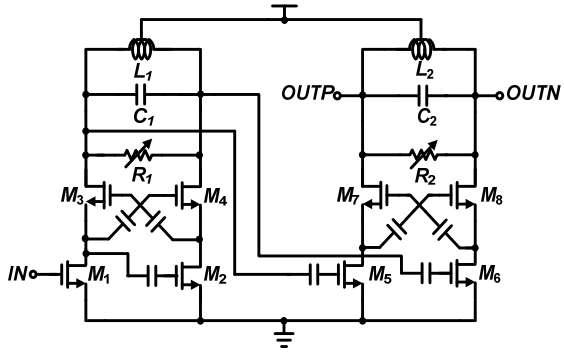


Fig. 5. Simplified schematic of the proposed two-stage LNA.

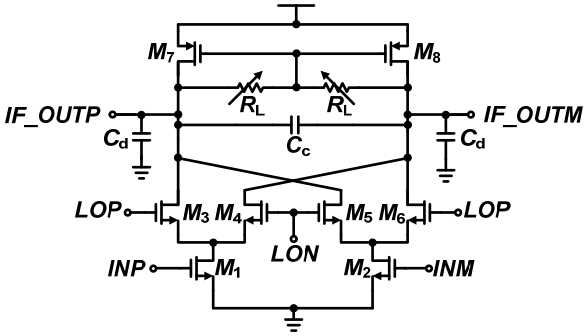


Fig. 6. Simplified schematic of the down-conversion mixer.

approximately $1/2\pi R_L(C_c+C_d)$, is implemented in the mixer's load in order to remove the spurious terms. By changing the value of the load resistor R_L, the mixer covers 12 dB gain range with a 2 dB gain step.

IV. MEASUREMENT RESULTS

The low noise and low power RF front-end for 5.8 GHz DSRC receiver is designed and fabricated in a 0.13 μm CMOS process. Fig. 7 shows the chip photograph of the proposed RF front-end. The active chip area of the RF front-end is 744 μm × 659 μm. The RF front-end draws 7.22 mA for a 1.2 V supply voltage.

Fig. 8 (a) shows the measured input matching (S11), which is lower than -10 dB in the DSRC band. Fig. 8(b) shows the measured NF. The NF is lower than 4.5 dB.

The measured performances of the RF front-end are summarized and compared with those of previously published DSRC receiver in the Table 1. In comparison with previous works, the RF front-end shows the good performances such as gain, NF and current consumption. Therefore, the RF front-end is suitable for low noise and low power RF front-end for 5.8 GHz DSRC receiver.

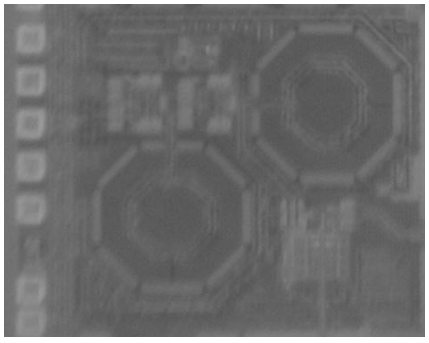
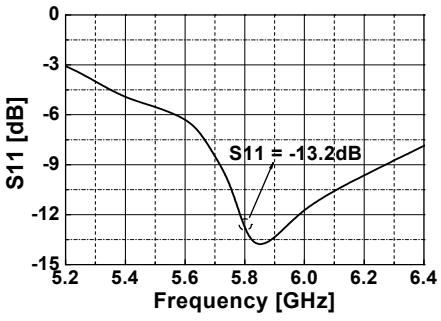
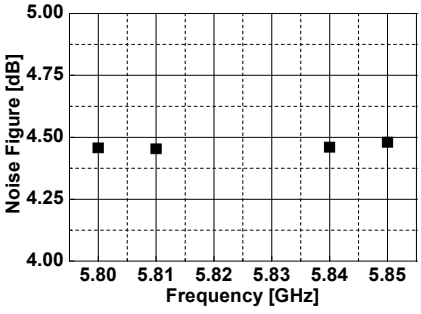


Fig. 7. Chip photograph of RF front-end.



(a)



(b)

Fig. 8. (a) Measured input matching (S11), (b) Measured NF.

V. CONCLUSIONS

A low power and low noise CMOS RF front-end suitable for 5.8 GHz DSRC receiver is proposed**.** The RF front-end is composed of a single-to-differential LNA and Gilbert down-conversion mixer. In order to remove an external balun and 5.8 GHz LC load tuning circuit, a single-to-differential LNA with capacitive cross coupled pair is proposed. It is fabricated in a 0.13 μm CMOS process and draws 7.3 mA from 1.2 V supply voltage. It shows a voltage gain of 40 dB and NF lower than 4.5 dB at the entire DSRC band. Therefore, the proposed RF front-end is suitable for low noise and low power 5.8 GHz DSRC receiver ICs.

Table 1. Performance summary and comparison with previous works

	[2]	[3]	[4]	[5]	[7]	This work
S11 [dB]	-	-19	-	-	-	< -10
Max gain [dB]	31	-	29.1	-	48	40
NF [dB]	8	-	6.1	7.9	< 5	4.5
P1dB [dBm]	- 40	-	- 34.5	-	- 41	- 31.5
Current consumption [mA]	51.6 @ 3.0 V (cf. Rx)	40 @ 3.0 V (cf. Rx/Tx)	68 @ 3.3 V (cf. Rx)	71 @ 3.3 V (cf. Rx)	52 @ 1.2 V (cf. Rx)	7.3 @ 1.2 V
Technology	SiGe HBT/CMOS	SiGe-BiCMOS	0.35 μm SiGe-BiCMOS	0.25 μm SiGe-BiCMOS	0.13 μm CMOS	0.13 μm CMOS

ACKNOWLEDGMENTS

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