A 40fJ/c-s 1 V 10 bit SAR ADC with Dual Sampling Capacitive DAC Topology

Binhee Kim, Long Yan, Jerald Yoo, and Hoi-Jun Yoo

Abstract—**A 40 fJ/c-s, 1 V, 10-bit SAR ADC is presented for energy constrained wearable body sensor network application. The proposed 10-bit dual sampling capacitive DAC topology reduces switching energy by 62% compared with 10-bit conventional SAR ADC. Also, it is more robust to capacitor mismatch than the conventional architecture due to its cancelling effect of each capacitive DAC. The proposed SAR ADC is fabricated in 0.18 μm 1P6M CMOS technology and occupies 1.17 mm^2 including pads. It dissipates only 1.1 μW with 1 V supply voltage while operating at 100 kS/s.**

Index Terms—**SAR ADC, dual sampling, low energy, wearable body sensor network**

I. INTRODUCTION

Recently, a battery-less disposable healthcare sensor [1, 2] with self configured network controller enables wearable healthcare in personal daily life. Such healthcare sensor needs to harvest the power from external network controller through cm-range inductive coupling. In such circumstances, the power budget of entire sensor is extremely limited as low as 12 μW [2]. An ADC is one of the key functional blocks whose power consumption and conversion rate are essential to realize continuous healthcare.

Among many types of ADCs, the SAR (Successive Approximation Register) ADC is one of the most widely used in energy constrained application [3, 4] due to its minimum analog blocks. Even though the SAR ADC [3, 4] consumes low power (about 25 μW), it is still beyond the power budget of the battery-less disposable healthcare sensor [1, 2].

For these reasons, a lot of previous works focused on reducing energy of the SAR ADC [6, 7]. The SAR ADC consists of digital logics to generate control signal, a capacitive DAC (digital-to-analog converter) for successive charge distribution to evaluate the sampled signal, and a comparator. Since the switching power of a capacitive DAC is dominant portion in the SAR ADC's power consumption, a lot of works focusing on saving the switching energy of the capacitive DAC have been reported [6, 7]. Previous works such as proposed in [6] reduce switching energy by eliminating unnecessary switching operation with splitting capacitors in the capacitive DAC. These methods can save 37% of the switching energy compared to the conventional ones [5].

However, since the requirement of low power is much stringent, this work proposes a new architecture for the capacitive DAC of SAR ADC. It was proved that it would be able to save 62% of the switching energy compared to the conventional switching scheme [5] and 40% even compared to the previous work [6] in 10-bit resolution. It eliminates MSB calculation switching energy as well as unnecessary switching operation by sampling input voltage at both nodes of the comparator. It is called dual sampling method in this paper.

This paper proposes a new 10-bit ADC fabricated in a 0.18 μm CMOS. Section II explains the operation of the proposed SAR architecture, compared with that of the conventional ones. Various analyses about switching power are explained in section III. The effects of capacitor

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mismatch in the proposed architecture are investigated in section IV. Implementation results are presented in section V. Finally, section VI draws our conclusions.

II. THE PROPOSED SAR ARCHITECTURE

In order to compare the operations, we first review the operation of the conventional SAR ADC shown in Fig. 1. The SAR ADC is composed of a binary capacitive DAC, a comparator, and SAR control logics. The total capacitance of a binary capacitive DAC is 2^nC where C is a unit capacitance. These capacitors are connected to one side of a comparator in parallel. In sample mode, the DAC samples V_{ref}-V_{in}, and the entire bottom plates of capacitive DAC are connected to the ground in hold mode. The bottom plates of capacitors are connected to the reference voltage or ground in calculation phase.

The proposed architecture splits a capacitive DAC into two and samples input voltage at both DAC as shown in Fig. 2. Total capacitance of a capacitive DAC is the same as conventional one with 2^nC, but each capacitive DAC of $2^{n-1}C$ capacitance is connected to respective input side of a comparator separately. The proposed architecture is single-ended, not differential. In other words, input

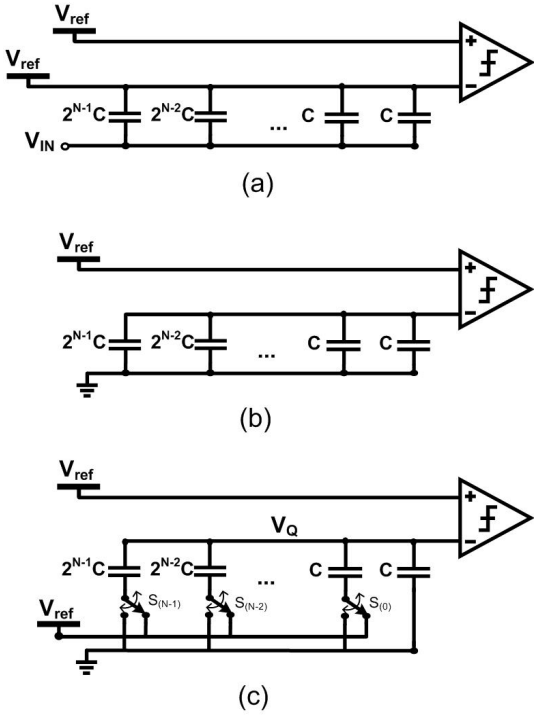


Fig. 1. Conventional SAR ADC Architecture and Operation. (a) Sample, (b) Hold and (c) Calculation.

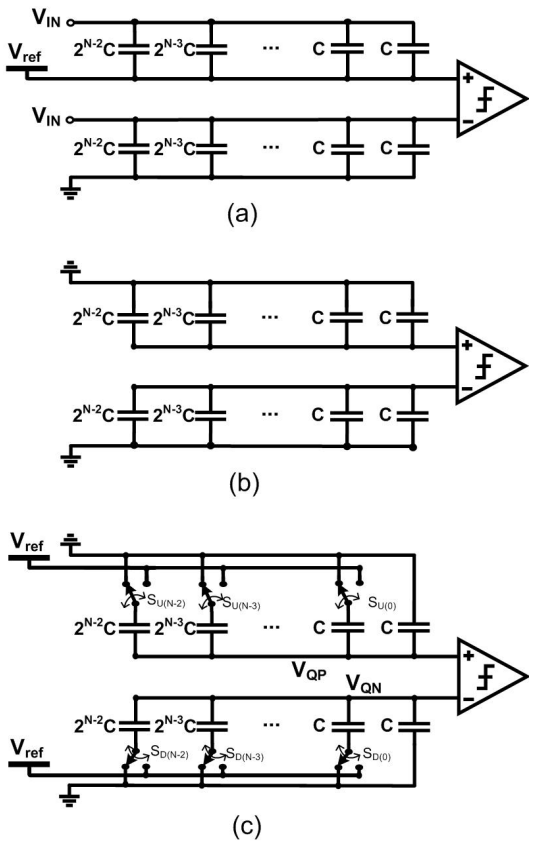


Fig. 2. The proposed SAR ADC Architecture and Operation. (a) Sample, (b) Hold and (c) Calculation.

voltage nodes are same at upper capacitive DAC and lower capacitive DAC. The operation of the proposed SAR ADC is as follows. First of all, the upper side capacitive DAC samples V_{ref}-V_{in}, while the bottom side capacitive DAC samples V_{in}. In hold mode (after sample mode), the entire bottom plates of capacitive DAC are connected to the ground. Simultaneously, MSB can be calculated in hold mode. In this way, this dual sampling method induces MSB calculation with no switching energy consumptions. Because almost the half of the total switching energy is consumed at the MSB calculation phase in the conventional architecture, the proposed sampling method has the possibility of reducing total switching energy.

The rest of the bits are calculated as follows. The timing diagram of 4-bit SAR ADC operation when output code is 1000 is shown as an example in Fig. 3. Each switch name is shown in Fig. 1(c) and Fig. 2(c). In the case of the conventional SAR ADC, S_3 is connected to the reference voltage to decide MSB in the first cycle. Depending on MSB, connections of S_3 and S_2 is decided

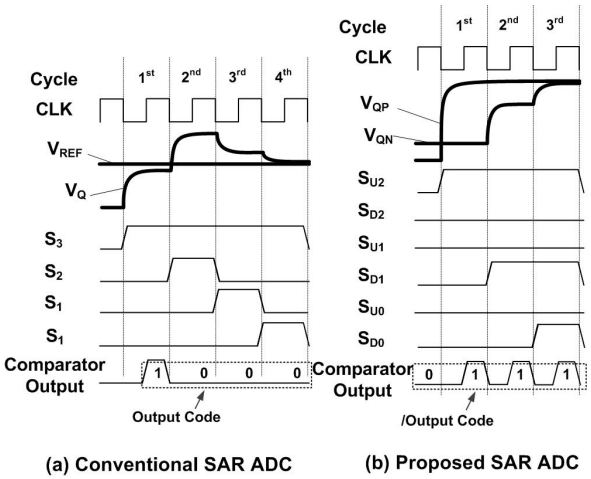


Fig. 3. Timing Diagram of operation of Conventional SAR ADC and the proposed Dual Sampling SAR ADC in calculation phase.

in the second cycle. In the same manner, connections of S_2 and S_1 are decided depending on the second bit in the third cycle.

In the case of the proposed SAR ADC, the MSB is decided in hold mode. Depending on the MSB, connections of S_{U2} and S_{D2} are decided in the first cycle. S_{UX} and S_{DX} do the opposite operation. In the second cycle, connections of S_{U1} and S_{D1} are decided depending on the second bit. Then completion of calculation of 4-bit ADC is done at the third cycle in the proposed architecture, while done at the fourth cycle in the conventional architecture.

Fig. 4 shows the circuit diagram of a comparator. A dynamic comparator is used for low power compensation. PMOS and NMOS connected to CLK# signal block continuous current flow. A comparator is activated at the edge of CLK# signal. By the complementary operation of sw(switch) signal and CLK# signal, the comparator output signal is transmitted to a latch.

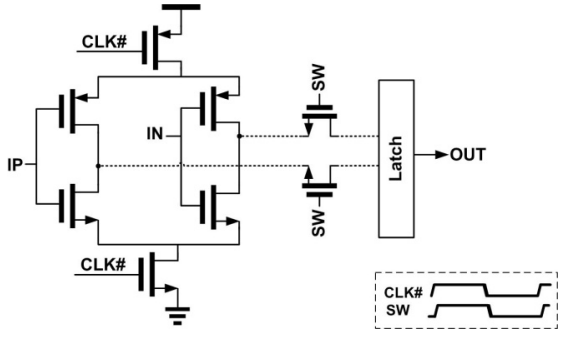


Fig. 4. Circuit Diagram of Comparator.

III. SWITCHING ENERGY ANALYSIS

The SAR ADC consists of digital logics, a capacitive DAC, and a comparator as referred in section II. This section is focused on switching energy analysis of the proposed Dual Sampling SAR ADC compared with the conventional SAR ADC.

Using the method of switching energy calculation in reference [7], the energy consumptions for each bit generation in three kinds of SAR ADC's architecture have been derived in Fig. 5. The split cap architecture in [6] also compared with the proposed architecture. The split cap architecture looks similar to the proposed one from a view point that the DAC in conventional one [5] is split into two blocks as shown in Fig. 5. However, while the entire capacitors in the split cap method are connected to the one input node of the comparator, split DACs in the proposed are connected to both input nodes of the comparator.

In Fig. 5, 3-bit SAR ADC is presented as an example. In the MSB calculation phase of the conventional architecture and the split cap architecture, the half of the total capacitor has to be connected to the reference voltage. MSB calculation power has great portion of weight on the total power consumption, especially in the split cap architecture.

If switching energy of each bit except MSB phase is compared, proposed one consumes more power. Hence, switching energy of each bit is

$$\begin{aligned} E_{n->n+1} &= -V_{REF}\,(Q_{n+1} - Q_n) \\ &= -V_{REF}\,(C_1(V_{n+1} - V_n) + C_2((V_{n+1} - V_{REF}) - V_n)) \end{aligned} \quad (1)$$

where C_1 represents the capacitance connected to the reference voltage in nth phase and *(n+1)*th phase simultaneously, C_2 represents the capacitance newly connected to the reference voltage in *(n+1)*th phase, V_n represent voltage at node connected to the comparator in nth phase, and V_{n+1} represent voltage at node connected to the comparator in *(n+1)*th phase. As lower bit is calculated, $V_{n+1} - V_n$ and C_2 are getting lower. Therefore, as lower bit is calculated, much less power is consumed. With this result, even though switching energy of each bit is consumed more in the proposed architecture than in

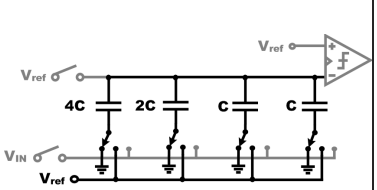
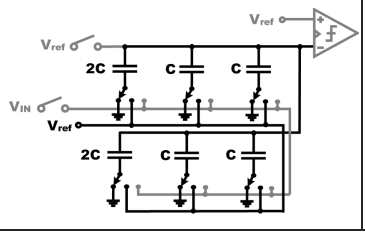
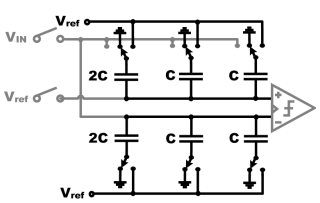
Architecture	Conventional Architecture[5]			Split Cap Architecture[6]			The proposed Architecture		
									
Vin	Each Bit Calculation Energy								
	MSB	2nd	3rd	MSB	2nd	3rd	MSB	2nd	3rd
1/8 V_{ref}	$2CV_{ref}^2$	$\frac{5}{2}CV_{ref}^2$	$\frac{9}{8}CV_{ref}^2$	$2CV_{ref}^2$	$\frac{1}{2}CV_{ref}^2$	$\frac{1}{8}CV_{ref}^2$	0	CV_{ref}^2	$\frac{1}{4}CV_{ref}^2$
3/8 V_{ref}	$2CV_{ref}^2$	$\frac{5}{2}CV_{ref}^2$	$\frac{5}{8}CV_{ref}^2$	$2CV_{ref}^2$	$\frac{1}{2}CV_{ref}^2$	$\frac{5}{8}CV_{ref}^2$	0	CV_{ref}^2	$\frac{3}{4}CV_{ref}^2$
5/8 V_{ref}	$2CV_{ref}^2$	$\frac{1}{2}CV_{ref}^2$	$\frac{13}{8}CV_{ref}^2$	$2CV_{ref}^2$	$\frac{1}{2}CV_{ref}^2$	$\frac{1}{4}CV_{ref}^2$	0	CV_{ref}^2	$\frac{3}{4}CV_{ref}^2$
7/8 V_{ref}	$2CV_{ref}^2$	$\frac{1}{2}CV_{ref}^2$	$\frac{1}{8}CV_{ref}^2$	$2CV_{ref}^2$	$\frac{1}{2}CV_{ref}^2$	$\frac{1}{8}CV_{ref}^2$	0	CV_{ref}^2	$\frac{1}{4}CV_{ref}^2$
Normalized Average	2	$\frac{3}{2}$	$\frac{7}{8}$	2	$\frac{1}{2}$	$\frac{9}{32}$	0	1	$\frac{1}{2}$

Fig. 5. Comparisons of switching power of three architectures. Conventional [5], Split Cap [6], the proposed architectures.

the conventional and the split cap architecture, total sum of every bit calculation energy is less in the proposed one than in the conventional and the split cap one due to the eliminated MSB calculation energy.

Accumulated switching energy distribution at each bit is presented in Fig. 6. As shown in Fig. 6, switching energy of MSB calculation in the proposed architecture is 0. By this property, switching energy of conversion in the proposed architecture is almost half of that in the split cap architecture, as plotted in 10^{th} bit in Fig. 6. As a result, the proposed architecture can save 62% of switching energy compared to the conventional one in 10-bit resolution. Also it can even save 40% of switching energy compared to the split cap architecture.

Fig. 7 shows the comparison of switching energy at each code in three kinds of architectures: the conventional architecture, the split cap, and the proposed one. These models are proved with rigorous SPICE simulations. This figure shows the switching energy at each output code. As shown in Fig. 6, the proposed architecture can save 62% of switching energy compared to the conventional one and save 40% of switching energy compared to the

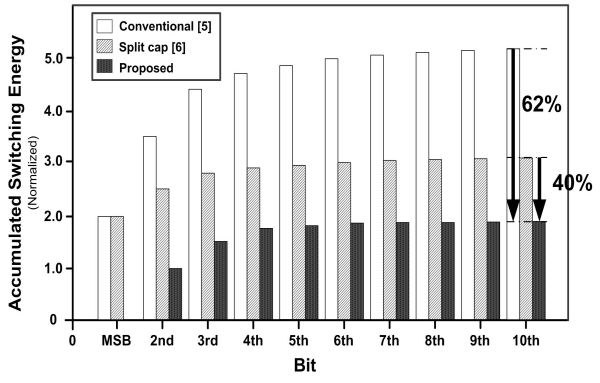


Fig. 6. Accumulated Average Switching Energy at Each Bit. Conventional architecture [5], Split cap architecture [6], the proposed architecture.

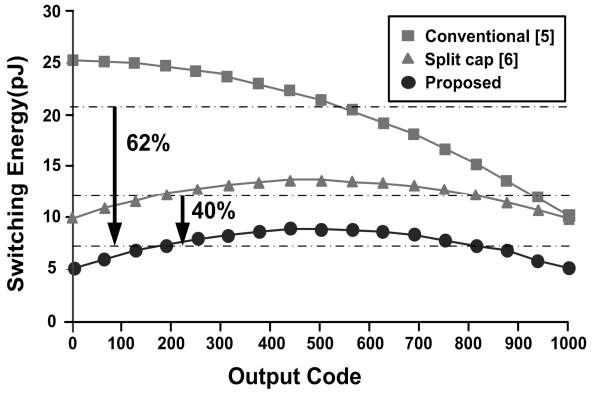


Fig. 7. Comparison of Switching Energy in 10-bit ADC Calculation Phase. Conventional architecture [5], Split cap architecture [6], the proposed architecture. Switching energy of the proposed architecture is almost half of that of split cap architecture.

split cap architecture in 10-bit resolution. Due to similarity in the switching mechanism method, the shape of energy distribution curve of the proposed one looks similar to that of the split cap architecture.

IV. CAPACITOR MISMATCH

Accuracy of SAR ADC can be affected by capacitor mismatch, which is occurred by parasitic capacitances of capacitive DAC, process variations of capacitors, etc. In this section, two factors of capacitor mismatch, parasitic capacitances of capacitive DAC and process variations of each capacitor, are analyzed in the conventional SAR ADC and the proposed Dual Sampling SAR ADC.

1. Parasitic Capacitances

SAR ADC suffers from the parasitic capacitances of the output nodes of the capacitive DAC. In the Dual Sampling SAR ADC, the output nodes of two capacitive DAC suffer from the own parasitic capacitances respectively, while the conventional and the split capacitor structures have one node with parasitic capacitances.

To compare the effect of parasitic capacitances of the Dual Sampling SAR ADC with that of the conventional and the split capacitor SAR ADC, effect to the accuracy of each ADCs by parasitic capacitance variations are analyzed. When x_{conv} indicates parasitic capacitance of the conventional SAR ADC, each bit, $D_{C(0)}, D_{C(1)},...., D_{C(n-1)}$ is decided with following equation in the conventional SAR ADC.

$$\arg\min_{D_{C(0)},D_{C(1)}..D_{C(n-1)}} \left| V_{ref} \times \left(\frac{2^{n-1}D_{C(0)} + 2^{n-2}D_{C(1)} + ... + D_{C(n-1)}}{2^n + x_{conv}}\right) - V_{in} \right| \quad (2)$$

Then error between output of conversion and input in the conventional SAR ADC can be represented as Eq (3).

$$Error_{conv} = V_{ref} \times \left(\frac{2^{n-1}D_{C(0)} + 2^{n-2}D_{C(1)} + ... + D_{C(n-1)}}{2^n}\right) - V_{in} \quad (3)$$

When x_{dual_up} indicates parasitic capacitance of upper capacitive DAC and x_{dual_down} indicates parasitic capacitance of lower capacitive DAC, each bit, $D_{D(0)}, D_{D(1)},...., D_{D(n-1)}$ is decided with following equation in the Dual Sampling SAR ADC.

$$\arg\min_{D_{D(0)},D_{D(1)}..D_{D(n-1)}} \left| V_{ref} \times \left(\frac{1}{2} + \frac{1}{2} \times \left(\frac{2^{n-1}D_{D(0)} + 2^{n-2}D_{D(1)} + ... + D_{D(n-1)}}{2^n + x_{dual\_up}} + \frac{2^{n-1}\overline{D_{D(0)}} + 2^{n-2}\overline{D_{D(1)}} + ... + \overline{D_{D(n-1)}}}{2^n + x_{dual\_down}}\right)\right) - V_{in} \right| \quad (4)$$

Then error between output of conversion and input in the Dual Sampling SAR ADC can be represented as Eq. (5).

$$Error_{dual} = V_{ref} \times \left(\frac{2^{n-1}D_{D(0)} + 2^{n-2}D_{D(1)} + ... + D_{D(n-1)}}{2^n}\right) - V_{in} \quad (5)$$

Based on these equations, SNDR versus a ratio of parasitic capacitances to total capacitance of capacitive DAC with the sinusoidal input is drawn in Fig. 8. This graph is drawn with two assumptions. First assumption is that parasitic capacitance is proportional to the total capacitance of capacitive DAC. Accordingly, parasitic capacitance of the conventional SAR ADC, x_{conv}, is same as sum of parasitic capacitances of the Dual Sampling SAR ADC, $x_{dual\_up} + x_{dual\_down}$. Second assumeption is that parasitic capacitance of upper capacitive DAC and lower capacitive DAC is same, $x_{dual\_up} = x_{dual\_down}$. With these assumptions, the graph in Fig. 8 indicates that SNDR of the Dual Sampling SAR

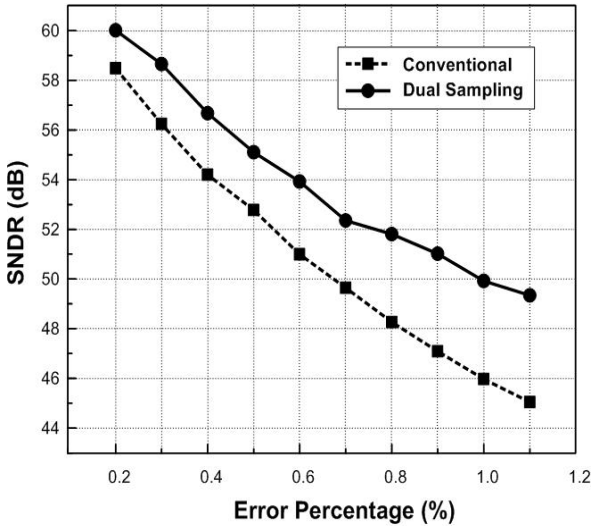


Fig. 8. SNDR versus a ratio of parasitic capacitances to total capacitance of capacitive DAC with the sinusoidal input.

ADC is higher than that of the conventional SAR ADC in all the variations of parasitic capacitance rates.

To analyze the effect of difference between parasitic capacitances of upper capacitive DAC and those of lower DAC in the Dual Sampling SAR ADC, SNDR versus ratio of parasitic capacitance of upper capacitive DAC to that of lower capacitive DAC is shown in Fig. 9. Dash line indicates the SNDR of case that ratio of parasitic capacitances to total capacitance of capacitive DAC is 0.011 in the conventional SAR ADC. Dots indicate SNDR points corresponding to the ratio of parasitic capacitances of upper capacitive DAC to that of lower capacitive DAC in the Dual Sampling SAR ADC. In this case, total parasitic capacitances of upper capacitive DAC and lower capacitive DAC is fixed as 1.1% of total capacitance of capacitive DAC to make same condition with the conventional SAR ADC. As shown in Fig. 9, even worst case rate of SNDR of the Dual Sampling SAR ADC is higher than SNDR of the conventional SAR ADC in the same condition in which total parasitic capacitance is same.

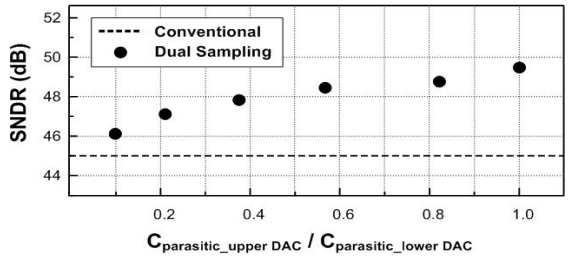


Fig. 9. SNDR versus ratio of parasitic capacitance of upper capacitive DAC to that of lower capacitive DAC.

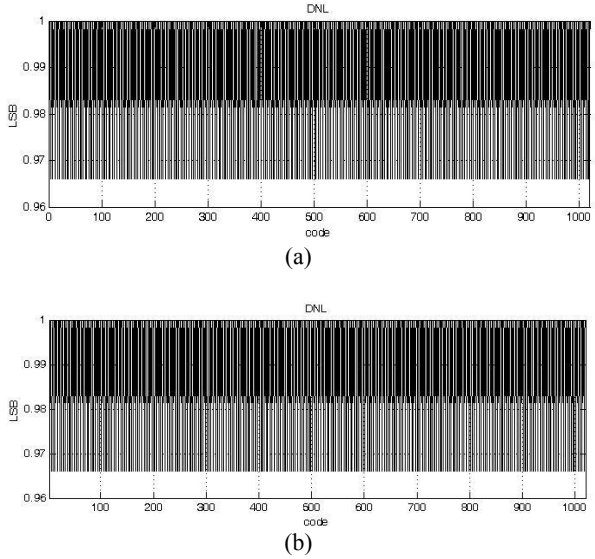


Fig. 10. DNL of case that rate of parasitic capacitances and total capacitance of capacitive DAC is 0.011. (a) Conventional SAR ADC, (b) Proposed SAR ADC.

Worse SNDR of the conventional SAR ADC with parasitic capacitances than the Dual Sampling SAR ADC with parasitic capacitances can be explained with Fig. 10 and Fig. 11. Fig. 10 indicates the DNL and Fig. 11 indicates the INL of the conventional SAR ADC and the Dual Sampling SAR ADC in the case that the rate of parasitic capacitances and total capacitance of capacitive DAC is 0.011. DNL of the conventional SAR ADC and that of the Dual Sampling SAR ADC doesn't have much difference. INL of the conventional SAR ADC is much worse than the Dual Sampling SAR ADC. INL graph shows the sine input can be truncated more at the upper part in the conventional SAR ADC than the Dual Sampling SAR ADC.

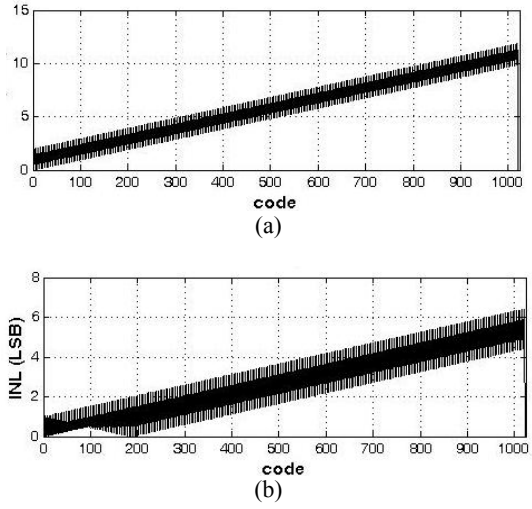


Fig. 11. INL of case that rate of parasitic capacitances and total capacitance of capacitive DAC is 0.011. (a) Conventional SAR ADC, (b) Proposed SAR ADC.

2. Process Variations of Capacitors

Capacitor mismatch by process variations largely affect to accuracy in the SAR ADC architecture. In this section, simulation results with capacitor mismatch are presented.

To see the effect of capacitor mismatch, Monte Carlo simulation is done. The values of the unit capacitors are taken to be Gaussian random variables with standard deviation of 5% (σ_0/C_0=0.05), and the ADC is otherwise ideal. Fig. 12 and Fig. 13 shows the results of 10,000 Monte Carlo runs, where the standard deviation of the INL and DNL are plotted versus output code at the 10-bit

level. Fig. 12 shows the results of the conventional SAR ADC and Fig. 13 shows the results of the Dual Sampling SAR ADC. The graph shows that linearity characteristics of the Dual Sampling SAR ADC are better than that of the conventional SAR ADC. The reason of these results can be explained with following equations. Each bit is decided as Eq. (6) in the Conventional SAR ADC, where x_{conv_tot} indicates sum of capacitor mismatch and x_{conv_n} indicates capacitor mismatch of n-th capacitor.

$$\arg\min_{D_{C(0)}\cdots D_{C(n-1)}} \left| V_{ref} \times \left(\frac{(2^{n-1} + x_{conv\_0}) D_{C(0)} + \ldots + (x_{conv\_n-1}) D_{C(n-1)}}{2^n + x_{conv\_tot}} \right) - V_{in} \right| \quad (6)$$

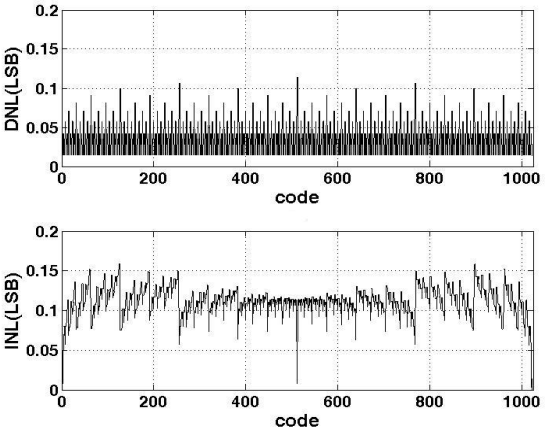


Fig. 12. Linearity simulation results of 10,000 Monte Carlo runs, where the standard deviation of the INL and DNL are plotted versus output code at the 10-bit level in the conventional SAR ADC. The values of the unit capacitors are taken to be Gaussian random variables with standard deviation of 5% (σ_0/C_0=0.05), and the ADC is otherwise ideal.

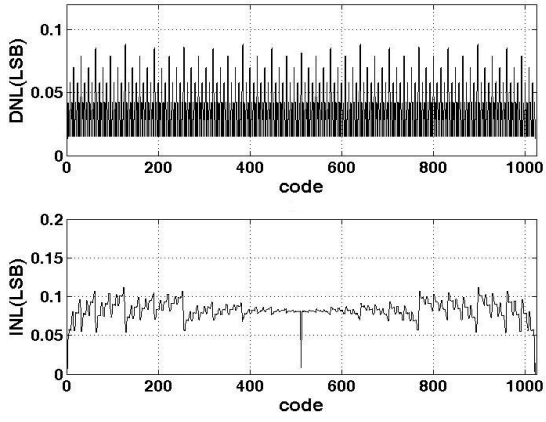


Fig. 13. Linearity simulation results of 10,000 Monte Carlo runs, where the standard deviation of the INL and DNL are plotted versus output code at the 10-bit level in the Dual Sampling SAR ADC. The values of the unit capacitors are taken to be Gaussian random variables with standard deviation of 5% (σ_0/C_0=0.05), and the ADC is otherwise ideal.

Each bit is decided as Eq. (7) in the Dual Sampling SAR ADC, where $x_{dual\_upp\_tot}$ indicates sum of capacitor mismatch in upper capacitive DAC, $x_{dual\_upp\_n}$ indicates capacitor mismatch of n-th capacitor in upper capacitive DAC, $x_{dual\_low\_tot}$ indicates sum of capacitor mismatch in lower capacitive DAC and $x_{dual\_low\_n}$ indicates capacitor mismatch of n-th capacitor in lower capacitive DAC.

$$\arg\min_{D_{D(0)}\cdots D_{D(n-1)}} \left| V_{ref} \times \left(\frac{1}{2} \times \left(\frac{(2^{n-1} + x_{dual\_upp\_0}) D_{D(0)} + \ldots + (x_{dual\_upp\_n-1}) D_{D(n-1)}}{2^n + x_{dual\_upp\_tot}} \right. \right. \right.$$
$$\left. \left. \left. + \frac{(2^{n-1} + x_{dual\_low\_0}) \overline{D_{D(0)}} + \ldots + (x_{dual\_low\_n-1}) \overline{D_{D(n-1)}}}{2^n + x_{dual\_low\_tot}} \right) + \frac{1}{2} \right) - V_{in} \right| \quad (7)$$

In the case of the Dual Sampling SAR ADC, error terms are multiplied by half compared with the Conventional SAR ADC as shown in Eq. (6) and Eq. (7). This factor effects to the linearity characteristics.

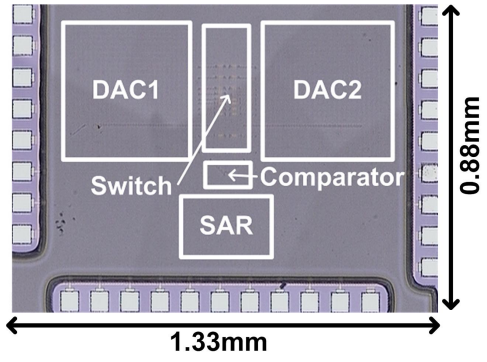


Fig. 14. Photomicrograph of the test chip.

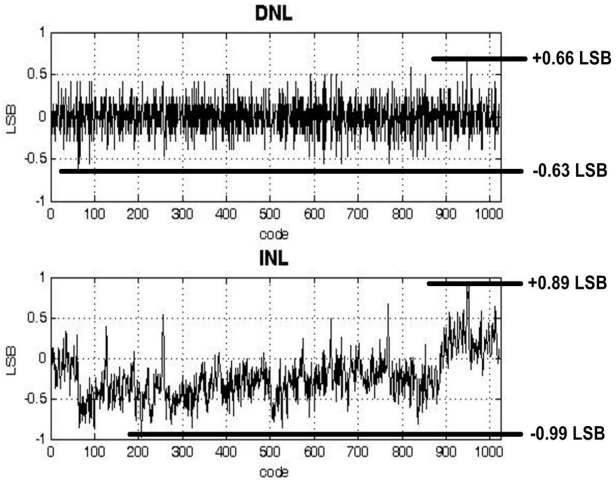


Fig. 15. Measured DNL/INL plots of ADC.

V. IMPLEMENTATION RESULTS

The ADC has been fabricated in a 0.18-μm CMOS technology. A die photograph is shown in Fig. 14. The static performance of the ADC is shown in Fig. 15. To overcome capacitor mismatch problem in layout, common centroid layout method is chosen for this work and recursive rearrange of layout is done with post layout simulation. The DNL is in the range of -0.63/+0.66 and INL is in the range of -0.98/+0.89.

The dynamic performance of the ADC is shown in Fig. 16. A fast Fourier transform of a 1 kHz sine wave input sampled at 100 kS/s is shown in Fig. 16 (a). ADC has its peak at 1 kHz with 52.4 dB of SNDR. It corresponds to an effective number of bit (ENOB) of 8.4 bits. The input frequency swept from DC to Nyquist and corresponding SNDR is plotted in Fig. 16(b). The SNDR does not drop by 3 dB until past the Nyquist frequency.

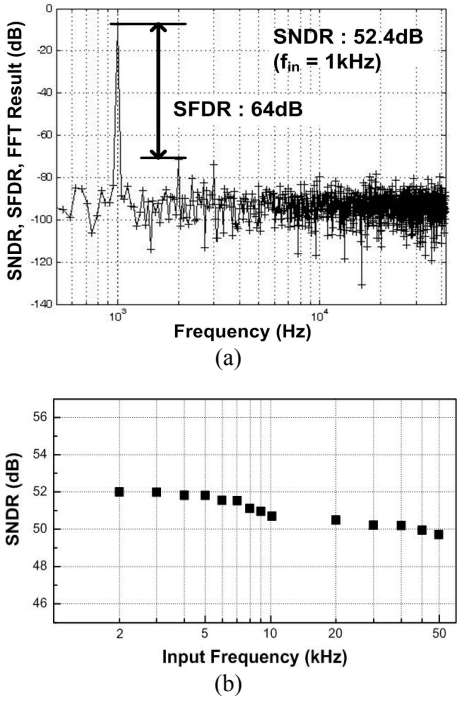


Fig. 16. (a) FFT of 1kHz sine wave sampled at 100 kS/s, (b) SNDR at input frequency swept from DC to Nyquist frequency.

Table 1 shows the summary of performance with this work. It is fabricated in 0.18-μm CMOS 1P6M. The supply voltage is 1 V, and has 100 kS/s sampling rate. Input range is 0 V – 600 mV. It achieves SNDR of 52.4 dB with 1 kHz sine wave sampled at 100 kS/s. This Figure of merits has 40 fJ/conversion-step. Its area is 1.33 mm × 0.88 mm with 53 fF of unit capacitance including pads.

Table 2 shows performance comparisons with other works. The proposed ADC spends least energy with an efficient conversion step. It has least power dissipation with 1.1 μW compared with other works. FoM(Figure of Merits) is also least value with 40 fJ/conversion-step compared with other works.

Table 1. Summary of Performance

Technology	0.18 μm CMOS 1P6M
Supply Voltage	1 V
Sampling Rate	100 kS/s
Resolution	10-bit
Input Range	0-600 mV
SNDR (f_{in} = 1 kHz)	52.4 dB
ENOB	8.4
FOM	40 fJ/c-s
Active Area (including pads)	1.33 mm × 0.88 mm

VI. CONCLUSIONS

An energy-efficient SAR ADC is presented. The proposed Dual-Sampling architecture provides energy-efficient switching process with capacitive DAC divided into two. This Dual Sampling architecture saves switching energy at calculation phase by 62% compared with the conventional architecture [5] and 40% compared with the split cap architecture [6] in 10-bit resolution.

Table 2. Performance Comparison

Source	JSSC ’07 [8]	JSSC ’07 [9]	ISSCC ’08 [10]	This Work
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Supply Voltage(V)	1 V	0.9 V	1 V	1 V
Sampling Rate	100 kS/s	200 kS/s	100 kS/s	100 kS/s
ENOB	10.55	7.58	9.4	8.4
FoM	166 fJ/c-s	64 fJ/c-s	56 fJ/c-s	40 fJ/c-s
Power Dissipation	25 μW	6.15 μW	3.8 μW	1.1 μW

Also, it is more robust to capacitor mismatch than the conventional architecture due to its cancelling effect of each capacitive DAC. It is demonstrated by ADC test chip with 1.1 μW, 1 V, 8.4-ENOB performance.

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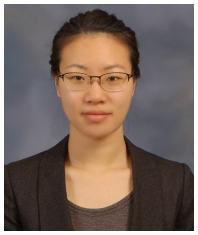

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