Experimental Characterization and Signal Integrity Verification of Interconnect Lines with Inter-layer Vias

Hyewon Kim, Dongchul Kim, and Yungseon Eo

Abstract—**Interconnect lines with inter-layer vias are experimentally characterized by using high-frequency S-parameter measurements. Test patterns are designed and fabricated using a package process. Then they are measured using Vector Network Analyzer (VNA) up to 25 GHz. Modeling a via as a circuit, its model parameters are determined. It is shown that the circuit model has excellent agreement with the measured S-parameters. The signal integrity of the lines with inter-layer vias is evaluated by using the developed circuit model. Thereby, it is shown that via may have a substantially deteriorative effect on the signal integrity of high-speed integrated circuits.**

Index Terms—**Circuit model, eye-diagram, scattering parameter, via**

I. INTRODUCTION

Over the last four decades, the circuit-switching speed and the level of integration of integrated electronic systems have dramatically improved [1]. Today's high-performance integrated circuits operate over several GHz of operating frequencies and a several tens (10s) of Gbps data rate. Recent SIP (system in a package) or three-dimensional (3D) integration technologies make even more tremendous progress in system performance and the level of the integration [2-6]. The higher level of integration inevitably requires the more I/Os(inputs/outputs) and induces more complicated routing congestion. In such systems, an area array I/O arrangement with a tight physical pitch is very common.

In next generation high-speed communication systems such as Ethernet or SONET (Synchronous Optical NETwork), high-speed chips with data rates of more than 100 Gbps are required [7-9]. Additionally, high-speed data processing modules such as SerDes (Serialization and De-serialization) require a several 10s of Gbps data rate in SIP or PCB (printed circuit board) level (i.e., outside of chips). These imply that interconnect latency tends to dominate the system performance rather than the gates[10]. Therefore, the circuit reliability and data bandwidth are increasingly limited by the signal integrity exacerbation due to interconnect lines [10, 11]. Since vias change the impedance of a signal path, they may cause substantial signal deterioration in high-speed system due to reflection and additional phase variation. The distribution of vias is highly dependent on the geometrical structures and routing algorithms [12]. In geometrically far more complicated future three-dimensional chips or packages, the vias may have a considerable effect on circuit performance.

While via effects have to be taken into account in the early phase of circuit design, the characterization of via is not straightforward. One of the reasons for this is that vias are not uniform transmission line structures [13]. There have been many techniques to characterize and model vias [14-23], however, most of them are based on numerical calculation [14-16], commercial field solvers [17, 18], or simple closed form models [19, 20]. There are relatively few experimental characterization techniques [21-23]. In practice, it is inherently difficult to accurately characterize a small via because of parasitics. Further, an air calibration using SMA connectors may not be

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suitable for de-embedding the parasitic effects.

In this work, test patterns for inter-layer via characterizations are designed and fabricated by using a package process. Two-port S-parameters for them are measured by using a VNA up to 25 GHz. Then representing the via by well-known circuit models (i.e., T-type and pi-type model), its model parameters are determined. It is shown that the circuit model has excellent agreement with the measured S-parameters. The signal integrity of the lines with inter-layer vias is evaluated in terms of eye-opening. It is shown that vias may induce substantial signal integrity deterioration in high-speed integrated system.

II. EXPERIMENTAL CHARACTERIZATION

1. Motivation for Via Characterization

A typical data path of an integrated system is configured with several vias as schematically described in Fig. 1. Since the impedance of a via is, in general, not matched with line segments, it may cause impedance mismatching (i.e., many reflection waves) during the signal transients. In many cases, since the line length between the discontinuities is not so long, the via effect may not appear in low frequencies. Thus, the via effects appear superficially to be insignificant in low-speed systems. However, this is not the case in high-speed circuits since the reflected waves between the discontinuities lead to resonance in relatively high-frequencies. In order to investigate the extent of the effect of vias on the signal integrity, the S-parameters of the line including the vias are compared with straight lines as shown in Fig. 2. Although the total length of the line including the vias is 2.1 mm, its S21 characteristic is comparable to the 10 mm long straight line. Thus, as far as a via is concerned, it is essential to characterize the effects in a broad frequency band over several 10s of GHz.

Although time domain reflectometry / time domain transmission (TDR/TDT) measurement techniques for via characterizations are often used [21], they may not be sufficiently accurate since the typical TDR/TDT equipment bandwidth is less than 10 GHz. A much more accurate frequency domain characterization can be achieved with VNA. Alternatively, SPICE provides macro-models, the W-model and the S-model, which can

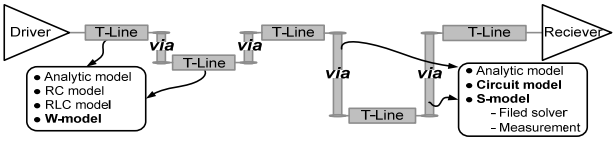


Fig. 1. Typical data link in an integrated system.

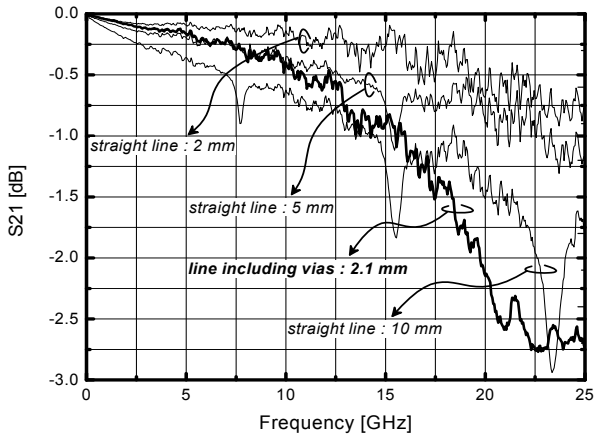


Fig. 2. S-parameter measurement data.

incorporate the S-parameter data of circuit components within a SPICE netlist. For a SPICE simulation using macro models, S-parameters for circuit components can be determined from either field-solver-based calculation or high-frequency measurements. However, such techniques have the following fundamental limitations which may be very risky in high-speed circuit designs. Not only do very high-frequency measurements cost too much even if it is possible to obtain them, but also the co-planar structure measurements are very error-prone due to the parasitics. Further, since a via is considered to be a two-port network, special test pattern and measurement techniques are required which will be discussed in more detail in the sub-section entitled "Experimental Characterization of Vias". A field solver does not accurately reflect real world characteristics of circuit components such as process variations and non-ideal frequency-variant transmission line characteristics; in a package process, a 10% process variations in both the dielectric thickness and metal pitch are typical. Finally, although the SPICE S-model extrapolates the frequency-variant characteristics that exceed the measured frequency band, it may not accurately reflect practical high-frequency characteristics. An incorrect extrapolation of high-frequency data may lead to significant misinterpretation of high-speed circuit performance. In order to demonstrate it, signal transients of 3 cm-long trans-

mission line with 4 vias are compared by using the two types of data. For the first type of data, S-parameter data for the test line are determined by using a SPICE W-model up to 10 GHz and then extrapolated from 10 GHz to 100 GHz with a SPICE S-model. The second type of data is determined with the SPICE simulation for the same test line up to 100 GHz without any extrapolation. As shown in Fig. 3, extrapolation is not accurate. SPICE S-model extrapolates S21 inaccurately while suppresses S11 as zero (large negative value in dB) which implies perfect matching (i.e., no reflection). Due to the inaccurate extrapolation of high-frequency data, time domain response of the extrapolated data show discrepancy from the reference data as shown in Fig. 4. Such discrepancy results in significant signal integrity deterioration (i.e., inter-symbol interference).

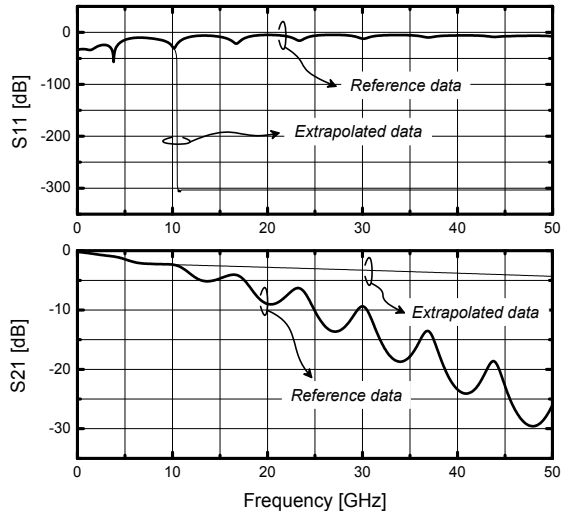


Fig. 3. Extrapolated S-parameters.

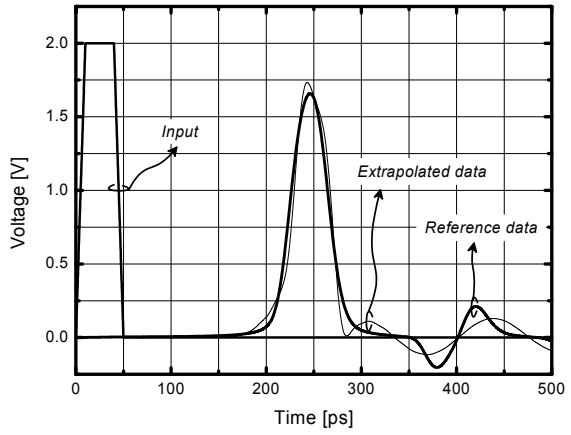


Fig. 4. Time-domain responses. Note, the difference may result in significant error in eye-opening evaluation.

2. Experimental Characterization of Vias

Since a via is too tiny in its size to be accurately characterized in high-frequencies by using SMA connectors that may induce large parasitic effects during measurements, a planar interconnect line characterization technique should be employed. The planar circuit probing for 2-port network measurements requires a pair of contact pads on the same plane. Otherwise, two port measurements may not be possible. Thus, two vias should be considered a pair for the via characterizations. That is, one is an upper layer to lower layer via and the other is a lower layer to upper layer via. Furthermore, although the access lines between the contact pad and the via are necessary, they have to be de-embedded for an accurate characterization. Thus, a 0.5 mm-long line is designed on the same test module for the purpose of parasitic effect de-embedding. The test patterns and its cross-sectional dimensions are described in Fig. 5.

A VNA for the test pattern measurements is calibrated by an SOLT (short, open, load, and thru) calibration method up to probe tips. Then, S-parameters for the test patterns including access lines are measured from 50 MHz to 25 GHz by using microwave probe tips (Cascade Microtech GSG probe tips).

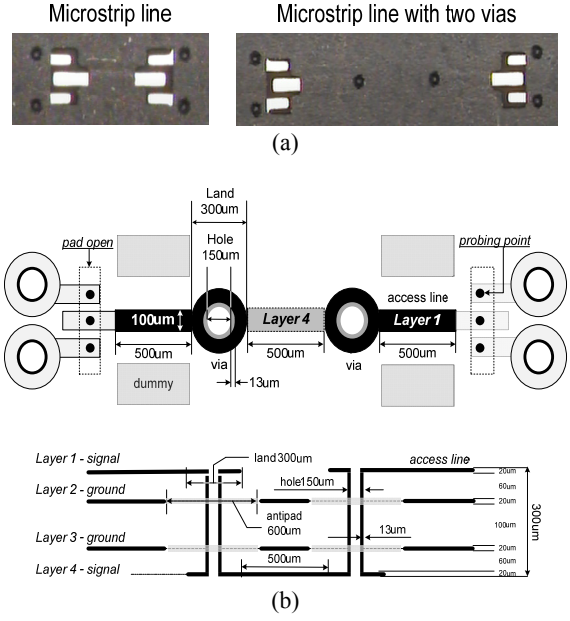


Fig. 5. Test patterns. (a) Photograph, (b) Layout dimension and cross-section.

III. CIRCUIT MODELING

1. Circuit Model and Parameter Determination

Considering the electromagnetic field distribution of a signal line through two vias, a via may be represented by one of the two possible circuit models: a T-type model and a Pi-type model as shown in Fig. 6.

Test pattern measurement system can be represented by cascaded ABCD or T-network. The measured S-parameter data of the test structure are represented by using ABCD matrices

$$[ABCD]_{total} = [ABCD]_{line}[ABCD]_{DUT}[ABCD]_{line}. \quad (1)$$

Therefore, the de-embedded S-parameters for DUT (device under test) can be readily determined as

$$[ABCD]_{DUT} = [ABCD]_{line}^{-1}[ABCD]_{total}[ABCD]_{line}^{-1}. \quad (2)$$

In the T-type model of Fig. 6(a), the measured S-parameter data can be equated by using the ABCD network parameters as follows

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{DUT}} = \begin{bmatrix} 1+\frac{Z_1}{Z_3} & \frac{Z_1Z_2+Z_2Z_3+Z_3Z_1}{Z_3} \\ \frac{1}{Z_3} & 1+\frac{Z_2}{Z_3} \end{bmatrix}_{\text{T-Type}}, \quad (3)$$

where the measurement reference impedance Z0 = 50[Ω]. Thus, the circuit model parameters for the T-type network can be determined as follows

$$\mathrm{Im}(1/Z_3)/\omega = \mathrm{Im}(C)/2\pi f = C_{\mathrm{via}}^{\mathrm{T}}, \quad (4)$$

$$\mathrm{Im}(Z_2)/\omega = \mathrm{Im}\big((D-1)/C\big)/2\pi f = L_{\mathrm{via}}^{\mathrm{T}}. \quad (5)$$

Similarly, since the ABCD parameters for the Pi-type circuit model are

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{DUT}} = \begin{bmatrix} 1+\frac{Y_2}{Y_3} & \frac{1}{Y_3} \\ \frac{Y_1Y_2+Y_2Y_3+Y_3Y_1}{Y_3} & 1+\frac{Y_1}{Y_3} \end{bmatrix}_{\text{Pi-Type}}, \quad (6)$$

then the circuit model parameters can be determined by

$$\mathrm{Im}(Y_1)/\omega = \mathrm{Im}\big((D-1)/B\big)/2\pi f = C_{\mathrm{via}}^{\pi}, \quad (7)$$

$$\mathrm{Im}(1/Y_3)/\omega = \mathrm{Im}(B)/2\pi f = L_{\mathrm{via}}^{\pi}. \quad (8)$$

The total inductances and total capacitances for each circuit model are defined, respectively, as

$$L_{\mathrm{total}}^{\mathrm{T}} \equiv 2L_{\mathrm{via}}^{\mathrm{T}}, L_{\mathrm{total}}^{\pi} \equiv L_{\mathrm{via}}^{\pi}, \quad (9)$$

$$C_{\mathrm{total}}^{\mathrm{T}} \equiv C_{\mathrm{via}}^{\mathrm{T}}, C_{\mathrm{total}}^{\pi} \equiv 2C_{\mathrm{via}}^{\pi}. \quad (10)$$

The total inductances and total capacitances of the test structure are compared in Fig. 7 and Fig. 8, respectively.

Note, regardless of the circuit model type (T-type or Pi-type) of the test structure, the circuit model parameters show excellent agreement up to 5 GHz. On

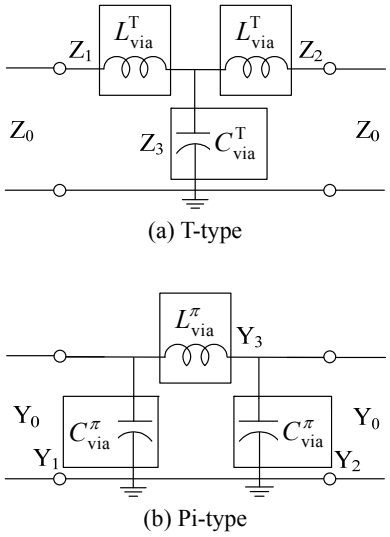


Fig. 6. Via circuit models.

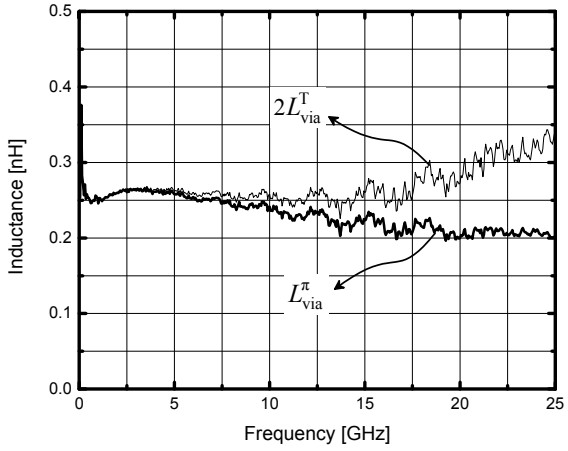


Fig. 7. Extracted total inductances for the test structure.

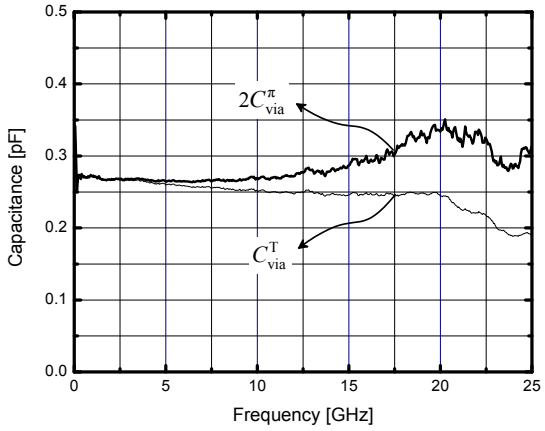
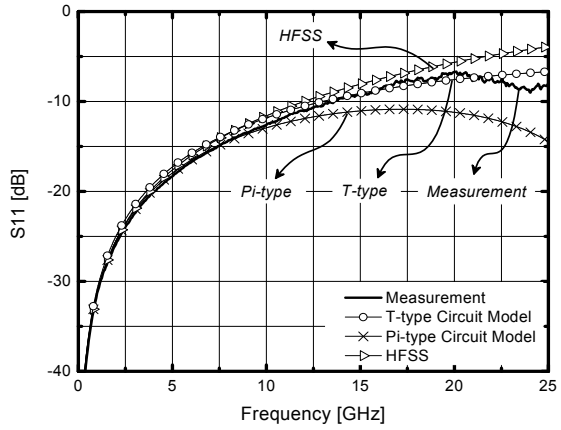
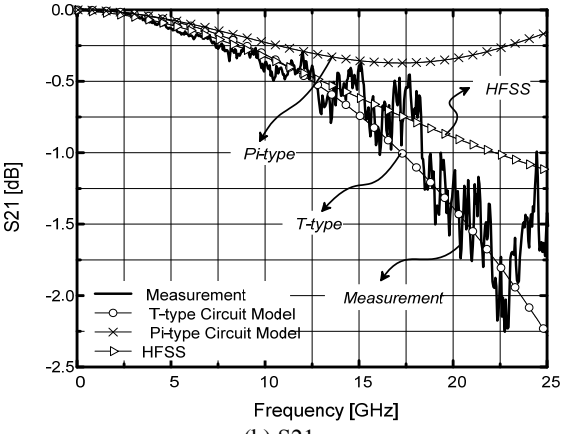


Fig. 8. Extracted total capacitances for the test structure.



(a) S11



(b) S21

Fig. 9. Comparison of extracted model parameters between the measurement data and the field-solver-based simulation.

the contrary, as the frequency increases, large discrepancy between the models becomes evident. This is considered to be due to the different lumped circuit models since the circuit model parameters scarcely vary with frequency. Therefore, the circuit model parameter values are averaged in 100 MHz to 5 GHz range. The total inductance and total capacitance are 0.26 nH and 0.26 pF, respectively.

2. Circuit Model Verification

In order to verify the accuracy of the experimental characterization, the S-parameters of the two types of circuit models are determined by performing SPICE simulations. In order to provide physical insight, the S-parameters using a commercial field solver are also determined. HFSS [24] is considered one of good references. Subsequently the extracted S-parameters are compared with measurement data as shown in Fig. 9. Up to 10 GHz, whichever technique is employed, both S11 and S21 has excellent agreement with the measurement data. Further, it is considered that the T-type circuit model for the via test structure is better than the Pi-type circuit model. However, the models shows deviation from the measurement data a bit as frequency increases. Nonetheless, judging from overall frequency range, T-parameter model is considered a reasonable circuit model to be employed for the signal integrity verification of discontinuous interconnect line. In order to further investigate the model accuracy, the circuit model for transmission lines with multiple vias (see Fig. 10) is compared with measurement data as shown in Fig. 11. The T-type model shows excellent agreement with the measurement data.

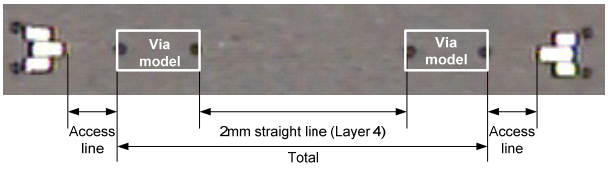


Fig. 10. Test pattern for verification.

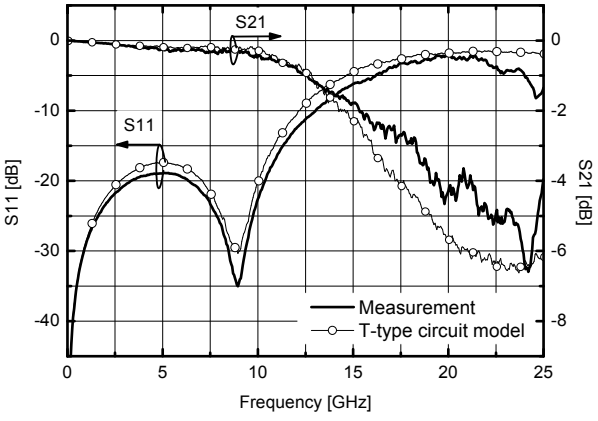


Fig. 11. Circuit model verification of the test pattern.

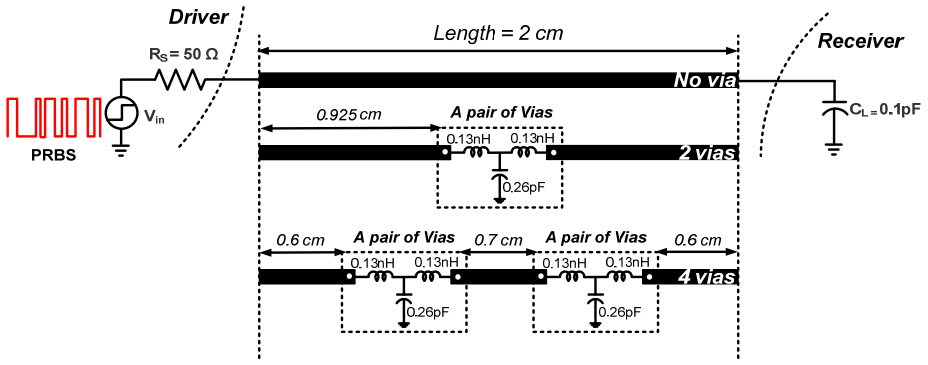


Fig. 12. Interconnect test structures for performance evaluation.

IV. Signal Integrity Verification

In order to investigate via effects, a practical interconnect system is considered as shown in Fig. 12. Note, the straight length between both ends of all of the structures is 2 cm long. SPICE-simulation-based S-parameters for the three types of line structures (i.e., a line with no via, a line with 2 vias, and a line with 4 vias) are determined by using the T-type via circuit models and compared in Fig. 13. Next, the transmission line parameters are determined by using two-dimensional field solver. It becomes evident that vias have a significant effect in high-frequencies. Further, assuming that the rise (fall) time (i.e., edge rate) is 20% of a bit period, the signal power spectrums for the various data rates are calculated as shown in Fig. 14. It is apparent that in data links with vias, signals may be significantly exacerbated.

An eye-diagram is a very helpful metric for intuitively and quickly assessing the performance quality of digital signals. That is, the signal integrity can be easily estimated with jitter and eye opening from the eye-diagram. Eye-diagrams are, in general, determined by overlapping the continual output responses for numerous PRBS (pseudo-random bit sequence) input signals. In order to evaluate the signal integrity of interconnect lines with inter-layer vias, a test circuit as shown in Fig. 12 is employed. Then eye-diagrams for the test circuit is determined by using the T-type via circuit model. With design variables such as data rate and the number of vias, eye diagrams using 50,000 PRBS are determined. In order to clearly show the signal deterioration due to vias, eye-diagrams for 5 Gbps and 20 Gbps are compared in Fig. 15. Obviously, unlike the 5 Gbps data, the 20 Gbps data are seriously exacerbated. Possibly, with longer line lengths and more vias, degradation effects may be substantial even in low data rate circuits.

V. Conclusions

A via has a deteriorative effect on the signal integrity of high- speed integrated circuits and packages. In this work, interconnect lines with inter-layer vias were experimentally characterized up to 25 GHz. Then, modeling the via with the T-network, the circuit model parameters were directly determined by using the measured S-parameters. The signal integrity of the lines with vias can be efficiently evaluated by using the developed circuit model eye-opening with various circuit design variables. It was shown that the vias have a significant effect on signal deterioration. Particularly, the higher data rate, the more significant the signal integrity degradation becomes.

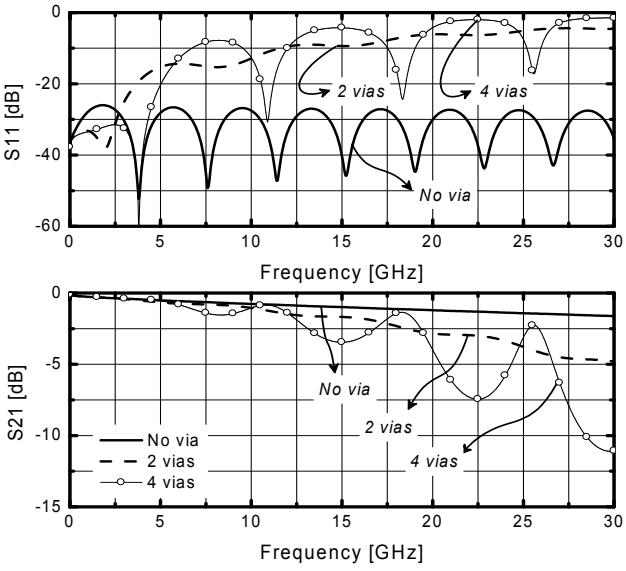


Fig. 13. Comparison of S-parameters of the test structures.

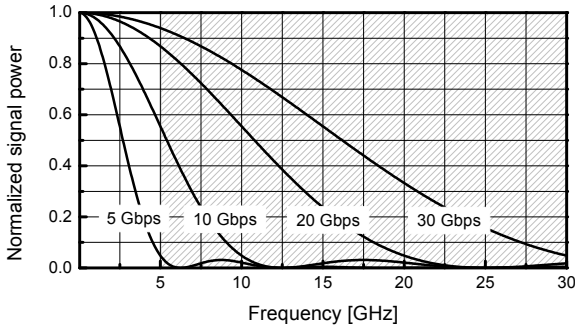


Fig. 14. Input signal power spectrum. A via has a significant effect in gray area.

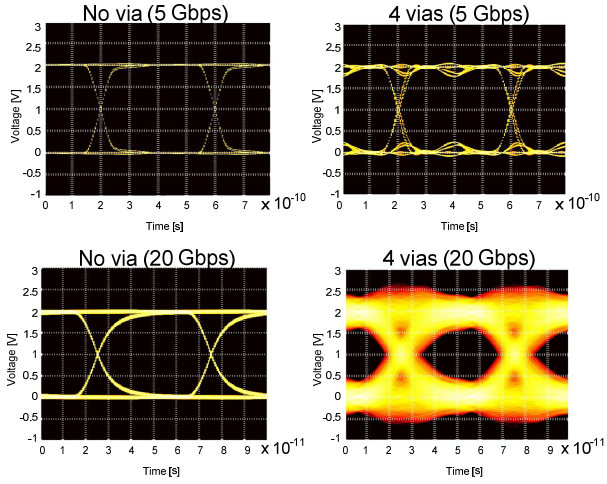


Fig. 15. Eye-diagrams determined by using the T-type circuit model.

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