Sign-Select Lookahead CORDIC based High-Speed QR Decomposition Architecture for MIMO Receiver Applications

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Abstract—**This paper presents a high-speed QR decomposition architecture for the multi-input-multi-output (MIMO) receiver based on Givens rotation. Under fast-varying channel, since the inverse matrix calculation has to be performed frequently in MIMO receiver, a high performance and low latency QR decomposition module is highly required. The proposed QR decomposition architecture is composed of Sign-Select Lookahead (SSL) coordinate rotation digital computer (CORDIC). In the SSL-CORDIC, the sign bits, which are computed ahead to select which direction to rotate, are used to select one of the last iteration results, therefore, the data dependencies on the previous iterations are efficiently removed. Our proposed QR decomposition module is implemented using TSMC 0.25 μm CMOS process. Experimental results show that the proposed QR architecture achieves 34.83% speed-up over the Compact CORDIC based architecture for the 4 × 4 matrix decomposition.**

Index Terms—**QR decomposition, Givens rotation, CORDIC, high-performance CORDIC, vectoring mode, sign prediction, lookahead**

I. INTRODUCTION

Recent explosive growth of the portable multimedia communication and computing devices demands high performance and low power very large scaled integration (VLSI) implementation of complex digital signal processing (DSP) algorithms. In communication, due to the high spectral efficiencies offered by multiple-input multiple-output (MIMO) system, the MIMO technology is chosen in many standards like IEEE 802.16e/m (WiMAX), long term evolution (LTE) projects and emerging 4 G systems [1]. Two main challenges encountered with the MIMO technology are the design of high-throughput and high-performance detectors and cost-effective VLSI implementations with a large number of antennas and constellation order.

Matrix decomposition and matrix inversion are the most fundamental operations performed in MIMO receivers [2]. Especially, in MIMO demodulation, the matrix size becomes larger as the number of antenna increases, thus significantly increasing the computational complexity for matrix decomposition or inversion. Moreover, when complex-valued matrices are used for channel model, the complexity becomes even aggravated. In orthogonal frequency division multiplexing (OFDM) system [3], where MIMO technique is widely applied in practice, the decomposition or inversion of channel matrix should be performed frequently (every a few μsec) in the case where the channel is different in each sub-carrier and varies with the maximum speed [4, 5]. Therefore, efficient hardware architectures of matrix decomposition, where the matrix operations are performed in faster clock speed with low latency, are highly required.

Many previous research efforts are focused on the high-performance VLSI implementation of matrix inversion [6-8]. Triangular systolic arrays (TSA) [9] are frequently used for matrix inversion with the properties

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of inherent parallelism and pipelining. The lattice arrangement of the basic processing unit in the systolic array is suitable for executing regular matrix-type computation. However, the array architecture needs considerable number of clock cycles to get all the inputs.

Recently, QR decomposition with Givens rotation [10] is widely adopted in matrix inversion for MIMO receivers [11-13], as it can be efficiently implemented using simple coordinate rotation digital computer (CORDIC) module. Since it was first proposed in 1959 [14], the CORDIC has been widely used to calculate the trigonometric functions in digital signal processing (DSP) systems. Although CORDIC can be implemented using only shifters and adders, it has performance limitations due to its inherent iterative computations [15]. In the QR matrix decomposition architecture mentioned above, since the CORDIC module is the most important core, speeding-up the CORDIC module is the fundamental requirement for high performance QR operations.

The main contribution of this paper is to develop a high speed CORDIC architecture, where the data dependencies from previous iterations can be efficiently overcome in the vectoring mode. A unified architecture of the vectoring and rotation modes of CORDIC operation is also proposed. Finally, using the proposed CORDIC, a high-speed and low-latency QR decomposition hardware is implemented. The rest of the paper is organized as follows. The basics of MIMO and QR decomposition algorithm are presented in section II. Section III explains the CORDIC algorithm and architecture, and our proposed Sign-Select Lookahead CORDIC (SSL-CORDIC) is proposed in section III. In section IV, using the proposed SSL-CORDIC, a hardware architecture of the high-performance QR decomposition is presented. The implementation results of the proposed architecture are presented in Section V. Comparison results with other QR decomposition architectures are also shown in Section V. Finally, conclusions are drawn in section VI.

II. System Model and QR Decomposition Algorithm

1. MIMO System

We consider a spatial multiplexing MIMO system with Nt transmit and Nr receive antennas for transmission and reception [16]. At the MIMO receiver, the received signal can be expressed in discrete time as

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n} \tag{1}$$

, where $\mathbf{y}$ is the ($Nr \times 1$) size of signal vector $\mathbf{y} = [y_1, y_2, ..., y_{Nr}]^T$, and here, y_j, (j=1, … , Nr) is the received data at the jth receive antenna. $\mathbf{x}$ represents ($Nt \times 1$) size of the transmitted signal vector $\mathbf{x} = [x_1, x_2, ... , x_{Nr}]^T$. Here, x_i, (i=1, … , Nt) is the transmitted symbol sent from ith transmit antenna. The channel impulse response of each multi path is represented by ($Nr \times Nt$) size of channel matrix $\mathbf{H}$ with $Nr \geq Nt$, and the (j, i) element of $\mathbf{H}$ indicates the channel gain between ith transmit antenna and jth receive antenna. $\mathbf{n}$ represents the additive white Gaussian noise vector of ($Nr \times 1$) size.

Assuming the known channel matrix $\mathbf{H}$, the matrix inversion is needed in order to demodulate $\mathbf{x}$ signal from the received signal $\mathbf{y}$. In general, the matrix inversion needs large amount of computations, and the computational complexity increases drastically as the number of antenna increases. QR decomposition is gaining popularity due to its relatively smaller complexity.

2. QR Decomposition Algorithm using Givens Rotation Method

The basic principal of QR decomposition is to decompose a matrix $\mathbf{H}$ into unitary matrix $\mathbf{Q}$ with orthogonal columns and upper triangular matrix $\mathbf{R}$, which is expressed as

$$\mathbf{H} = \mathbf{Q}\mathbf{R} . \tag{2}$$

Substituting Eq. (2) with Eq. (1), the equation is rewritten as following,

$$\mathbf{y} = \mathbf{Q}\mathbf{R}\mathbf{x} + \mathbf{n} . \tag{3}$$

Using Hermitian transpose matrix $\mathbf{Q}^H$, $\mathbf{Q}^H\mathbf{y}$ can be derived as following,

$$\begin{aligned} &\hat{\mathbf{y}} = \mathbf{Q}^H\mathbf{y} = \mathbf{Q}^H\mathbf{Q}\mathbf{R}\mathbf{x} + \mathbf{Q}^H\mathbf{n} = \mathbf{R}\mathbf{x} + \mathbf{Q}^H\mathbf{n} = \mathbf{R}\hat{\mathbf{x}} \\ &\Rightarrow \hat{\mathbf{x}} = \mathbf{R}^{-1}\hat{\mathbf{y}} \end{aligned} \tag{4}$$

, where $\mathbf{Q^H n}$ is still a Gaussian random noise vector [17]. From Eq. (4), $\mathbf{Q^H}$ and $\mathbf{R^{-1}}$ matrix can be computed to obtain $\hat{\mathbf{x}}$.

At first, from the Eq. (2), matrix $\mathbf{R}$ is expressed as,

$$\mathbf{R} = \mathbf{Q^H H} . \tag{5}$$

The upper triangular matrix $\mathbf{R}$ can be obtained using Givens rotation, where the approach makes the selective zero insertion into one of the two selected rows [13]. For example, let's assume a 2 × 2 complex matrix $\mathbf{H}$,

$$\mathbf{H} = \begin{bmatrix} \mathbf{h_{11}} & \mathbf{h_{12}} \\ \mathbf{h_{21}} & \mathbf{h_{22}} \end{bmatrix} . \tag{6}$$

Since each of the elements in matrix $\mathbf{H}$ is a complex number, the Eq. (6) can be represented as following,

$$\mathbf{H} = \begin{bmatrix} h_{r11} + h_{i11}j & h_{r12} + h_{i12}j \\ h_{r21} + h_{i21}j & h_{r22} + h_{i21}j \end{bmatrix} = \begin{bmatrix} |h_{11}|e^{j\theta_{11}} & |h_{12}|e^{j\theta_{21}} \\ |h_{21}|e^{j\theta_{21}} & |h_{22}|e^{j\theta_{22}} \end{bmatrix} \tag{7}$$

, where θ denotes the argument of corresponding complex elements. When the matrix $\mathbf{H}$ is multiplied with the following $\mathbf{Q^H}$, from Eq. (5) the resulting matrix is upper triangular matrix and all the diagonal components become real numbers. Following shows the $\mathbf{Q^H}$ matrix,

$$\mathbf{Q^H} = \begin{bmatrix} 1 & 0 \\ 0 & e^{-j\theta'_{22}} \end{bmatrix} \cdot \begin{bmatrix} \cos\theta_1 & \sin\theta_1 \\ -\sin\theta_1 & \cos\theta_1 \end{bmatrix} \cdot \begin{bmatrix} e^{-j\theta_{11}} & 0 \\ 0 & e^{-j\theta_{21}} \end{bmatrix} \tag{8}$$

, where $\theta_1 = \tan(|h_{21}| / |h_{11}|)$. Thereafter, using the back substitution method, $\mathbf{R^{-1}}$ can be obtained.

III. SIGN-SELECT LOOKAHEAD CORDIC ARCHITECTURE

1. Conventional CORDIC Approaches

As mentioned earlier, each rotation matrix which composes $\mathbf{Q^H}$ in Eq. (8) can be realized using the vectoring and rotation modes of CORDIC algorithm. The CORDIC algorithm can be represented by the following numerical expression of vector rotation [14],

$$\begin{bmatrix} x_1 \\ y_1 \\ z_1 \end{bmatrix} = \begin{bmatrix} -\sigma_1 y_0 \\ \sigma_1 x_0 \\ \sigma_1 \cdot 90 \end{bmatrix} \quad \text{<1st iteration>}$$
$$\begin{bmatrix} x_i \\ y_i \\ z_i \end{bmatrix} = \begin{bmatrix} x_{i-1} - \sigma_i 2^{2-i} y_{i-1} \\ y_{i-1} + \sigma_i 2^{2-i} x_{i-1} \\ z_{i-1} - \sigma_i \alpha_i \end{bmatrix} \quad \text{<}i\text{th iteration>} . \tag{9}$$

Here, x and y represent the vector coordinate components of x and y axis, respectively, and i means the ith iteration step. σ is the sign-bit that can be +1 or -1 indicating the direction of the vector rotation, and z represents the accumulated rotation angle. α denotes the predefined angle value of each micro-rotation step, $\alpha_i = \arctan(2^{2-i})$, which can be implemented using shifters. The block diagrams of the vectoring and rotation mode are shown in Fig. 1(a) and (b), respectively. As shown in Fig. 1(a) and (b), we can calculate the amplitude and argument of a given vector using the vectoring mode, and the sine and cosine values of the given angle using the rotation mode.

If a system uses the rotation CORDIC right after the vectoring CORDIC for the calculation of sine or cosine value of given vectors, the two modes can be operated simultaneously using Compact CORDIC architecture which uses sign-bit sharing method [18]. Thus, it does not need to calculate the argument of given vector so that the look up table can be perfectly removed. Fig. 2 indicates the concept of Compact CORDIC.

With the vectoring and rotation mode CORDIC, we can calculate various elementary functions with relatively small hardware complexity. The CORDIC, however, has inherent bottleneck - the data dependencies on previous iterations for which next iterations should wait - fundamentally limiting the serial operations. In

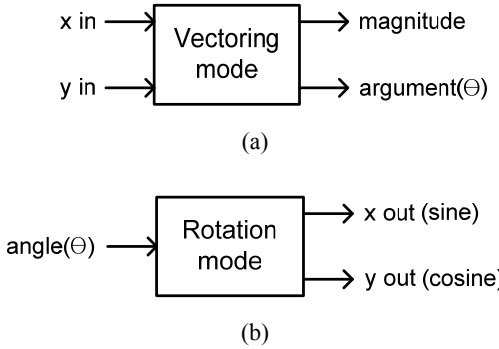


Fig. 1. Block diagram of (a) Vectoring, (b) Rotation mode.

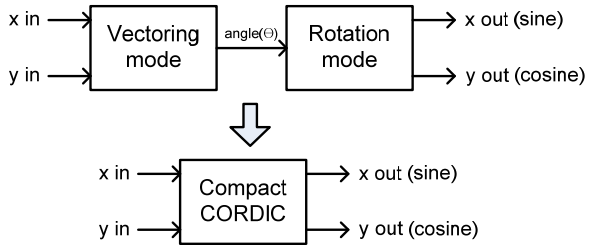


Fig. 2. Concept of Compact CORDIC architecture.

order to get over the data dependencies shown above, lookahead approach was proposed [19-21]. Eq. (10) shows an example of 4-iteration step lookahead CORDIC algorithm,

$$\begin{bmatrix} x_4 \\ y_4 \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} -\alpha_1\alpha_2 \\ -\alpha_1\alpha_3 2^{-1} \\ -\alpha_1\alpha_4 2^{-2} \\ +\alpha_1\alpha_2\alpha_3\alpha_4 2^{-3} \end{bmatrix} & \begin{bmatrix} -\alpha_1 \\ +\alpha_1\alpha_2\alpha_3 2^{-1} \\ +\alpha_1\alpha_2\alpha_4 2^{-2} \\ +\alpha_1\alpha_3\alpha_4 2^{-3} \end{bmatrix} \\ \begin{bmatrix} \alpha_1 \\ -\alpha_1\alpha_2\alpha_3 2^{-1} \\ -\alpha_1\alpha_2\alpha_4 2^{-2} \\ -\alpha_1\alpha_3\alpha_4 2^{-3} \end{bmatrix} & \begin{bmatrix} -\alpha_1\alpha_2 \\ -\alpha_1\alpha_3 2^{-1} \\ -\alpha_1\alpha_4 2^{-2} \\ +\alpha_1\alpha_2\alpha_3\alpha_4 2^{-3} \end{bmatrix} \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}. \quad (10)$$

However, previous works based on lookahead CORDIC are only applied to the rotation mode, thus it takes long time to find the sign-bits and perform the comparison operation of input angle. In the next section, we propose a new CORDIC scheme, named Sign-Select Lookahead (SSL) CORDIC, which is applicable to both of the rotation and vectoring modes of operations.

2. Sign-Select Lookahead CORDIC Architecture

As mentioned in the previous subsection, one of the main design challenges in CORDIC is that if the direction of vector rotation can be known in advance, the performance degradation due to data dependencies from previous iterations can be efficiently removed. Fig. 3 shows the architecture of our proposed SSL-CORDIC with 4-iteration step lookahead**.** As shown in the figure, the direction of vector rotation in vectoring mode is determined by checking the MSB of y component. In case of conventional CORDIC, after checking the MSB of coordinate component y_0 of input vector, carry propagation occurs in add operation. x_1 and y_1 comes out after carry propagation is done, which is the same in SSL-CORDIC architecture. However, unlike the conventional CORDIC architecture, which has to perform add operation (and carry propagation) again in order to calculate x_2 and y_2, in SSL-CORDIC, all of the iteration results can be computed in parallel taking only 1 CSA and 1 MUX delay.

In order to calculate all the possible results in each stage, the following lookahead algorithms can be applied,

$$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = \begin{bmatrix} -\alpha_1\alpha_2 & -\alpha_1 \\ \alpha_1 & -\alpha_1\alpha_2 \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}, \quad (11)$$

$$\begin{bmatrix} x_3 \\ y_3 \end{bmatrix} = \begin{bmatrix} -\alpha_1\alpha_2 - \alpha_1\alpha_3 2^{-1} & -\alpha_1 + \alpha_1\alpha_2\alpha_3 2^{-1} \\ \alpha_1 - \alpha_1\alpha_2\alpha_3 2^{-1} & -\alpha_1\alpha_2 - \alpha_1\alpha_3 2^{-1} \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}. \quad (12)$$

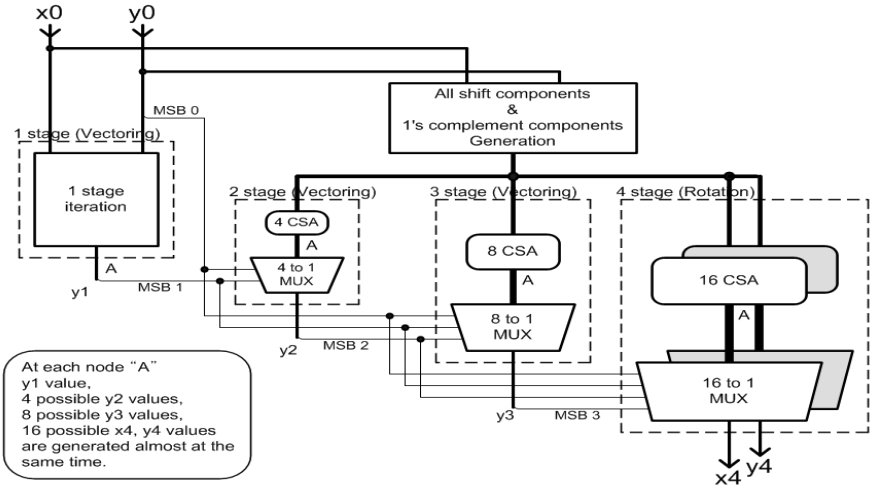


Fig. 3. Architecture of proposed Sign-Select Lookahead CORDIC (4-iteration step).

Eq. (11) and Eq. (12) are used to generate the results of stage 2 and 3, respectively, and the results of stage 4 uses Eq. (10). As shown in the equations, there are more than two terms in matrix expression such that we can use carry save adder (CSA) to compute add operation. Therefore, the result of 1st iteration step comes out and all the other possible results of each iteration step can be computed (at each node 'A' in Fig. 3) in parallel.

Meanwhile, as soon as one value from all the possible results of each stage is selected through the MUX, MSBs (sign-bits) are obtained. Since the calculations of all the possible values in each stage are done almost same time, final vector in the last stage can be selected directly after the calculations.

As mentioned earlier, using CSA structure, final CORDIC output can be obtained almost at the same time with 1st iteration step with only single carry propagation. Another advantage of the SSL-CORDIC is that, with sign-bit sharing, we can directly obtain the sine and cosine values of given vector with only changing the final stage into rotation mode. As a result, a lookup table is completely removed, and hardware complexity is reduced as well.

When the proposed approach is applied to larger lookahead, like 5 or 6-iteration steps, the required number of computation increases. Thus, it needs more time to execute CSA stages. On the other hand, higher-shift terms can be neglected since they over-run the bit width, which finally results in almost same time compared to 4-iteration case.

IV. HIGH PERFORMANCE QR DECOMPOSITION ARCHITECTURE BASED ON SIGN-SELECT LOOKAHEAD CORDIC

Using the proposed SSL-CORDIC, we propose a high performance hardware architecture of the Givens rotation based QR decomposition. First, we start from the complex channel matrix indicated in Eq. (7). The matrix can be expressed with separate real and imaginary components as following:

$$\mathbf{H}=\begin{bmatrix} h_{r11}+h_{i11}j & h_{r12}+h_{i12}j \\ h_{r21}+h_{i21}j & h_{r22}+h_{i21}j \end{bmatrix} \Rightarrow \begin{bmatrix} \begin{bmatrix} h_{r11} \\ h_{i11} \end{bmatrix} & \begin{bmatrix} h_{r12} \\ h_{i12} \end{bmatrix} \\ \begin{bmatrix} h_{r21} \\ h_{i21} \end{bmatrix} & \begin{bmatrix} h_{r22} \\ h_{i22} \end{bmatrix} \end{bmatrix}. \quad (13)$$

The imaginary components of (1, 1) and (2, 1) elements in Eq. (13) can be changed to real components using the third matrix of Eq. (8)

$$\mathbf{H}^{n1}=\begin{bmatrix} e^{-j\theta_{11}} & 0 \\ 0 & e^{-j\theta_{12}} \end{bmatrix}\cdot\begin{bmatrix} h_{r11}+h_{i11}j & h_{r12}+h_{i12}j \\ h_{r21}+h_{i21}j & h_{r22}+h_{i21}j \end{bmatrix} \quad (14)$$

, where the upper subscript 'n_k (k=1, 2, 3)' represents the number of matrix multiplication performed.

Eq. (14) can be changed into the following expression using Euler's formula,

$$\mathbf{H}^{n1}\Rightarrow\begin{bmatrix} \begin{bmatrix} \cos\theta_{11} & \sin\theta_{11} \\ -\sin\theta_{11} & \cos\theta_{11} \end{bmatrix} & \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} \cos\theta_{12} & \sin\theta_{12} \\ -\sin\theta_{12} & \cos\theta_{12} \end{bmatrix} \end{bmatrix}\cdot\begin{bmatrix} \begin{bmatrix} h_{r11} \\ h_{i11} \end{bmatrix} & \begin{bmatrix} h_{r12} \\ h_{i12} \end{bmatrix} \\ \begin{bmatrix} h_{r21} \\ h_{i21} \end{bmatrix} & \begin{bmatrix} h_{r22} \\ h_{i22} \end{bmatrix} \end{bmatrix}$$
$$=\begin{bmatrix} \begin{bmatrix} h_{r11}^{n1} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r12}^{n1} \\ h_{i12}^{n1} \end{bmatrix} \\ \begin{bmatrix} h_{r21}^{n1} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r22}^{n1} \\ h_{i22}^{n1} \end{bmatrix} \end{bmatrix}. \quad (15)$$

Now, in Eq. (15), we can use the vectoring and rotation modes of CORDIC module. Please note that the imaginary components of (1, 1) and (2, 1) elements are changed into zero values. In addition, the elimination of (2, 1) element should to be following,

$$\mathbf{H}^{n2}=\begin{bmatrix} \cos\theta_1 & \sin\theta_1 \\ -\sin\theta_1 & \cos\theta_1 \end{bmatrix}\cdot\begin{bmatrix} h_{r11}^{n1} & h_{r12}^{n1}+h_{i12}^{n1}j \\ h_{r21}^{n1} & h_{r22}^{n1}+h_{i22}^{n1}j \end{bmatrix}. \quad (16)$$

Eq. (16) can be rewritten as,

$$\mathbf{H}^{n2}=\begin{bmatrix} h_{r11}^{n1}\cos\theta_1+h_{r21}^{n1}\sin\theta_1 & \\ -h_{r11}^{n1}\cos\theta_1+h_{r21}^{n1}\cos\theta_1 & \\ & h_{r12}^{n1}\cos\theta_1+h_{r22}^{n1}\sin\theta_1+(h_{i12}^{n1}\cos\theta_1+h_{i22}^{n1}\sin\theta_1)j \\ & -h_{r12}^{n1}\sin\theta_1+h_{r22}^{n1}\cos\theta_1+(-h_{i12}^{n1}\sin\theta_1+h_{i22}^{n1}\cos\theta_1)j \end{bmatrix}$$
$$\Rightarrow\begin{bmatrix} \begin{bmatrix} \cos\theta_1 & 0 \\ 0 & \cos\theta_1 \end{bmatrix} & \begin{bmatrix} \sin\theta_1 & 0 \\ 0 & \sin\theta_1 \end{bmatrix} \\ \begin{bmatrix} -\sin\theta_1 & 0 \\ 0 & -\sin\theta_1 \end{bmatrix} & \begin{bmatrix} \cos\theta_1 & 0 \\ 0 & \cos\theta_1 \end{bmatrix} \end{bmatrix}\cdot\begin{bmatrix} \begin{bmatrix} h_{r11}^{n1} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r12}^{n1} \\ h_{i12}^{n1} \end{bmatrix} \\ \begin{bmatrix} h_{r21}^{n1} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r22}^{n1} \\ h_{i22}^{n1} \end{bmatrix} \end{bmatrix}$$
$$=\begin{bmatrix} \begin{bmatrix} h_{r11}^{n2} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r12}^{n2} \\ h_{i12}^{n2} \end{bmatrix} \\ \begin{bmatrix} 0 \\ 0 \end{bmatrix} & \begin{bmatrix} h_{i22}^{n2} \\ h_{i22}^{n2} \end{bmatrix} \end{bmatrix}. \quad (17)$$

We can also make the (2, 2) element as a real

component as following,

$$\mathbf{H}^{n3} = \begin{bmatrix} 1 & 0 \\ 0 & e^{-j\theta_{22}^{n2}} \end{bmatrix} \cdot \begin{bmatrix} h_{r11}^{n2} & h_{r12}^{n2} + h_{i12}^{n2} j \\ 0 & h_{r22}^{n2} + h_{i22}^{n2} j \end{bmatrix}. \tag{18}$$

Eq. (18) can be represented as separate form,

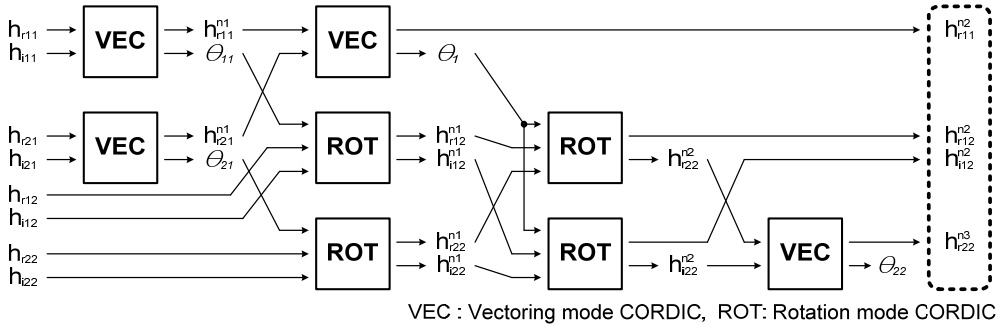
$$\begin{aligned} \mathbf{H}^{n3} \Rightarrow & \begin{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} & \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} \cos\theta_{22}^{n2} & \sin\theta_{22}^{n2} \\ -\sin\theta_{22}^{n2} & \cos\theta_{22}^{n2} \end{bmatrix} \end{bmatrix} \cdot \begin{bmatrix} \begin{bmatrix} h_{r11}^{n2} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r12}^{n2} \\ h_{i12}^{n2} \end{bmatrix} \\ \begin{bmatrix} 0 \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r22}^{n2} \\ h_{i22}^{n2} \end{bmatrix} \end{bmatrix} \\ = & \begin{bmatrix} \begin{bmatrix} h_{r11}^{n2} \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r12}^{n2} \\ h_{i12}^{n2} \end{bmatrix} \\ \begin{bmatrix} 0 \\ 0 \end{bmatrix} & \begin{bmatrix} h_{r22}^{n3} \\ 0 \end{bmatrix} \end{bmatrix} \end{aligned} \tag{19}$$

, which shows the completion of QR decomposition with upper triangular form matrix.

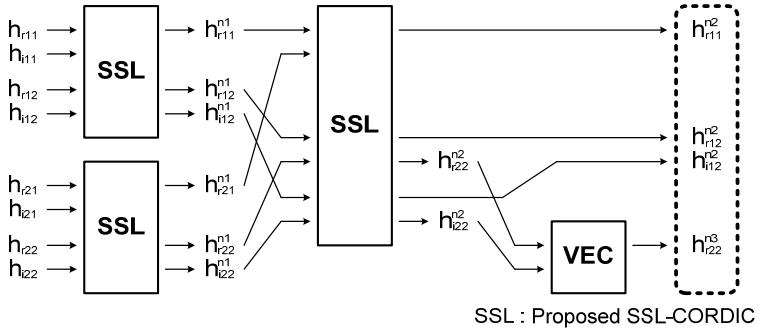
The hardware architecture of QR decomposition is shown in Fig. 4(a), where the rotation operation is fulfilled after the vectoring mode, and thus, we can apply our proposed SSL-CORDIC. Fig. 4(b) shows the architecture of proposed QR decomposition core based on SSL-CORDIC module. We can notice from the figure that the number of CORDIC stage is reduced compared to the architecture in Fig. 4(a). If the size of matrix to be decomposed becomes larger, the number of CORDIC stages increases, however, we can save more computational time using SSL-CORDIC since the increase in stage is much smaller in our proposed architecture than the conventional one.

V. NUMERICAL RESULTS

Our proposed QR decomposition hardware was implemented using TSMC 0.25 μm technology and the experimental results are compared with the TACR/TSA based hardware [9] and low complexity QR decomposition architecture [12]. Table 1 summarizes the numerical results of the various sizes of QR decomposition architectures. Here, a SSL-CORDIC, which is the core module of the proposed QR decomposition hardware, executes 12-iteration steps. In the table, *number of cycles* means the required total number of cycles to finish the QR decomposition process. For example, in case of 2 × 2 size matrix decomposition



(a)



(b)

Fig. 4. Hardware architecture of QR decomposition using (a) Conventional CORDIC architecture, (b) The proposed SSL-CORDIC architecture. (VEC: Vectoring mode, ROT: Rotation mode, SSL: SSL-CORDIC module)

Table 1. Delay and area comparisons for different QR decomposition architectures

Delay/Area Comparison (using 12-iteration step CORDIC)		TACR/TSA based architecture [9]	Using Compact CORDIC based architecture [12]	Using SSL-CORDIC based architecture (3-iteration step)	Using SSL-CORDIC based architecture (4-iteration step)
Clock cycle		73.80 *nsec*	27.10 *nsec*	19.60 *nsec*	17.66 *nsec*
2 × 2 size	Number of cycles	5 cycles	3 cycles	3 cycles	3 cycles
	Cell area	2,241,468 μm^2	1,572,108 μm^2	1,978,212 μm^2	2,592,324 μm^2
	Number of gates	54,048	37,908	47,699	62,507
3 × 3 size	Number of cycles	8 cycles	6 cycles	6 cycles	6 cycles
	Cell area	6,063,016 μm^2	5,301,668 μm^2	6,904,189 μm^2	8,425,053 μm^2
	Number of gates	146,195	127,837	154,421	203,105
4 × 4 size	Number of cycles	11 cycles	9 cycles	9 cycles	9 cycles
	Cell area	8,305,428 μm^2	14,454,672 μm^2	19,480,419 μm^2	22,814,551 μm^2
	Number of gates	200,266	348,541	433,796	516,361

with a 3-iteration step lookahead unit, the proposed SSL-CORDIC based architecture needs 3 cycles with 19.60 nsec clock (total 58.80 nsec) to finish QR decomposition, however, 3 cycles with 27.10 nsec clock (total 81.30 nsec) is spent in the Compact CORDIC based one [12].

As the number of antenna increases, the proposed QR decomposition offers an advantage of more speed. However the hardware complexity also increases. In the proposed architecture, the tradeoff between the performance advantage and the hardware complexity can be controlled by selecting an appropriate lookahead step. Table 1 shows the numerical results of the two optimal division cases, which are 3-iteration step and 4-iteration step lookahead cases. According to the results, 4-iteration step lookahead approach shows 34.83% of delay reduction at the cost of 57.84% of hardware complexity increase compared to the Compact CORDIC based architecture [12]. On the other hand, the 3-iteration step lookahead based scheme presents 27.67% performance improvements with 34.77% of hardware area increase. We can notice from the results that considering the QR decomposition application and its required performance, an adequate number of lookahead iteration steps can be decided in the proposed SSL-CORDIC based architecture.

VI. CONCLUSIONS

In this paper, we proposed a Sign-Select Lookahead CORDIC based high-performance QR decomposition architecture which can be efficiently used in MIMO receiver under fast-varying channel. The proposed SSL-CORDIC efficiently overcomes the data dependencies of previous iterations results and it can be used to facilitate both the vectoring and rotation modes. The SSL-CORDIC offers a superior performance compared to other CORDIC schemes since it can remove the basic limit of CORDIC algorithm by obtaining the direction of vector rotation in advance. Based on the proposed CORDIC, a high performance hardware architecture for QR decomposition was also proposed. According to the experimental results, our proposed QR decomposition architecture shows up to 34.83% of performance improvements over the Compact CORDIC based approach. The idea presented in this paper can assist in the design of QR decomposition algorithm and the implementations of high performance applications.

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REFERENCES

[1] Qinghua Li, et al, "MIMO Techniques in WiMAX and LTE: A Feature Overview," *Communications Magazine, IEEE,* Vol. 48, Issue 5, May. 2010, pp. 86-92.

[2] T. Kailath, H. Vikalo, and B. Hassibi, "MIMO

receive algorithms," *Cambridge, U.K.: Cambridge Univ. Press,* 2005.

[3] L. J. Cimini, "Analysis and Simulation of a Digital Mobile Channel using Orthogonal Frequency Division Multiplexing," *Communications, IEEE Transactions on,* Vol. 33, Issue 7, Jul. 1985, pp. 665-675.

[4] C. K. Singh, S. H. Prasad, and P. T. Balsara, "VLSI Architecture for Matrix Inversion using Modified Gram-Schmidt based QR Decomposition," *VLSI Design, 2007. Held jointly with 6th International Conference on Embedded Systems., 20th International Conference on,* Jan. 2007, pp. 836-841.

[5] D. C. Yu, and H. Wang, "A New Parallel LU Decomposition Method," *Power Systems, IEEE Transactions on,* Vol.5, Issue 1, Feb. 1990, pp. 303-310.

[6] Lei Ma, et al, "Modified Givens Rotations and their Application to Matrix Inversion," *Acoustics, Speech and Signal Processing, 2008. ICASSP, 2008. IEEE International Conference on,* Mar. 2008, pp. 1437-1440.

[7] Di Wu, et al, "Fast Complex Valued Matrix Inversion for Multi-User STBC-MIMO Decoding," *VLSI, 2007. ISVLSI '07. IEEE Computer Society Annual Symposium on,* 9-11, Mar. 2007, pp. 325-330.

[8] DaeGon Kim, and S. V. Rajopadhye, "An Improved Systolic Architecture for LU Decomposition," *Application-specific Systems, Architectures and Processors, 2006. ASAP '06. International Conference on*, Sept. 2006, pp. 231-238.

[9] A. Maltsev, et al, "Triangular Systolic Array with Reduced Latency for QR-decomposition of Complex Matrices," *Circuit and Systems, 2006. ISCAS 2006. Digest of Technical Papers. IEEE International Symposium on,* 21-24, May. 2006, pp. 385-388.

[10] A. El-Amawy, and K. R. Dharmarajan, "Parallel VLSI Algorithm for Stable Inversion of Dense Matrices," *Computers and Digital Techniques, IEEE Proceedings E,* Vol. 136, No.6, Nov. 1989, pp. 575-580.

[11] Kuang-Hao Lin, et al, "Implementation of QR Decomposition for MIMO-OFDM Detection Systems," *Electronics, Circuit and Systems, 2008. ICECS 2008. 15th IEEE International Conference on,* Aug. 2008, pp. 57-60.

[12] Yin-Tsung Hwang, and Wei-Da Chen, "A Low Complexity Complex QR Factorization Design for Signal Detection in MIMO OFDM Systems," *Circuit and Systems, 2008. ISCAS 2008. IEEE International Symposium on,* 18-21, May 2008, pp.932-935.

[13] D. Patel, M. Shabany, and P. G. Gulak, "A Low-Complexity High-Speed QR Decomposition Implementation for MIMO Receivers," *Circuit and systems, 2009. ISCAS 2009. IEEE International Symposium on,* 24-27, May. 2009, pp. 33-36.

[14] J. E. Volder, "The CORDIC Trigonometric Computing Technique," *Electronic Computers, IRE Transactions on,* Vol. EC-8, Issue 3, Sept. 1959, pp. 330-334.

[15] P. K. Meher, et al, "50 Years of CORDIC: Algorithms, Architectures, and Applications," *Circuit and systems I, Regular papers, IEEE Transactions on,* Vol. 56, Issue 9, Sept. 2009, pp. 1893-1907.

[16] A. Paulraj, R. Nabar, D. Gore, "Introduction to Space-Time Wireless Communications," Cambridge, U.K.: Cambridge Univ. Press, 2003.

[17] Shu-hui Liu, et al, "A SC-FDE Scheme Adopting Frequency-Domain QR Decomposition in MIMO System," *Personal, Indoor and Mobile Radio Communications, 2009 IEEE 20th International Symposium on,* 13-16, Sept. 2009, pp. 261-265.

[18] Jae-Woong Han, and Young-Beom Jang, "A Residual Frequency Offset Synchronization Scheme Using a Simplified CORDIC Algorithm in OFDM Systems," *Communication Theory Workshop, 2009. AusCTW 2009. Australian,* 4-7 Feb. 2009, pp. 67-70.

[19] Shaoyun Wang, E. E. Swartzlander, "Merged CORDIC Algorithm," *Circuit and Systems, 1995. ISCAS `95., 1995 IEEE International Symposium on,* Vol. 3, May. 1995, pp. 1988-1991.

[20] B. Gisuthan, and T. Srikanthan, "Pipelining Flat CORDIC Based Trigonometric Function Generators," *Microelectronics Journal,* Vol. 33, No. 1, 2, Jan. 2002, pp. 77-89.

[21] S. Suchitra, et al, "Elimination of Sign Precomputation in Flat CORDIC," *Circuit and Systems, 2005. ISCAS 2005. IEEE International Symposium on,* Vol. 4, 23-26, May 2005, pp.3319-3322.

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