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Characteristics of Hafnium Silicate Films Deposited on Si by Atomic Layer Deposition Process

Jung-Chan Lee, Kwang-Sook Kim, Seok-Won Jeong, and Yonghan Roh†
School of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, Korea

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We investigated the effects of O_2 annealing (i.e., temperature and time) on the characteristics of hafnium silicate ($HfSi_xO_y$) films deposited on a Si substrate by atomic layer deposition process (ALD). We found that the post deposition annealing under oxidizing ambient causes the oxidation of residual Hf metal components, resulting in the improvement of electrical characteristics (e.g., hysteresis window and leakage current are decreased). In addition, we observed the annealing temperature is more important than the annealing time for post deposition annealing. Based on these observations, we suggest that post deposition annealing under oxidizing ambient is necessary to improve the electrical characteristics of $HfSi_xO_y$ films deposited by ALD. However, the annealing temperature has to be carefully controlled to minimize the regrowth of interfacial oxide, which degrades the value of equivalent oxide thickness.

Keywords: Metal-oxide-semiconductor capacitor, Atomic layer deposition, high-*k*, $HfSi_xO_y$, Interfacial layer regrowth, O_2 annealing

1. INTRODUCTION

Several candidates for future high-*k* gate oxides in metal-oxide-semiconductor (MOS) devices have been extensively studied by many research groups to overcome the problems such as the large leakage current caused by the direct tunneling through extremely thin SiO_2. Hafnium-based oxides are under intense investigation to replace conventional SiO_2 [1-3]. Recently, research efforts on high-*k* gate oxides have been focused on materials such as HfO_2, and its silicates due to their excellent electrical properties and high thermal stability in direct contact with Si [1-5]. HfO_2 has attracted considerable attention and has been considered as one of the most promising high-*k* candidates due to its high dielectric constant (~25), reasonable band alignment and relatively large band gap of 5.65 eV [1]. However, amorphous HfO_2 can easily crystallize at relatively low temperatures (~500℃): Crystallization not only increases the leakage current, but also deteriorates the interface of high-*k* oxide and Si substrate [1-5].

Low-temperature deposition and oxidation may be used in an attempt to prevent the crystallization of high-*k* oxide. It is, however, likely that the thermal cycles required in fabricating a transistor could cause high-*k* oxide to crystallize. Although the dielectric constant values *k* of $HfSi_xO_y$ (~13) is substantially lower than that of HfO_2, the structure of $HfSi_xO_y$ remains amorphous even after the high temperature heat treatment. Therefore, it is possible to minimize the leakage current through the grain boundaries in $HfSi_xO_y$ [2-5]. $HfSi_xO_y$ films have been deposited by pulsed laser deposition (PLD) [6], sputtering [3], E-beam evaporation [5], chemical vapor deposition [7] and atomic layer deposition (ALD) [8]. PLD and the sputtering process have some drawbacks such as poor step coverage and the damaging effect of the plasma on the channel region of the CMOS devices [9]. ALD is generally preferred for depositing very thin films because it is based on self-limiting surface reactions, which gives it attractive properties, like accurate and simple control of the film thickness and composition, sharp interfaces, highly conformal, uniform thin film growth, good reproducibility, and high film qualities at relatively low temperatures [10]. However, it has been reported that the residual metal components caused by insufficient oxidation during the ALD process may cause the C-V hysteresis and leakage current generation [11].

† Author to whom all correspondence should be addressed:
E-mail: yhroh@skku.edu

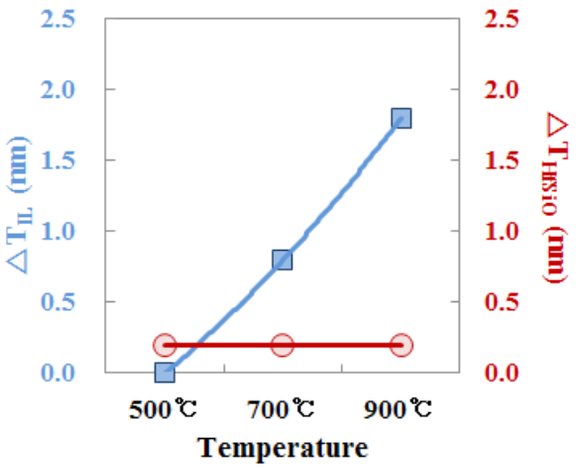

Fig. 1. Interfacial layer regrowth in terms of O_2 annealing temperature.

2. EXPERIMENTS

The $HfSi_xO_y$ films were deposited by the ALD method on the p-type Si substrate at 450℃. Prior to the deposition of $HfSi_xO_y$ film, the Si wafers were treated in a buffered HF (HF:H_2O = 1:100) solution to remove native oxide and contaminants. The precursors used in this work were $Hf[OC(CH_3)_2CH_2OCH_3]$ and $Si[OC(CH_3)_2CH_2OCH_3]$ at a ratio of 75:25% and remote-plasma oxygen with carrier N_2 gas. The remote-plasma oxidation has been demonstrated to reduce the amount of impurities, thus improving the electrical properties [11]. The processing parameters were set to obtain a final thickness of 35 Å. During the ALD process, the pressure of the reactor was kept at 100 Pa. After completing the deposition cycles, the $HfSi_xO_y$ films were annealed at various temperatures (i.e., 500℃, 700℃ and 900℃) using a rapid thermal processor (RTP) in O_2 ambient for 5 minutes. After O_2 annealing, Pd (1,000 Å) was thermally evaporated through a shadow mask to fabricate the MOS capacitors. The metal gate area was 2.4×10^{-4} cm^2. The effects of the annealing process were analyzed by high-resolution transmission electron microscopy (HR-TEM), X-ray photoelectron spectroscopy (XPS), capacitance versus applied voltage (*C-V*) and leakage current-density versus applied voltage (*J-V*) measurements. The capacitance was measured using a HP4275A LCR meter at the frequency of 1 MHz. The leakage current density characteristics were monitored using a HP4145B semiconductor parameter analyzer.

3. RESULTS AND DISCUSSION

Figure 1 shows regrowth of interfacial layer (IL) and $HfSi_xO_y$ following O_2 annealing. Thicknesses were measured by HR-TEM. Initial thicknesses of IL and $HfSi_xO_y$ were 1.6 nm and 2.4 nm, respectively. The data shown in Fig. 1 were obtained from the samples subjected to the post deposition annealing using RTP in O_2 ambient for 5 minutes at 500℃, 700℃ and 900℃, respectively.

While the IL thickness increased as the annealing temperature increased, the thickness of the $HfSi_xO_y$ layer (with the exception of IL between Si substrate and $HfSi_xO_y$ layer) shows no visible change after annealing at high temperature. The $HfSi_xO_y$ film is completely amorphous at 500℃ and 700℃. In contrast, in the $HfSi_xO_y$ film with 900℃ annealing, we observed crystallized portions. Recently, it was reported that localized crystallization occurs after a high temperature annealing [12-14].

In order to examine the structural change associated with the annealing temperature, we measured the XPS spectra of the as-deposited $HfSi_xO_y$ film and annealed $HfSi_xO_y$ (Fig. 2). Figure 2 exhibits the (a) Hf 4*f* and (b) Si 2*p* spectra observed from $HfSi_xO_y$ layer annealed with variable temperature by RTP. Figure 2(a) shows the Hf 4*f*(7/2) peak at 19.1 eV, separated by 1.7 eV from the Hf 4*f*(5/2) peak at 17.4 eV, which is attributed to Hf bound to oxygen [12]. From Si 2*p* peak in the Fig. 2(b), we observed that the higher the temperature, the larger the silicate peak associated with Si-O bonding [15]. On the other hand, as shown in Fig. 2(a), in the Hf 4*f* peak, the identified shoulders that appear in the lower binding energy are considered to be caused by an unoxidized Hf-Si bond. However, as the annealing temperature increased, the residual Hf-Si peaks disappeared. This implies that the metallic Hf components are oxidized by diffusion of oxygen from the surface into the Si substrate, in the oxygen gas annealing [12]. This is also associated with an increase in the IL thickness between the Si substrate and $HfSi_xO_y$ layer. The physical changes in the IL have an effect on the electrical properties.

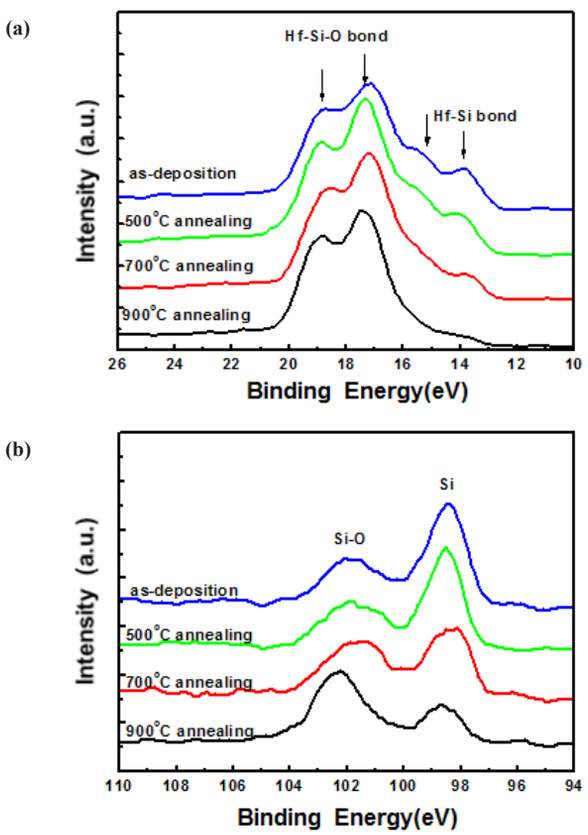

Fig. 2. X-ray photoelectron spectroscopy spectra at (a) Hf 4f and (b) Si 2p spectra annealed by rapid thermal processor at 500℃, 700℃ and 900℃, respectively, for 5 minutes in O_2 ambient.

Figure 3 shows the capacitance versus applied voltage (*C-V*) characteristics of the p-Si/$HfSi_xO_y$/Pd capacitor according to annealing temperature. From Fig. 3, we find that the accumulation capacitance decreases as the annealing temperature increase. This phenomenon can be explained by the increase in the IL thickness due to high temperature annealing, as shown in Fig. 2. The as-deposited $HfSi_xO_y$ films exhibit a large hysteresis of around 0.4 V due to the defects caused by partial oxidization (Hf-Si bonding states). The hysteresis voltages were reduced by a higher annealing temperature. These experimental results indicate that the charges trapped in the film decreased with O_2 annealing.

Figure 4 shows the leakage current density characteristics of

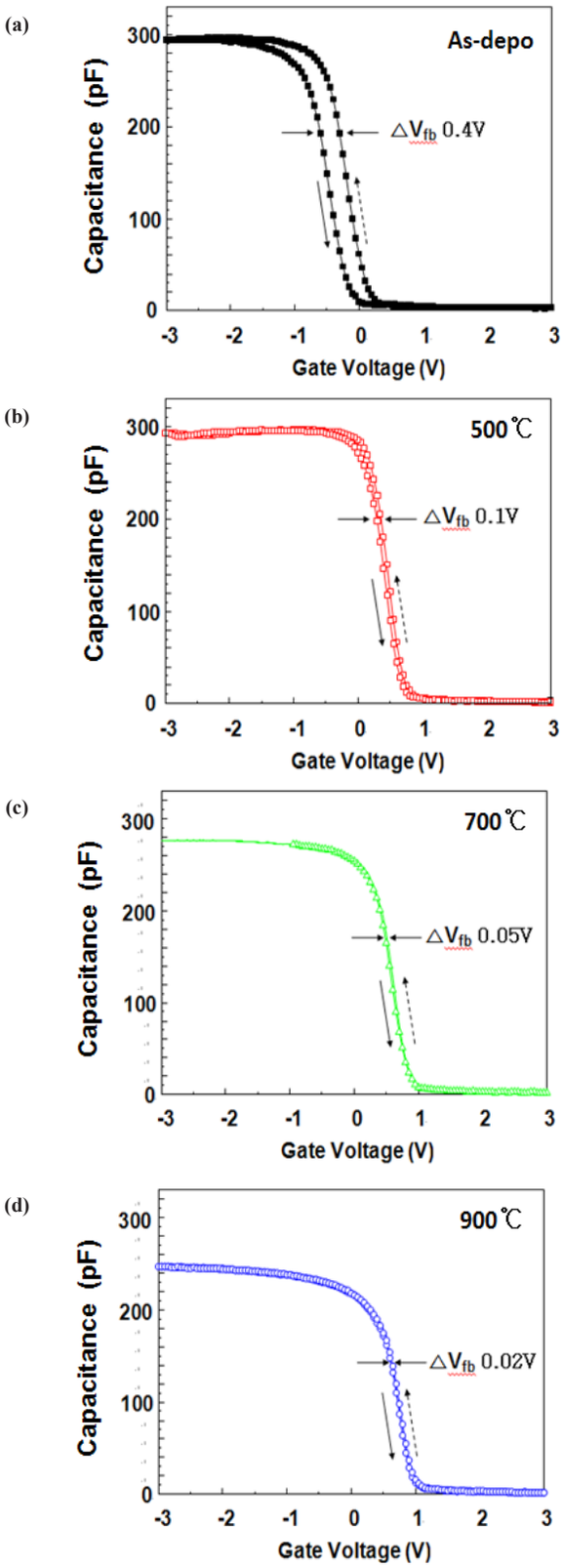

Fig. 3. High frequency capacitance (C-V) characteristics of p-Si/ $HfSi_xO_y$/Pd capacitors annealed by rapid thermal processor at 500℃, 700℃ and 900℃, respectively, for 5 minutes in O_2 ambient.

the p-Si/$HfSi_xO_y$/Pd capacitor according to annealing temperature. The leakage current is dependent on annealing temperature.

For example, we obtained the lowest value of leakage current density from an annealed sample at 900℃ due to the increase in the IL thickness. The leakage current density of $HfSi_xO_y$ film annealed at 500℃ is similar to that of the as-deposited sample. Moreover, both samples have nearly the same capacitance value.

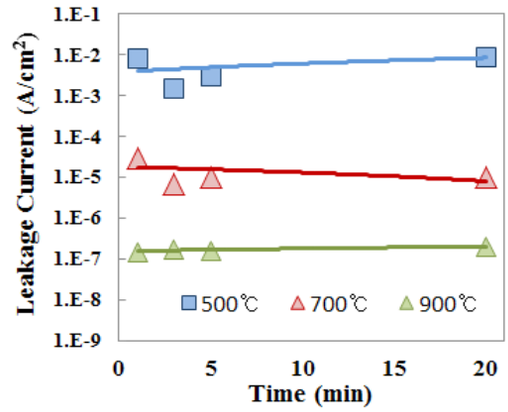

Fig. 4. Leakage current density (J-V) characteristics of p-Si/$HfSi_xO_y$/Pd capacitors annealed by rapid thermal processor at 500℃, 700℃ and 900℃, respectively, for 5 minutes in O_2 ambient.

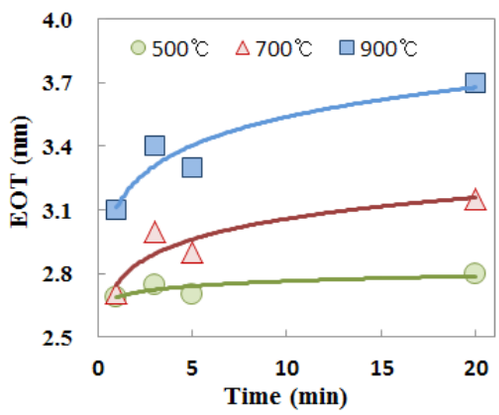

Fig. 5. Equivalent oxide thickness of p-Si/$HfSi_xO_y$/Pd capacitors annealed by rapid thermal processor at 500℃, 700℃ and 900℃, respectively, for 5 minutes in O_2 ambient.

Figure 5 shows equivalent oxide thickness (EOT) characteristics of p-Si/$HfSi_xO_y$/Pd capacitor according to annealing temperature and time. EOT was dependent on annealing temperature.

EOT and the leakage current density of the $HfSi_xO_y$ film is less dependent of the post deposition annealing time, as shown in Figs. 4 and 5. As the annealing time increases, both the EOT and leakage current density show only a little change. This result indicates that the relationship between the electrical characteristics and annealing condition is more strongly dependent on the annealing temperature than the annealing time.

4. CONCLUSIONS

We have studied the effect of annealing on $HfSi_xO_y$ film deposited by ALD. We found that post deposition annealing causes oxidation of residual Hf metal components, resulting in an improvement in the hysteresis window and leakage current density. These experimental results indicate that the post deposition annealing improves the electrical and physical characteristics (e.g., hysteresis window and leakage current were decreased). In ad-

dition, we found that the role of annealing temperature is more important than that of annealing time in post deposition annealing. However, EOT increased as increasing the temperature due to IL regrowth. Based on the current observation, the annealing temperature has to be carefully controlled to minimize the growth of interfacial oxide, which degrades the value of the EOT.

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