Journal of the Korean Institute of Illuminating and Electrical Installation Engineers (2011) 25(3) : 40~49
DOI : 10.5207/JIEIE.2011.25.3.040

Optimal Design of a DC-DC Converter for Photovoltaic Generation

Soon-Kurl Kwon*

Abstract

This paper presents novel circuit topology of half-bridge soft-switching PWM inverter type DC-DC high power converter for DC bus feeding power plants. The proposed DC-DC power converter is composed of a typical voltage source-fed, half-bridge high frequency PWM inverter with a high frequency planar transformer link PWM control scheme and parallel capacitive lossless snubbers. The operating principle of the new DC-DC converter treated here is described by using switching mode-equivalent circuits, together with its unique features. All the active power switches in the half-bridge arms and input DC bus lines can achieve ZCS turn-on and ZVS turn-off commutation transitions. The total turn-off switching losses of the power switches can be significantly reduced. As a result, high switching frequency IGBTs can actually be selected in the frequency range of 40[kHz] under the principle of soft-switching. The performance evaluations of the experimental setup are illustrated practically.

Key Words : Photovoltaic DC-DC Power Converter; High Frequency Transformer Link; Snubbers; Soft-Switching PWM

1. Introduction

Recently, DC-DC converters using phase - shift modulation in the secondary side of high frequency transformer-saturable inductor switch assisted ZVS-PWM full-bridge high-frequency converter was proposed [1-3]. These DC-DC power converter circuit topologies are suitable for handling high output power more than several kW, especially for high or medium voltage and low current DC applications as new energy-related power supplies. However, secondary magnetic switches or secondary side semiconductor switching devices as active power rectifiers in these converter circuit topologies may cause large conduction loss when these power circuit topologies are adopted for low voltage and large current applications.

Therefore, for the low voltage and large current application power supplies, a soft-switching DC-DC power converter with active switches in the primary

* Main author : Electrical Engineering Department of Kyungnam University
Tel : +82-55-249-2633, Fax : +82-55-242-2683
E-mail : soonkurl@kyungnam.ac.kr
Date of submit : 2011. 2. 22
First assessment : 2011. 3. 1
Completion of assessment : 2011. 3. 21

side of a high frequency transformer is considered to be more suitable and acceptable. As a circuit topology to meet this requirement for PV in the industry, the author developed a novel circuit topology of voltage source full-bridge soft-switching PWM inverter with a phase shift PWM scheme, in which all the active switches can achieve ZCS turn-on and ZVS turn-off commutation operations [4].

This paper presents a novel circuit topology of a voltage source half-bridge soft-switching PWM high frequency inverter type DC-DC power converter and low side active edge resonant snubbers. Under the newly-proposed high frequency inverter link, DC-DC power converter circuit, all the active switches in the half-bridge arm and DC bus lines can actively achieve ZCS turn-on and ZVS turn-off commutation operations.

The steady-state operating principle of the proposed soft-switching PWM DC-DC power converter is described along with its remarkable features. The experimental operation results of this new type of soft-switching PWM DC-DC power converter using IGBT power modules are illustrated including power loss analysis as compared with that of the hard-switching PWM DC-DC power converter. The practical effectiveness of the proposed high frequency transformer link DC-DC power converter acceptable and suitable for high power applications, which is designed for low voltage and large current output, is actually proved on the basis of experimental data. Although the conduction power loss of the additional switches may increase the total power loss slightly, the total turn-off switching loss of half-bridge type PWM inverter can be significantly decreased with the optimum aid of DC bus line series switches and the lossless snubbing capacitors.

2. New soft-switching DC-DC converter

Figure 1 shows the proposed voltage source soft-switching PWM DC-DC converter circuit using a novel topology of half-bridge soft-switching PWM inverter with a high frequency planar transformer link. This DC-DC converter is composed of a typical divided voltage source modified type half-bridge inverter with an active PWM switch $Q_3(S_3/D_3)$ in positive DC bus line, an active PWM switch $Q_4(S_4/D_4)$ in negative DC bus line, and two lossless snubbing capacitors, C_1 and C_2, and two diodes, D_5 and D_6. Two center points of the two capacitors (C_1, C_2) in parallel with two diodes (D_5, D_6) are connected to a mid point of two voltage sources (E_1, E_2) and a terminal of primary winding of high frequency transformer. The voltages represented by E_1 and E_2, and capacitance of C_1 and C_2 are designed so as to be equal ($E_1=E_2=E$, $C_1=C_2=C$). The main active switches (Q_1, Q_2) can periodically be turned on and off in the same pulse pattern with a certain dead-time as a conventional half-bridge type hard-switching PWM inverter.

Under the proposed DC-DC converter, the switches (Q_1, Q_2) in the half-bridge type inverter arms can perform ZVS turn-off transition due to the presence of the active PWM switches (Q_3 or Q_4), which are turned off, and the snubbing capacitors (C_1 or C_2) are completely discharged before the active switches (Q_1 or Q_2) in half-bridge type inverter arms are turned off. In addition, all the inverter switches can also perform ZCS at a turn-on mode transition with the aid of inductance (L_S) as a primary side-lumped parasitic leakage inductance of high frequency transformer HF-T.

As for the active PWM switches (Q_3 - Q_4) in series with the DC bus line side, the PWM

controlled switches (Q_3, Q_4) can achieve ZVS at a turn-off mode transition due to the lossless snubbing capacitors (C_1 or C_2). These active PWM switches (Q_3, Q_4) can also achieve ZVS/ZCS at a turn-on mode transition due to the lossless snubbing capacitors (C_1, C_2), which have been charged up to the same voltage as the half voltage (E_1 or E_2) of DC power bus line voltage source by the energy storage in the leakage inductance (L_S) after the half-bridge type inverter switches (Q_1, Q_2) are turned off completely. With the proposed soft-switching PWM DC-DC converter, although the conduction power loss of the additional switches (Q_3 - Q_4) may increases the total power loss slightly, the total turn-off switching loss of half-bridge type PWM high frequency inverter can be significantly decreased with the optimum aid of DC bus line series switches (Q_3 - Q_4) and the lossless snubbing capacitors (C_1 - C_2).

Figures 1 (b) and (c) depict the modified circuit topologies of the proposed PWM DC-DC power converter with a high frequency transformer link.

3. Principle of operation

3.1 Gate voltage pulse timing sequences

Figure 2 shows the specified timing pattern sequences of switching gate driving pulses. The gate voltage pulse signals for the inverter switches (Q_1, Q_2) in voltage source half-bridge inverter arms are the same as PWM signal sequences of conventional half-bridge inverters. Regarding the turn-on gate voltage pulse signals to the DC bus line side series switches (Q_3, Q_4) the signals are applied to Q_3 and Q_4 at the same timing as the turn-on signals to Q_1 and Q_2, respectively. As for the turn-off signals to Q_3 and Q_4, the signals are delivered to Q_3 and Q_4 before the predetermined length (t_d) of time on the basis of the time when the turn-off signals are applied to Q_1 or Q_2. In other words, the turn-off pulse signals are applied to Q_1 and Q_2 after the turn-off gate signals applied to Q_3 and Q_4 by time t_d.

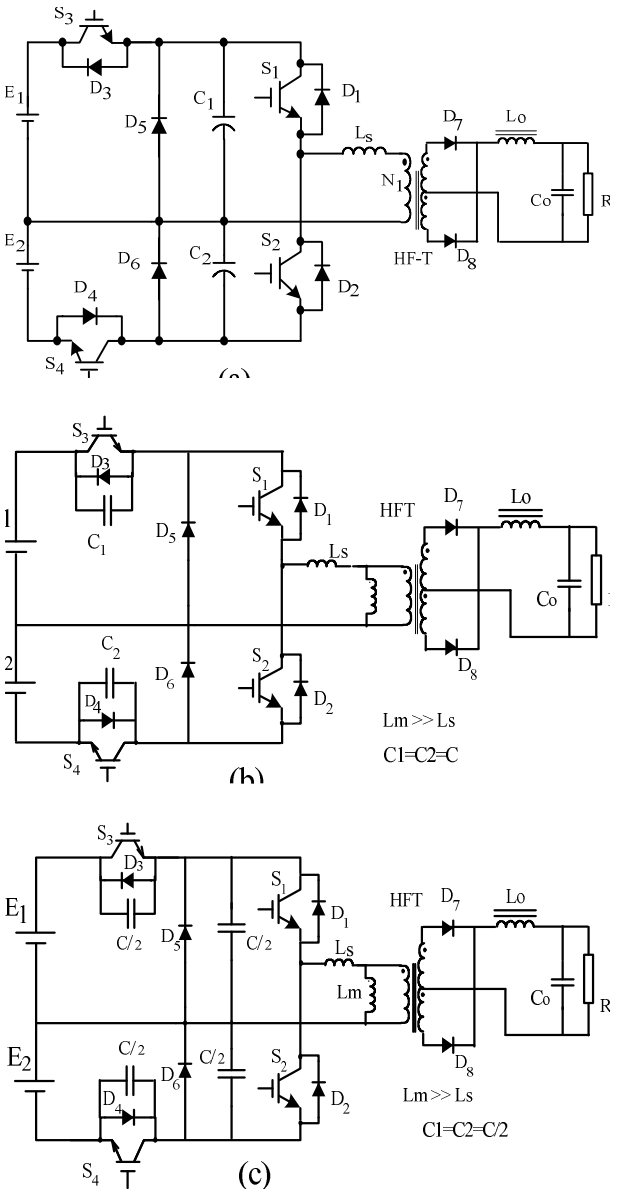


Fig. 1. Proposed half-bridge soft-switching PWM DC-DC power converter and its modified versions

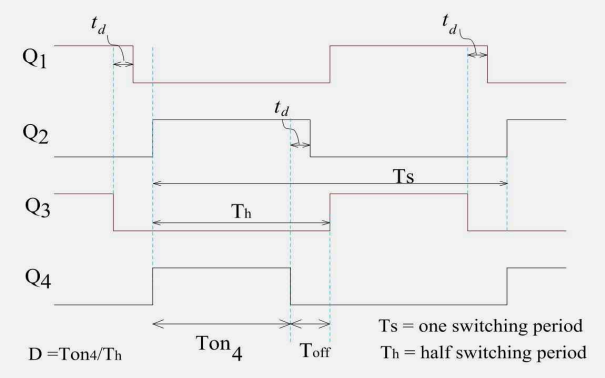


Fig. 2. Timing Pattern sequences of switching gate driving pulses

3.2 Duty cycle control scheme

The proposed DC-DC converter for PV uses the current feedback control algorithm. The output current control signal is obtained from a secondary current sensing of a planar high frequency transformer; thereafter it is compared with the current setting reference signal, and this can be done through an error amplifier. Hence this process, output current PI controller pulse modulator, generates the PWM switching signal of the DC-DC power converter treated here, in which the frequency of gate pulse remains constant, while the pulse width only is varied.

C. Switching operation modes and equivalent circuits

Figure 3 illustrates the relevant operating waveforms during a complete switching period for the pattern of gate drive pulse timing sequences shown in Figure 2. The switching operation modes of this DC-DC power converter are divided into twelve operation modes from mode 1 to mode 12 in accordance with operating timing sequences, from t_0 to t_{11}. The operation principle is described in the following. The equivalent circuits corresponding to respective operation mode are shown in Figure 4.

1) Mode 1 ($-t_0$): Before time t_0, switches Q_1 and Q_3

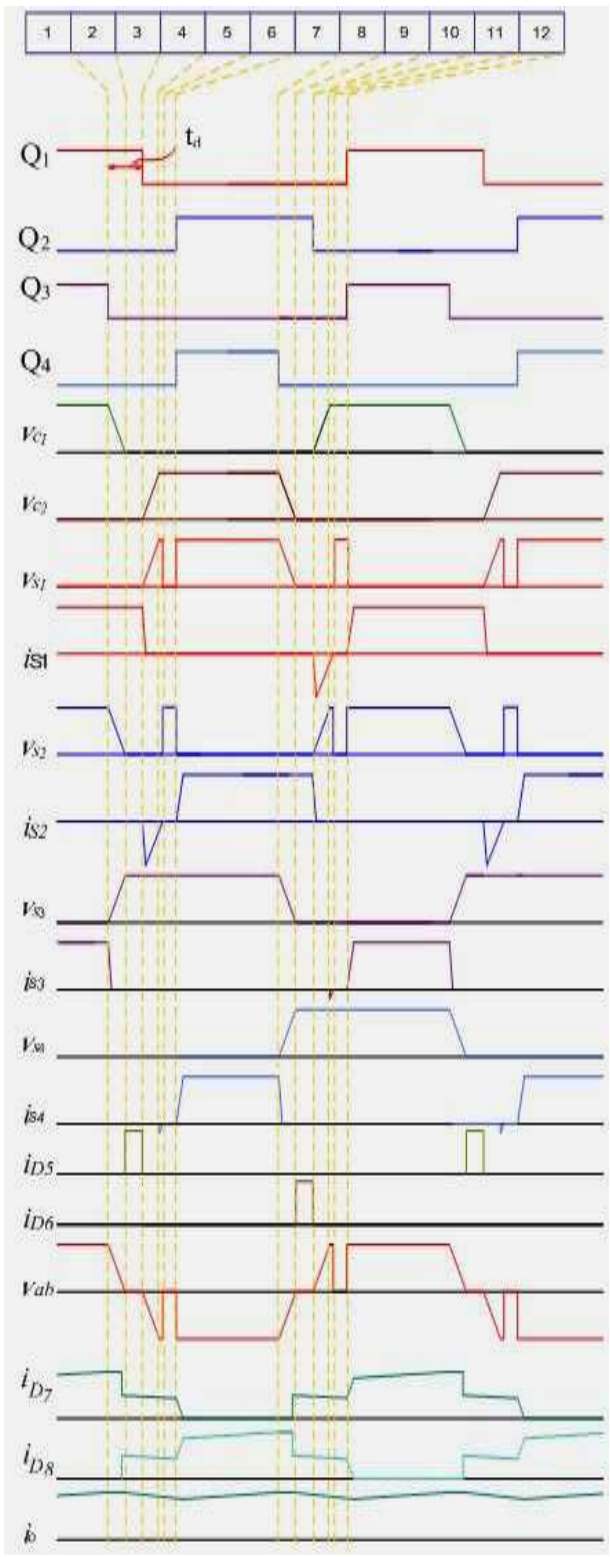


Fig. 3. Operating waveforms during one switching period

are turned on. At this time, i_{t1} flows through the primary winding of high frequency transformer HF-T. i_{s1} flows through Q_1, and i_{s3} flows through Q_3. In this period, all currents (i_{t1}, i_{s1} and i_{s3}) are equal, and the voltage (v_{C1}) across C_1 is the same as the DC bus line voltage E_1.

2) Mode 2 (t_0 - t_1): At time t_0, the turn-off pulse signal is applied to Q_3. At this time, the high side series switch Q_3 in the DC bus line can be turned off with ZVS because the current i_{s3} through Q_3 is immediately cut off due to the lossless snubbing capacitor C_1. After time t_0, the voltage v_{C1} across the capacitor C_1 discharges constantly toward zero voltage from E_1=E. At this time, the voltage v_{C1} across the lossless snubber capacitor C_1 is estimated by,

$$v_{C1}(t) = E - (i_{t1}/C)t \quad (1)$$

where, i_{t1} is a primary current of a high frequency transformer. From equation (1) until this voltage v_{C1} becomes zero, the discharging time (t_x) of the capacitor C_1 is given by:

$$t_x = CE/i_{t1} \quad (2)$$

From equation (2), the larger the current i_{t1} though the primary winding of high frequency transformer HF-T, the shorter the discharging time for capacitor C_1. On the other hand, the smaller the current i_{t1}, the longer the discharging time t_x. Under this newly-developed DC-DC power converter circuit [see Figure 1 (a)], the delay time t_d indicated in Figure 2 is designed so as to be longer than the time calculated from equation (2) under the condition of the maximum i_{t1} or the maximum output current. In this case, the switches Q_1 or Q_2 can achieve ZVS turn-off transition completely. To enlarge the complete ZVS operation range at the turn-off commutation for the switches Q_1 or Q_{2i}, the delay time t_d should be varied according to the value of current i_{t1}.

3) Mode 3 (t1-t_2): At time t1, the voltage v_{C1} becomes zero. In the interval from t_1 to t_2, the diode D_5 is turned on and the current i_{t1} through the high frequency transformer primary winding flows through the circulation loop; $L_S \rightarrow D_5 \rightarrow S_1 \rightarrow L_S$.

4) Mode 4 (t_2-t_3): At time t_2, the turn-off gate pulse signal (see Figure 2) is applied to Q_1. At this time, the switch Q_1 can be turned off with ZVS because the voltage v_{C2} across C_2 was already zero during the second half of the operation cycle, and the diodes D_2 of Q_2 are immediately turned on. After that, the capacitor C_2 is charged up to the same voltage as the DC bus line voltage E_2.

At this mode, in order to achieve ZVS, the energy stored in the leakage inductance has to be large enough to charge and discharge divided capacitance; neglecting the transformer winding capacitance, the energy stored in the leakage inductance has to satisfy the condition that the capacitor C_2 is charged up to just the same voltage as the DC bus line voltage E_2, which can be estimated by equation (3).

$$(1/2)CE^2 = (1/2)L_S(i_{t1})^2 \quad (3)$$

where C_1=C_2=C

However, as described below in mode 6, circuit parameters should be designed to meet the condition of:

$$(1/2)CE^2 \leqq (1/2)L_S(i_{t1})^2$$

in order to achieve ZVS turn-on transition of Q_4.

5) Mode 5 (t_3-t_4): Under the condition of $(1/2)CE^2 < (1/2)L_1(i_{t1})_2$, after the voltage v_{C2} reaches the DC

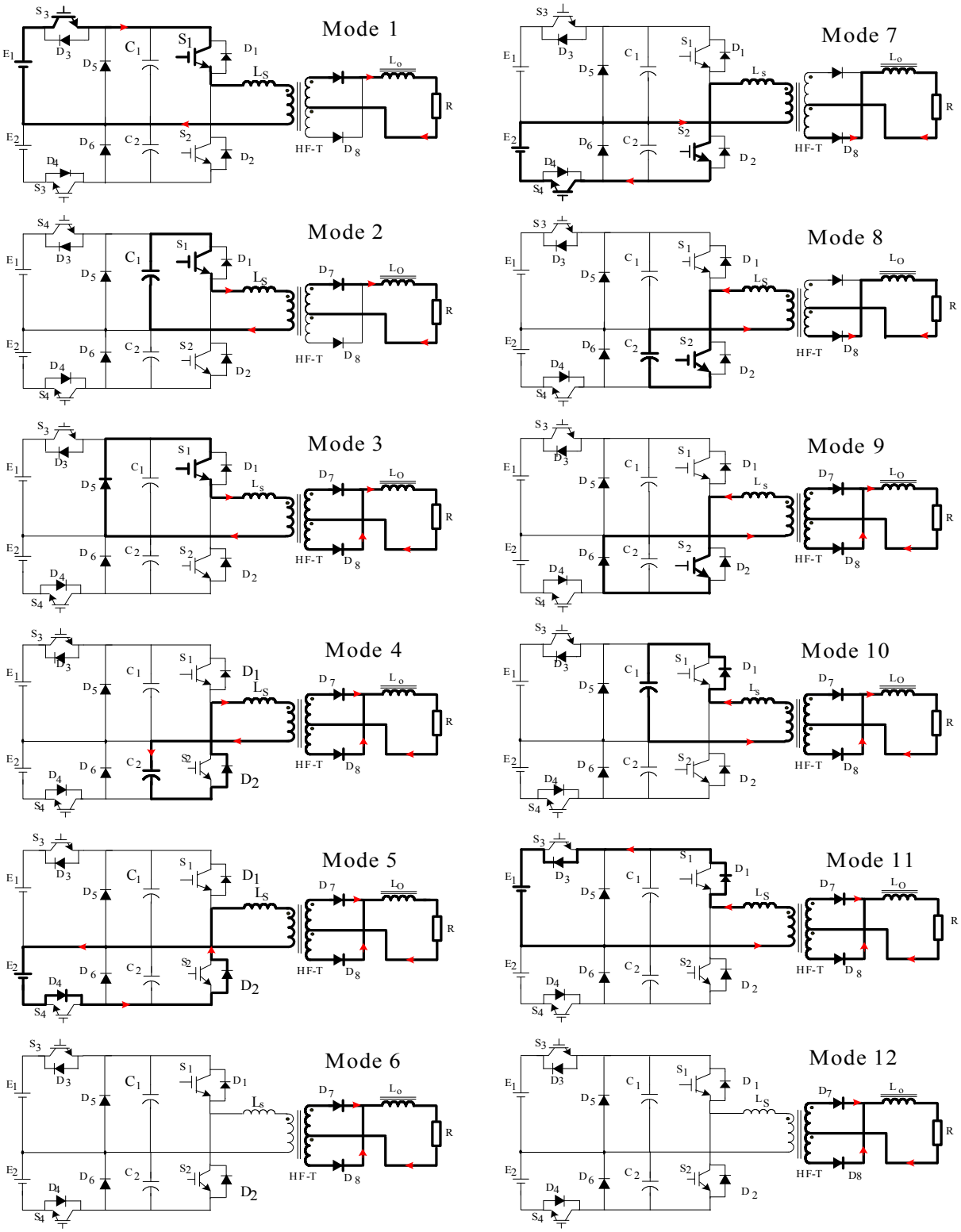


Fig. 4. Switch-mode transition states and their corresponding equivalent circuits

bus line voltage E_2, the voltage v_{C2} across the snubber capacitor C_2 is clamped to DC bus line voltage E_2 because diode D_4 of Q_4 is turned on and the energy stored in the inductor with leakage inductance L_S is back to DC bus line voltage source E_2.

6) Mode 6 (t_4-t_5): In this mode, all operations are stopped in the primary circuit of the high frequency transformer.

7) Mode 7 (t_5-t_6): At time t_5, the turn-on gate pulse signals are applied to the switches Q_2 and Q_4. At this time, the switch Q_2 can be turned on with ZCS due to the primary-side lumped parasitic inductance L_S of the high frequency transformer. Furthermore, the series switch Q_4 in the bus line achieves a complete soft-switching ZVS/ZCS at turn-on transition because the voltage v_{C2} is the same voltage as the DC power bus line voltage E_2.

Thereafter, the operation processes for Q_2 and Q_4 are the same as those for aforementioned Q_1 and Q_3, and the operation processes for Q_1, Q_3 and Q_2, Q_4 will be repeated in sequence continuously from mode 8 to mode 12 as in Figure 4, the switching operation modes and equivalent circuits during the second half of the cycle period.

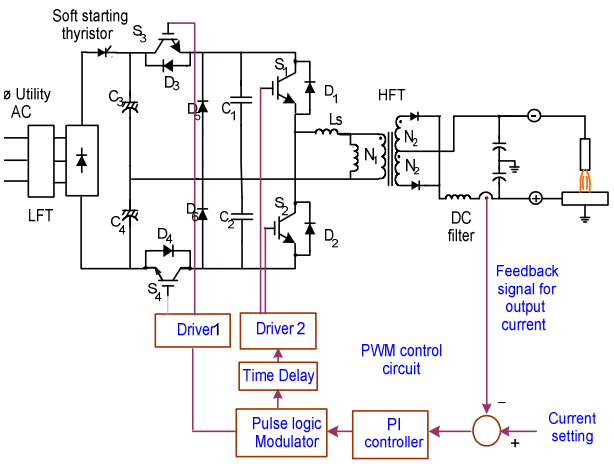


Fig. 5. Experimental circuit

4. Experimental results and discussion

4.1 Total system implementations

The experimental DC-DC converter circuit setup treated here is shown in Figure 5. In the DC-DC converter setup implementation, the maximum output voltage and current are designed for 36[V] and 400[A], respectively. The design specifications and circuit parameters are described in Table 1.

The maximum DC output power of this experimental power supply setup is designed for 14.4[kW].

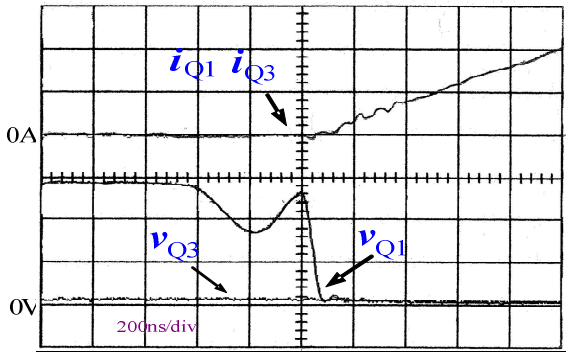
The IGBT power modules are mounted on the heat sink and connected by the printed circuit board in which the capacitors C_1 and C_2 are mounted on PCB, and the capacitors C_3 and C_4 are directly connected to the output of a three phase rectifier. Connecting IGBTs and capacitor C_1, C_2, C_3 and C_4 by the printed circuit board enables to minimize the stray line inductance with optimum connections among IGBTs, C_1, C_2, C_3 and C_4. Actually, the minimum leakage inductance of the high frequency transformer is particularly important on this new soft-switching PWM DC-DC converter, because spike voltage across the collector and emitter of IGBTs easily appears at the turn-off transition if there is stray wiring inductance between snubbing capacitors and the IGBT switches. The control circuit for newly-developed circuits can be implemented easily by modifying the conventional PWM signal processing circuit using a common PWM control IC (μPC494) with dual alternating output switches and dead time control.

4.2 Measured voltage and current switching waveforms

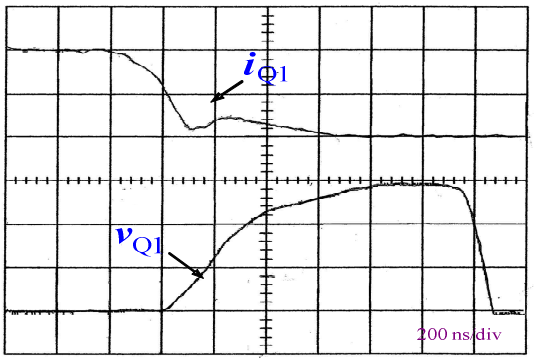
The switching operating waveforms for voltage and current when the switch Q_1 is turned on and off are shown in Figures 6 (a) and (b). Observing these operating waveforms, switch Q_1 is turned on with ZCS and also turned off with ZVS. The switching waveforms for voltage and current when switch Q_3 is turned on and off are shown respectively in Figures 6 (a) and (c). Observing the operating waveforms, switch Q_3 is turned on with ZVS/ZCS and is turned off with ZVS. However, at the turn-off transition for Q_1 and Q_3, only a few switching power losses still exist due to the inherent tail current characteristic of IGBTs. Figure 7 represents the assembled component appearance on the printed circuit board (PCB) in the primary main circuit.

Table 1. Design specifications and circuit parameters

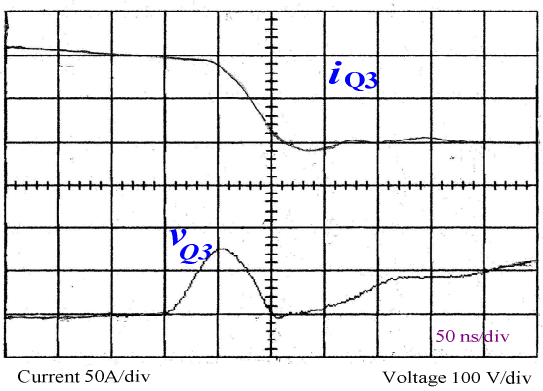
Item	Symbol	Value
Utility AC Input Voltage		AC200[V]
Inverter Switching Frequency	f_s	40[kHz]
Switching Period	T_s	25[μs]
Primary Side-Lumped Leakage Inductance of High Frequency Transformer	L_s	2[μH]
Capacitance of Quasi Resonant Capacitors	C_1, C_2	0.235[μF]
Capacitance of DC Smoothing Filter Capacitor	C_3, C_4	2200[μF]
Inductance of DC Reactor in Load Side	L_o	60[μH]
Equivalent Load Resistance (Stable Arc Welding Load)	R	0.09[Ω]
Maximum Load Current	I_o	300[A]
Turns Ratio of HFT	N_1:N_2:N_3	4:1:1
Remarks: Lm >> L_s		



(a) Turn on switching waveforms for Q1,Q3



(b) Turn off switching waveforms for the switch Q1



(c) Turn off switching waveforms for the switch Q3

Fig. 6. Switching voltage and current waveforms for active power switches Q_1 and Q_3

4.3 Comparative results of power loss analysis

In power loss analysis and evaluations shown in Figure 8, the total power loss of all the switches, including Q_3 and Q_4, in the newly-developed DC-DC power converter circuit [see Figure 1 (a)] is

compared with those of all the switches in a conventional hard-switching PWM half-bridge inverter type DC-DC power converter. When the switching frequency is 10[kHz], the total power losses for both inverter type high frequency DC-DC power converter circuits are almost equal tp each other. And, the switching frequency of a high frequency inverter power stage using IGBTs is designed for 40[kHz] more. The more the switching frequency of a DC-DC converter increases, the more this newly-developed DC-DC power converter circuit has remarkable advantages in terms of the power conversion efficiency and power density compared to the conventional hard-switching inverter type DC-DC power converter.

If the switching frequency or operating frequency is designed for 40[kHz], the total power loss for the switches in the developed DC-DC power converter (see Figure 1) is 225[W] and that of the conventional hard-switching PWM inverter is 435[W]. Furthermore, the snubber circuit is required for the conventional hard-switching half-bridge PWM DC-DC power converter circuit. Therefore, the total power loss for a conventional hard-switching converter circuit, including the power loss of the snubber circuit, can be estimated as approximately 635W, which is three times more than the total power loss of the newly-developed DC-DC power converter.

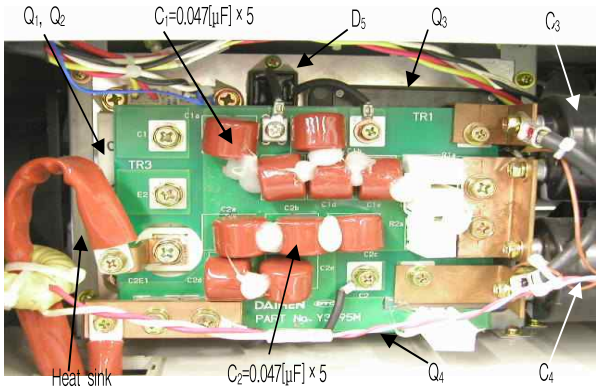


Fig. 7. Assembled component appearance in high frequency transformer primary side circuit

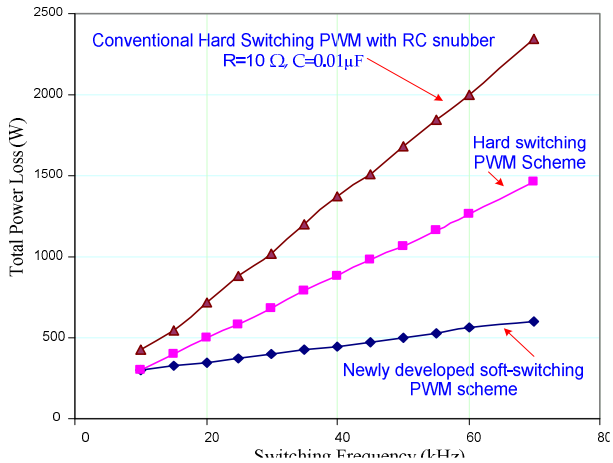


Fig. 8. Comparative power loss analysis between the proposed and conventional hard-switching PWM DC-DC converters

5. Conclusions

In this paper, the novel circuit topology of voltage source modified half-bridge soft-switching PWM DC-DC power converter with a high frequency planar transformer link was presented. The operating principle, switching pattern and control strategy of the half-bridge soft-switching PWM DC-DC power converter designed for inverter switching frequency of 40[kHz], 36[V] and 200[A] output specifications were illustrated and discussed for low-voltage and large current output applications such as telecommunication and automotive applications as well as arc welding power supply applications. The power loss analysis of the proposed soft-switching DC-DC power converter was discussed and evaluated compared to the hard-switching PWM DC-DC power converter with a high frequency transformer link. The practical effectiveness of the proposed DC-DC power converter operation under the soft-switching

PWM scheme was actually proved from a practical point of view, and the high efficiency and power density of this converter could be achieved on the basis of experimental results for low-voltage and large current power supplies.

Under the simple circuit, which has two additional power semiconductor switching devices and two passive circuit components to the typical half-bridge inverter circuit, all the active switching devices incorporated into half-bridge inverter arms and DC bus line input achieve ZVS turn-off and ZCS turn-on commutation. When the switching frequency of a high frequency inverter using IGBTs is selected more than approximately 20[kHz], the more the switching frequency of the inverter increases, the more this proposed PWM DC-DC power converter has a remarkable advantage in terms of the power conversion efficiency and power density compared to the conventional hard-switching inverter type DC-DC power converter.

The downsizing and light-weighted power supply using this newly-developed soft-switching DC-DC power converter circuit was developed and put into the practical market in the PV system industry.

This work is supported by the Kyungnam University Research Fund, 2009

Biography

Soon-Kurl Kwon

He received a B.E. degree in Electrical Engineering from Young-Nam University, Daegu, Korea, and received an M.S. degree in Electrical Engineering from Busan National University, Busan, Korea, He received a Ph.D. (Dr-Eng) in Electrical Engineering from Young-Nam University, Daegu, Korea. He joined the Electrical Engineering Department of Kyungnam University, Masan, Korea in 1983 and has served as a professor. He was a visiting professor of VPEC in VPI & SU, USA in 1997 and 2007. His research interests include application developments of power electronics circuits and systems. He is a member of the KIEE and KIPE.