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A Novel Filter Design for Output LC Filters of PWM Inverters

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Abstract

The cutoff frequency of the output *LC* filters of PWM inverters limits the control bandwidth of the converter system while it attenuates voltage ripples that are caused by inverter switching activities. For a selected cutoff frequency of an output *LC* filter, an infinite number of L-C combinations is possible. This paper analyses the characteristics of output *LC* filters for PWM inverters terms of the L-C combinations. Practical circuit conditions such as no-loads, full resistive-loads, and inductive-load conditions are considered in the analysis. This paper proposes a *LC* filter design method for PWM inverters considering both the voltage dynamics and the inverter stack size. An experimental PWM inverter system based on the proposed output *LC* filter design guideline is built and tested.

Key Words: Cut-off frequency, Inverter size, L-C combination, Output *LC* filter, PWM inverter

I. INTRODUCTION

PWM inverters are widely used in various applications, such as Adjustable Speed Drives (ASD), Active Power Filters (APF), Dynamic Voltage Restorers (DVR), Uninterruptible Power Supplies (UPS), and Distribution Static Compensators (DSTATCOM) [1]–[5].

First-order passive *L*-type filters are normally used on the AC side of PWM inverters when the output AC current is the main control target. The main purpose the of *L*-type filter is to attenuate the current ripples that result from inverter switching [6], [7]. This type of filter has a restriction in low- switching-frequency applications of high-power PWM inverters due to the inevitable large filter size.

An alternative filter configuration is the third-order *LCL*-type filter, which can achieve a reduced level of current harmonics with less total filter inductance at lower switching frequencies. On the other hand, *LCL*-type filters can cause steady-state and transient problems with the output current due to resonance [13]–[19].

Second-order passive *LC*-type filters have been widely used on the AC terminals of PWM inverters when the output voltages are the main control targets [20], [21]. The main purpose of the *LC* filters is to attenuate the voltage ripple that stems from inverter switching.

The output voltage on the *LC* filter capacitor is controlled by switching the PWM inverter, where the *LC* filters introduce a time delay and cause resonance in the output AC voltage. Thus various approaches have investigated regulating the output voltage across the *LC* filter capacitor. Rotational frame DQ controllers are becoming the industry standard for three-phase discrete control systems in these applications [20]–[24]. A deadbeat control method was adopted for the high-performance vector control system of an AC motor using a low-switching-frequency (2 kHz) PWM inverter with an output *LC* filter [25]. Excellent high-dynamics of the output voltage have been realized using the proposed deadbeat control algorithm. Together with the deadbeat controller, a neural network-based estimation unit was proposed with low computational demand to estimate the interfacing parameters and the grid voltage vector simultaneously in real time [23]. The proposed control algorithm was stable and generated minimal low-order harmonics even with a 60% mismatch in the filter inductance. Resonant filters have been invented that are capable of sensing major low-order harmonics across the filter capacitor voltage. The low order harmonics are offset by each harmonic rotational frame DQ controller separately to obtain the sinusoidal load voltages in DVR systems [24].

In addition to the voltage distortion of *LC* filters during steady-state operation, very large voltage overshoot can occur at the filter capacitor when inverters respond in a step-wise manner to the transient state [22], [23]. The voltage overshoot can be dampened out by generating the proper damping voltage with a voltage controller. Sensing the capacitor current of the output *LC* filter in a feedback control system provides good dynamics as regards the sinusoidal output voltage across the filter capacitor [26]. The capacitor current is fed forward to an inverter voltage controller to obtain high dynamics of the capacitor voltage [21]. This method achieves maximum

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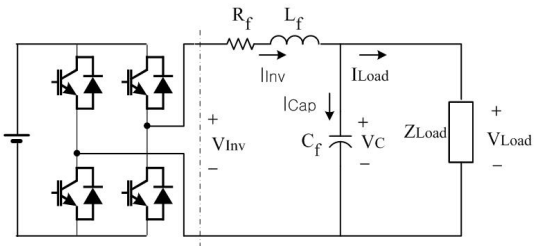


Fig. 1. Single-phase equivalent circuit of a PWM inverter system.

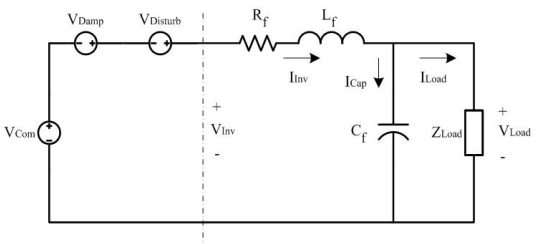


Fig. 2. Single-phase equivalent circuit of properly controlled inverter system.

control bandwidth up to the output filter cutoff frequency without using nested control loops. Similar active damping schemes have been accomplished by sensing and offsetting the harmonics of the filter the capacitor voltage [27].

The aforementioned voltage controllers can therefore attenuate the lower-order voltage harmonics on the filter capacitors. However, the higher-order voltage harmonics that result from PWM switching can be attenuated not by a controller but by a passive *LC* filter.

The attenuation effect of *LC* filters can be increased by decreasing the filter cut-off frequency against the switching frequency of inverters according to -40log (f_{sw}/f_{cutoff}) [dB]. However, the filter cut-off frequency limits the control bandwidth of inverter systems. Increasing the control bandwidth is important not only for fast operation of the inverter system but also for precise voltage compensation without a phase delay at higher-order harmonics. Thus, there is a trade-off between the attenuation effect and the control bandwidth in the design of *LC* filters.

Another issue is the large amount of transient current that flows through the inverter switches when inverters are requested to generate a significant amount of voltages suddenly in a step-wise manner. In this case, inverter switches should supply a very large amount of charging current in a very short time to build up the capacitor voltage to the requested level. When the transient charging exceeds a certain limit, the control system should decrease the current by reducing the inverter voltage instantly. Otherwise, the inverter system may be tripped by an over-current limitation.

However, when the inverter voltage is instantly reduced by the current protection mechanism, active damping may not work properly, increasing the danger that the output voltage will oscillate severely in a transient state. This problem can be solved by the over-sizing of the inverter switches, which inevitably results in increased costs.

This paper proposes *LC* filter design methods that minimize the transient current overshoot problem without decreasing the active damping performance of inverter systems.

There are infinite combinations of filter inductance and filter capacitance for a given filter cutoff frequency. Intuitively, the current ripple of a PWM inverter can decrease when the filter inductance increases. However, the output AC voltage becomes more sensitive to the load current disturbance due to the comparatively small value of the filter capacitance. Moreover, large filter inductors not only increase the cost and weight of the output filters but also increase voltage stress on the inverter switches, as the voltage drop of the inductor results in a loss of the inverter output voltage [28], [29].

This paper analyses the characteristics of output *LC* filters for PWM inverters while considering the L-C combinations. Practical circuit conditions such as the no-load, full resistive-load, and inductive-load conditions are considered in the analysis. Based on the analysis, a novel filter design method that guarantees good control dynamics and that minimizes the transient current overshoot is proposed. The proposed design method is verified in an experimental setup.

II. Analysis of PWM Inverter System

The single-phase equivalent circuit of an inverter system is described in Fig. 1. Here, VINV is the inverter output voltage, L_f is the filter inductor, C_f is the filter capacitor, and R_f is the series-equivalent resistance that exists through the filter inductor and inverter switches.

Fig. 2 shows a single-phase equivalent circuit for a properly controlled the PWM inverter system. The output regulating voltage V_{Com} regulates the AC terminal voltage of the PWM inverter to the reference voltage. The oscillation-damping voltage V_{Damp} dampens out the overshoot of the output voltage. The disturbance-rejection voltage $V_{Disturb}$ suppresses the voltage disturbance that occurs in the load current. If the PWM inverter system is controlled properly, three controlled voltages can be generated by the inverter controller described below.

A. Output Regulating Voltage

The output regulating voltage V_{Com} regulates the output terminal voltage of a PWM inverter system. When the oscillation-damping voltage V_{Damp} and the disturbance -rejection voltage $V_{Disturb}$ are ideally controlled, the load current disturbance becomes completely decoupled and the system-damping factor reaches a state of unity. Hence, the output *LC* filter serves as a time-delay component with a delay time of $2/\omega_f$ in a steady state.

Thus, the instantaneous load voltage V_{Load} can be regulated precisely to the reference load voltage V^*_{Load} when the time delay is pre-compensated according to equation (1) in a steady state.

$$V_{Com} = (1 + \frac{2}{\omega_f} s) V^*_{Load} \tag{1}$$

where, $\omega_f = 1/\sqrt{L_f C_f}$: filter cut-off frequency.

B. Oscillation-Damping Voltage

The damping coefficient can be increased electronically by generating the oscillation-damping voltage V_{Damp} according to equation (2).

$$V_{Damp} = K_{Damp} \times i_{Inv} = -aR_f \times i_{Inv}. \tag{2}$$

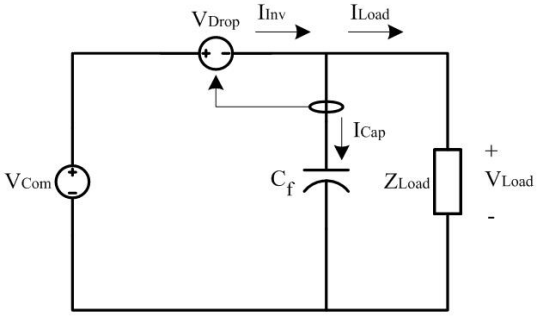


Fig. 3. Single-phase equivalent circuit of a PWM inverter system represented by two controlled voltage sources.

According to equation (2), V_{Damp} is proportional to the inverter current with a negative coefficient K_{Damp}=$-aR_f$.

Thus, the oscillation-damping voltage V_{Damp} acts as the series resistance with R_f which results in a total equivalent resistance of $(1+a)R_f$ that is connected in series with the filter inductor, L_f. Thus the effective system-damping factor ξ_c can be increased according to equation (3).

$$\xi_c = (1+a)\frac{R_f}{2}\sqrt{\frac{C_f}{L_f}} = (1+a)\xi_f. \tag{3}$$

Therefore, the control gain of the oscillation-damping voltage $K_{Damp} = -aR_f$ is determined by equation (4).

$$K_{Damp} = -aR_f = R_f - 2\xi_c\sqrt{\frac{L_f}{C_f}}. \tag{4}$$

C. Disturbance-Rejection Voltage

As the oscillation-damping voltage V_{Damp} causes an increase in the equivalent series resistance of the PWM inverter, the output voltage can be slightly different from the output regulating voltage V_{Com} depending on the load current. The magnitude of the output voltage decreases and its phase shifts from the output regulating voltage V_{Com} when the load is reactive. When the load current is non-sinusoidal, the output voltage can be further distorted by the voltage drop across the equivalent series resistance $(1+a)R_f$ and the filter inductance L_f. The disturbance-rejection voltage $V_{Disturb}$ should be generated by according to equation (5) to remove the voltage distortion due to the load current disturbance.

$$V_{Disturb} = \left[(1+a)R_f + sL_f\right] \times i_{Load}. \tag{5}$$

D. Equivalent Voltage Drop

The total voltage drop that occurs from the oscillation-dam ping voltage V_{Damp} and the disturbance-rejection voltage $V_{Disturb}$ can be calculated by equation (6).

$$\begin{aligned} V_{Drop} &= (R_f + sL_f) \times i_{Inv} - (V_{Damp} + V_{Disturb}) \\ &= \left[(1+a)R_f + sL_f\right] \times (i_{Inv} - i_{Load}) \\ &= \left[(1+a)R_f + sL_f\right] \times i_{Cap}. \end{aligned} \tag{6}$$

Here, the equivalent voltage drop V_{Drop} of a properly controlled PWM inverter system is only determined by the filter capacitor current. Thus, the single-phase equivalent circuit of the PWM inverter system shown in Fig. 2 can be simplified, as shown in Fig. 3. Here, the derivative operator in sL_f is very difficult to implement in discrete control systems because the sampling frequency causes an enormous amount of noise in the derivative operator in discrete control systems. However, around the utility frequency band, sL_f can be neglected as the value of $(1+a)R_f$ is designed around the rated load impedance Z_{rated}, which is usually 10 times larger than the filter reactance $sL_f = 2\pi f_o L_f$, which is designed at about 10% of the rated load impedance, i.e., $0.1 \times Z_{rated}$. Here f_o is the utility frequency. The equivalent voltage drop V_{Drop} causes an error in the reference load voltage.

III. Analysis of the Output LC Filter

The peak value of the inverter output current is an important factor in designing the inverter stack size. The inverter current rating is normally determined by the filter impedance and the rated load impedance in a steady state. However, in a transient state, where the inverter should synthesize the output voltage rapidly, an instantaneous inverter current may exceed its rated peak value due to the charging current flowing into the filter capacitor.

The target of equation (3) is to design a proper control gain a, that can obtain the desired system-damping factor ξ_c of the filter capacitor voltage. By selecting the proper control gain a, any control damping factor can be realized for every filter ratio. However, even for equal system-damping factors, the current overshoot may be different according to the filter ratio. As shown in the simulation waveforms in Fig. 4, the inverter current overshoot becomes larger at a low filter ratio for equal system-damping factors of filter capacitor voltages.

When the transient current of a PWM inverter exceeds its rated peak value, it must be limited by decreasing the inverter output voltage to protect the inverter switches from an over-current fault. In this case, the control dynamics of the output voltage is detrimentally affected by the transient current overshoot.

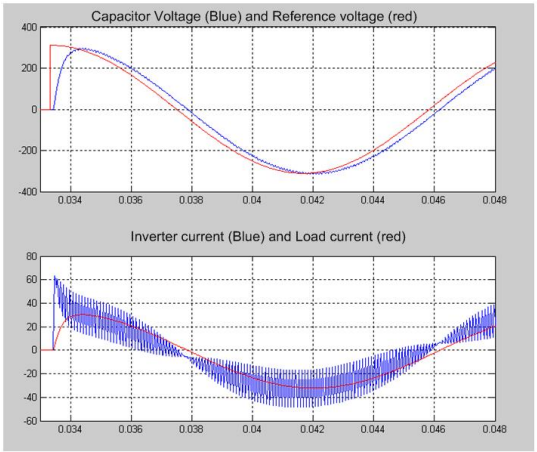
Conventionally, this type of transient current problem was solved via the over-sizing of the inverter switches, which increases the cost. This paper proposes a design guideline for *LC* output filters that does not generate the transient current overshoot problem without increasing the size of the inverter switches.

A. Equivalent Circuit With No Load

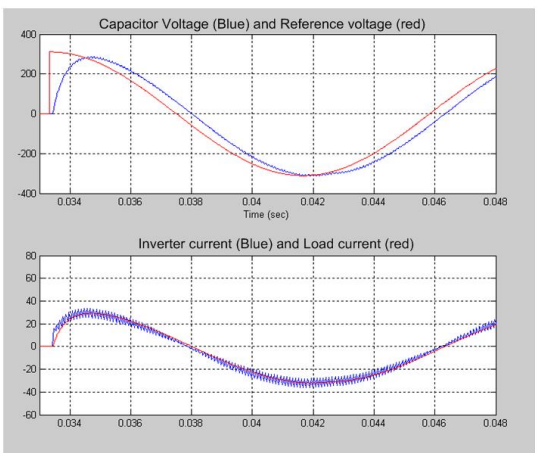
Fig. 5 shows a simplified equivalent circuit of a PWM inverter system without a load. In a worst-case scenario, the reference load voltage V_{Load}^* is commanded suddenly by the peak value of $\sqrt{2}V$, where V is the rated RMS voltage.

Because major problems generally occur in a very short time, this paper focuses on transient state analyses of the inverter system.

The reference load voltage V_{Load}^* can be regarded as a DC value during a transient state. In Fig. 5, aR_f is the equivalent resistance according to the oscillation-damping controller V_{Damp}. Various voltage-control methods to counterbalance the



(a)



(b)

Fig. 4. Simulation waveforms on the capacitor voltage (upper window blue color), the inverter current (lower window blue color) and the load current (lower window red color) by Matlab;
a) ξ_c =0.8, $\sqrt{L_f/C_f} = 0.25 \times Z_{Load}/\xi_c$,
b) ξ_c =0.8, $\sqrt{L_f/C_f} = Z_{Load}/\xi_c$.

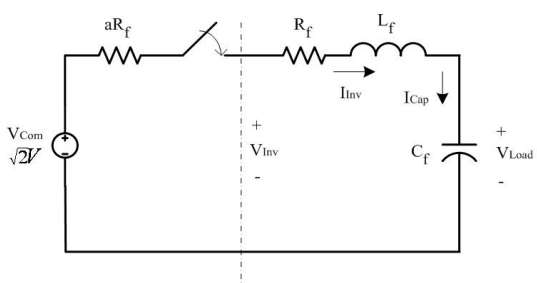


Fig. 5. Simplified equivalent circuit of a PWM inverter system without a load.

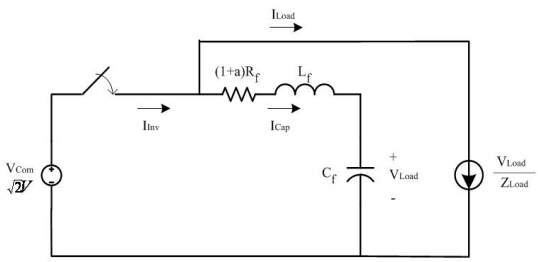


Fig. 6. Simplified equivalent circuit of PWM inverter system with a full load.

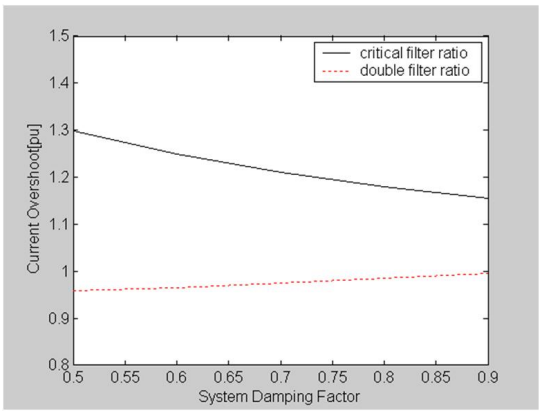


Fig. 7. Inverter Current Overshoot Depending On Filter Ratio.

time delay of output *LC* filters have been exploited as the lead-lag controller described by equation (1) no longer applies in a transient state.

However, this paper simply uses a simple feed-forward controller for regulation of the output voltage, i.e., $V^*_{Load} = V_{Com} = \sqrt{2}V$ for simplicity, as developing the output voltage controller itself is outside the scope of this paper.

The inverter current can be calculated by equation (7).

$$i_{INV} = \frac{\sqrt{2}\omega_f C_f V}{\sqrt{1-\xi_c^2}} e^{-\xi_c \omega_f t} \cdot \sin(\omega_f \sqrt{1-\xi_c^2} t). \tag{7}$$

The inverter current described by equation (7) has a maximum value when the time equals the result of equation (8).

$$t_m = \frac{\text{acos}\xi_c}{\omega_f \sqrt{1-\xi_c^2}}. \tag{8}$$

Thus maximum inverter current can be calculated by equation (9).

$$I_{INVMax} = \sqrt{2}\sqrt{\frac{C_f}{L_f}} \cdot V \cdot e^{-\text{acos}(\xi_c)/(\sqrt{1-\xi_c^2}/\xi_c)}. \tag{9}$$

Given that $I_{INVMax} < \sqrt{2}I$, where $I = V/Z_{Load}$, the ratio between the filter inductance and the filter capacitance should be limited by equation (10).

$$\sqrt{\frac{L_f}{C_f}} > Z_{Load} \cdot e^{-\text{acos}(\xi_c)/(\sqrt{1-\xi_c^2}/\xi_c)}. \tag{10}$$

Here, Z_{Load} is the rated load impedance. If we let $\text{acos}(\xi_c) = \alpha$, we can obtain following relationship:

$$\frac{\text{acos}(\xi_c)}{\frac{\sqrt{1-\xi_c^2}}{\xi_c}} = \frac{\alpha}{\tan\alpha} = \frac{\alpha}{\sin\alpha}\cos\alpha = \frac{\alpha}{\sin\alpha}\xi_c > \xi_c \tag{11}$$

Thus for simplicity, the lower boundary of the filter ratio can be concisely expressed by equation (12).

$$\sqrt{\frac{L_f}{C_f}} > Z_{Load} \cdot e^{-\xi_c}. \tag{12}$$

When the filter ratio is set to a value larger than the lower bound defined by equation (12), there is no overshoot in the inverter current at no load.

B. Equivalent Circuit with a Full Load

Although output *LC* filters are the main cause of inverter current stress in a transient state, load current sometimes adds to the current stress. Inductive loads do not increase the current stress in a transient state, as the load current increases smoothly after the load terminal voltage is established. However, when the load is purely resistive, the load current cannot be neglected because it increases sharply in proportion to the established load voltage.

The equivalent circuit of a PWM inverter system with a full load is described in Fig. 6, where the inverter output current $I_{Inv}$is the sum of the filter capacitor current I_{Cap} and the load current I_{Load}. Here, the oscillation-dam ping voltage V_{Damp} and the disturbance-rejection voltage $V_{Disturb}$ are assumed to be controlled ideally. In the worst-case scenario, the reference load voltage with a magnitude of $V^*_{Load} = \sqrt{2}V$ is suddenly required of the PWM inverter system at time $t = 0$. The worst-case scenario can also occur when the load impedance is purely resistive, e.g., $Z_{Load} = R_{Load}$.

When the output regulating voltage V_{Com} is regulated precisely to the reference load voltage $V_{Load}{}^*$ by a normal feed-forward controller, the load voltage can be calculated by equation (13).

$$\begin{aligned} V_{Load} &= \frac{\omega_f^2}{s^2 + 2\xi_c\omega_f s + \omega_f^2} V^*_{Load} \\ &= \frac{\omega_f^2 \sqrt{2}V}{s\left(s^2 + 2\xi_c\omega_f s + \omega_f^2\right)}. \end{aligned} \tag{13}$$

Thus, the filter capacitor current $I_{Cap}$and the load current I_{Load} can be calculated by equation (14) and equation (15), respectively.

$$I_{Cap} = sC_f V_{Load} = \frac{\sqrt{2}C_f V\omega_f^2}{s^2 + 2\xi_c\omega_f s + \omega_f^2} \tag{14}$$

$$I_{Load} = \frac{V^*_{Load}}{Z_{Load}} = \frac{\sqrt{2}V}{R_{Load}} \cdot \frac{\omega_f^2}{s\left(s^2 + 2\xi_c\omega_f s + \omega_f^2\right)}. \tag{15}$$

When the filter ratio is determined by $\sqrt{L_f/C_f} = R_{Load}/2\xi_c$, which is a critical value when $R_{Load} = (1+a)R_f$, the filter capacitor current can be expressed by equation (16).

$$I_{Cap} = \frac{\sqrt{2}V}{R_{Load}} \cdot \frac{2\xi_c\omega_f}{s^2 + 2\xi_c\omega_f s + \omega_f^2}. \tag{16}$$

The inverter output current $i_{Inv}(t)$in the time domain can then be calculated by the sum of the filter capacitance current $i_{Cap}(t)$and the load current $i_{Load}(t)$, as expressed by equation (17).

$$\begin{aligned} i_{Inv}(t) &= i_{Cap} + i_{Load} \\ &= \frac{\sqrt{2}V}{R_{Load}} \cdot \left[1 + \frac{e^{-\xi_c\omega_f t}}{\sqrt{1-\xi_c^2}} \cdot \sin\left(\omega_f\sqrt{1-\xi_c^2} \cdot t - \cos^{-1}\xi_c\right)\right]. \end{aligned} \tag{17}$$

The inverter current reaches its maximum value at $t_m = 2 \cdot \cos^{-1}\xi_c/(\omega_f\sqrt{1-\xi_c^2})$. Therefore, the maximum inverter current can be calculated by equation (18).

$$I_{InvMax} = \frac{\sqrt{2}V}{R_{Load}} \cdot \left(1 + e^{-\frac{\xi_c}{\sqrt{1-\xi_c^2}}\cos^{-1}\xi_c}\right). \tag{18}$$

When the filter ratio is set to twice the critical ratio, $\sqrt{L_f/C_f} = R_{Load}/\xi_c$, the maximum inverter current can be calculated by equation (19).

$$I_{InvMax} = \frac{\sqrt{2}V}{R_{Load}} \cdot \left(1 - \sqrt{1-\xi_c^2} \cdot e^{-\left(\frac{\pi - \cos^{-1}\sqrt{1-\xi_c^2}}{\sqrt{1-\xi_c^2}}\right)}\right). \tag{19}$$

Fig. 7 shows the inverter current overshoot calculated by equations (18) and (19) depending on the filter ratio when the system-damping factor ranges from 0.5 to 0.9. The proposed theory can be applied to the entire range of the system-dam ping factor. However, because the normal control target of the system-damping factor on the capacitor voltage is usually around 0.5˜0.9, system-damping factors lower than 0.5 or higher than 0.9 are not considered in this paper. When the filter ratio is set to a critical value, the inverter current overshoot decreases according to the system-damping factor; this is always higher than 1.15, as shown in Fig. 7. When the filter ratio is set to twice the critical value, the inverter current overshoot is always less than 1.0.

Thus, in purely resistive loads, the filter ratio may be set to the upper bound, as $\sqrt{L_f/C_f} < R_{Load}/\xi_c$, to maintain the inverter output current under the rated peak value in a transient state. When the load is highly inductive, the filter ratio can be set to the lower bound, as expressed by (12). A lower filter ratio is preferred because large filter inductors have a detrimental effect on the load current disturbance, leading to cost and weight issues related to the output *LC* filters and voltage stress on the inverter. Therefore, this paper proposes a filter design guideline for determining the filter ratio according to equation (20).

$$\frac{Z_{Load}}{\xi_c} \geq \sqrt{\frac{L_f}{C_f}} \geq \frac{Z_{Load}}{e^{\xi_c}}. \tag{20}$$

Here, the upper bound is for a purely resistive full load, the lower bound is for no load, and the middle region is for inductive loads or partial loads.

By combining equation (4) with the upper bound of equation (20), the gain of the oscillation-damping controller is as follows:

$$K_{Damp} = -aR_f = R_f - 2Z_{Load}. \tag{21}$$

Therefore, this paper proposes a *LC*-filter design step as follows;

1) Determine the filter cut-off frequency referring to the inverter switching frequency,

$$\omega_f = \frac{1}{\sqrt{L_f C_f}} \leq \frac{\omega_{sw}}{10}$$

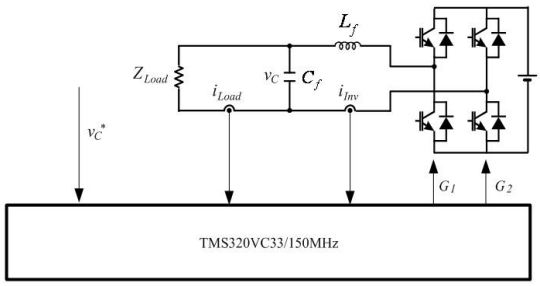


Fig. 8. Experimental setup.

TABLE I
EXPERIMENTAL CONDITIONS

V_{CMAX}	120V
Z_{Load}	5Ω resistive
F_{sw}	10kHz
F_c	840Hz

2) Determine the filter ratio referring to the rated load impedance and the control-damping coefficient,

$$\sqrt{\frac{L_f}{C_f}} = \frac{Z_{Load}}{\xi_c}$$

3) Calculate the control gain of the oscillation-damping controller,

$$K_{Damp} = R_f - 2Z_{Load}$$

IV. EXPERIMENTAL RESULTS

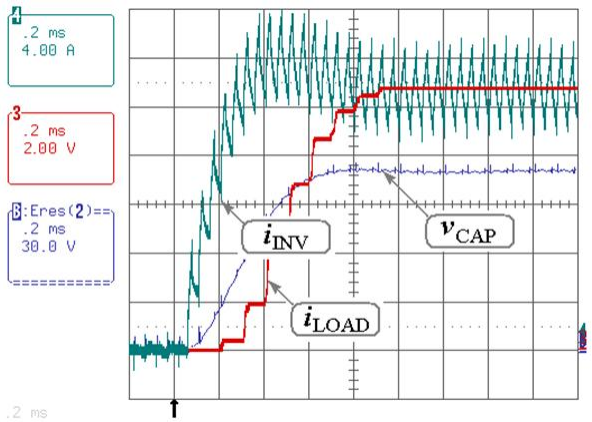
Fig. 8 shows the experimental setup that verifies the proposed design method for the output LC filter. The experiment was performed on a single-phase inverter module. The experimental conditions are shown in Table I. A sinusoidal reference load voltage was applied when its magnitude was at the maximum value of 120V. The inverter was composed of 4 IGBT switches with a switching frequency of 10 kHz. The sampling time of the digital control system is 10 kHz.

As the filter cutoff frequency was set to 840Hz, as shown in Table I, the control bandwidth of the proposed controller reached 840Hz, which allowed the PWM inverter system to synthesize the voltage harmonics up to the 13TH order. The harmonic attenuation at the switching frequency was about – 43dB; hence, only 0.7% of the voltage ripple caused by inverter switching remained in the output load voltage as noise.

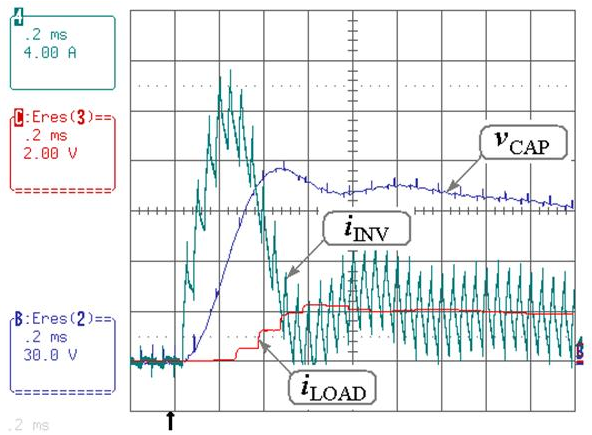
Fig. 9 shows the experimental waveforms of the transient response when the system-damping factor is set to 1.0 and the load is purely resistive. Fig. 9(a) shows the waveforms when the filter ratio between the inductor and the capacitor was designed as $\sqrt{L_f/C_f} = Z_{Load}$ according to the upper bound of equation (20). While the load current settles around 21.6 A, the inverter current overshoots to around 24A in its center value, which indicates that the inverter current reaches approximately 1.1 times its rated peak current. Considering the normal safety factors of IGBT switches, this amount of over-current is practically acceptable.

TABLE II
DESIGNED FILTER INDUCTOR AND CAPACITOR

f_c	840Hz
L_f	900μH
C_f	40μF



(a)



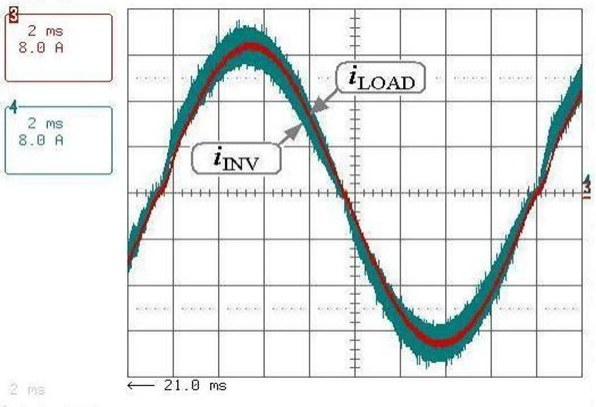
(b)

Fig. 9. Experimental waveforms when the sampling time and the PWM switching frequency are 10kHz, the system-damping factor is 1.0, and the load is purely resistive (horizontal axis: 0.2ms/div, vertical axis: 4.00A/div or 30.0V/div);
a) $\sqrt{L_f/C_f} = Z_{Load}$,
b) $\sqrt{L_f/C_f} = Z_{Load}/4$.

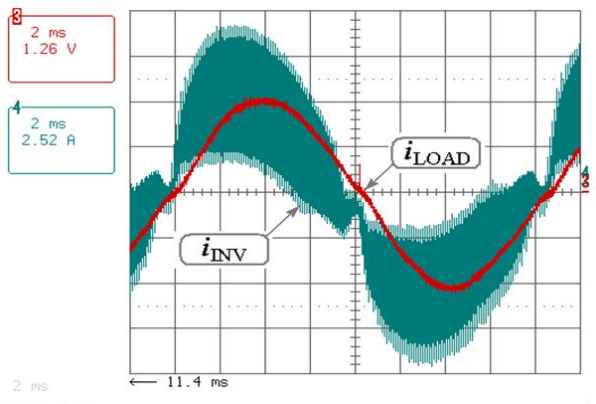
Fig 9(b) shows the wave forms when the filter ratio was adjusted to $\sqrt{L_f/C_f} = Z_{Load}/4$. by replacing the load resistor with 20Ω, which is four times larger than the case shown in Fig. 9a. While the load current settles around 4A, the inverter current overshoots to approximately 19A in its center value, which indicates that the inverter current reaches nearly 4.75 times its rated peak current.

This over-current may conflict with typical safety factors of IGBT switches. The output load voltage v_{Cap} also shows some oscillatory behavior.

Fig. 10 shows the experimental waveforms of the steady state response of the proposed inverter system with the same filter combination described in Fig. 9. The peak value of the inverter ripple current in a steady state reaches around 1.2 times the rated peak value in Fig. 10a, where the filter ratio was designed according to $\sqrt{L_f/C_f} = Z_{Load}$. It reaches nearly 1.8 times to the rated peak value in Fig. 10b where the filter ratio was designed according to $\sqrt{L_f/C_f} = Z_{Load}/4$. In both cases, the THD value is close to 1.8%.



(a)



(b)

Fig. 10. Experimental waveforms when the sampling time and the PWM switching frequency are 10kHz, the system-damping factor is 1.0, and the load is purely resistive (horizontal axis: 0.2ms/div, vertical axis: 4.00A/div or 30.0V/div);
a) $\sqrt{L_f/C_f} = Z_{Load}$,
b) $\sqrt{L_f/C_f} = Z_{Load}/4$.

V. Conclusions

This paper analyzed the characteristics of LC filters as they relate to the filter capacitor voltage and the filter inductor current of PWM inverters in a transient state. When PWM inverters are required to generate a sudden output voltage in a step-wise manner, inverter switches should supply a very large amount of charging current into the filter capacitor, which increases the inverter stack size. This paper proposed a novel filter design method for the output LC filters of PWM inverters which does not generate unnecessarily high current stress in the inverter switches nor degrade the control performance of the inverter system.

Experimental results have verified that the proposed output LC filter ensures minimum transient current overshoot and good control dynamics for PWM inverter systems.

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