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Interconnect Scaling에 따른 온칩 인터커넥 인덕턴스의 중요성 예측

(Predicting the Significance of On-Chip Inductance Issues Based on Inductance Screening Results)

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요 약

Chip 동작 주파수가 상승함에 따라, 온-칩 인터커넥에서 인덕턴스 문제 대한 우려가 증가하고 있다. 본 논문에서는 VLSI 설계에서 인덕턴스 효과가 큰 인터커넥을 선택하는 2단계의 인덕턴스 screening tool을 소개한다. Technology가 scaling함에 따라 인터커넥의 단면이 줄어들어 저항이 증가한다. 저항의 증가는 인덕턴스의 영향을 줄이는 효과가 있다. 따라서 각각 다른 CMOS 공정(0.25μm, 0.13μm, 90nm)을 사용하여 디자인된 칩을 개발한 tool로 실험함으로써 technology scaling에 따른 인덕턴스 영향을 분석해 보았다. 인덕턴스 screening tool의 결과는 디자인의 0.1% 이내의 net들이 작동 주파수에서 인덕턴스 문제를 보임으로써, 모든 인터커넥에 인덕턴스 모델을 추가하는 대신 인덕턴스 screening을 한 후 필요한 인터커넥에만 추가하는 것이 효율적임을 알 수 있다. 대부분 test chip들이 본래 칩 동작 주파수에서는 인덕턴스 영향이 문제되지 않았지만, 주파수를 높일 경우 문제가 되는 인터커넥들을 찾아낼 수 있었다. 본 연구에서 개발한 인덕턴스 screening tool은 회로 설계자들에게 유용한 지침을 제공할 수 있을 것이다.

Abstract

As chip operating frequency increases, there is growing concern about on-chip interconnect inductance. This paper presents a two-step inductance screening tool to select interconnects with significant inductance effects in a VLSI design. Test chips designed in different CMOS technology nodes are examined. The inductance screening results show that 0.1% of the nets in a design have inductance problems with chips running at its operating frequency, supporting the necessity of a screening process instead of adding inductance model to all the nets in the design. The increase in resistance due to geometry scaling will strongly affect the significance of inductance on delay as technology and frequency scale. Since higher frequency worsens inductance problem and geometry scaling alleviates it, inductance screening tool can provide useful guidelines to circuit designers.

Keywords : Interconnect, inductance, VLSI, delay, CMOS technology.

Ⅰ. Introduction

As technology scales, interconnect parasitic effects become increasingly important and directly limit circuit performance and wiring density. Post-layout full-chip parasitic resistance and capacitance extraction is now a standard step in integrated circuit design flow. Full-chip inductance extraction is known

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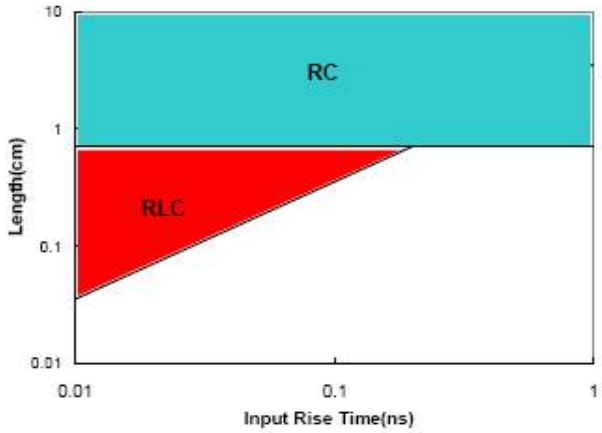


그림 1. 신호상승시간이 줄어듦에 따라 RLC modeling 이 필요한 인터커넥 길이 영역이 늘어난다. R = 400 Ω, L = 20 nH and C = 1 pF.

Fig. 1. Length range of interconnect where RLC modeling is necessary R = 400 Ω, L = 20 nH and C = 1 pF.

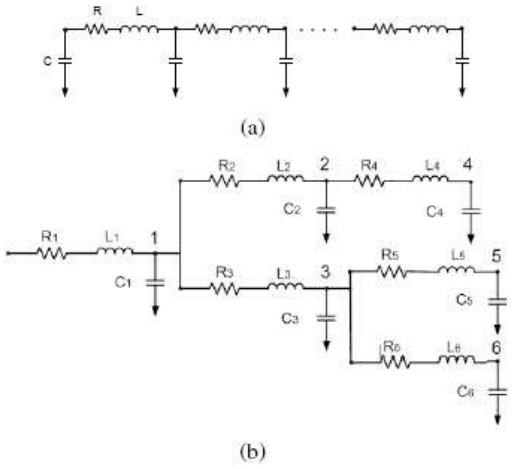


그림 2. RLC interconnect 구조
(a) 분산된 RLC 전송선 (b) RLC tree 구조

Fig. 2. RLC interconnect structure.
(a) Distributed RLC transmission line.
(b) RLC tree structure.

to be prohibitively complex because of unknown inductive current return paths, and circuit simulation including interconnect inductance is expensive[1]. Inductance opposes an instantaneous change in current. As a result, when a signal switching speed is fast enough such that the inductance effect becomes noticeable, the line delay becomes larger. Inductance also causes ringing, reflections, crosstalk noise, and simultaneous switching noise. Current static timing analysis tools cannot handle inductance ,and circuit simulation including inductance is very time consuming[2]. As a result, it would be a significant waste of resources to extract inductance for all the nets and include them in the simulations, when only a few of them actually affect the signal integrity.

Deustch[3] characterized on-chip interconnects by dividing them into three categories, which are short, medium and long based on its length, and developed the criteria to determine when inductance influences signal delay and crosstalk. Based on the circuit simulation results and transmission line theory, it is shown that the inductance effects depend on the driver strength, loading capacitance, and the signal attenuation, and appears predominantly on medium length lines. Ismail[4] defined the rules to characterize the importance of on-chip inductance based on the signal rise time and the line damping ratio. This region is expressed as Equation 1 and is shown in Figure 1.

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}} \qquad (1)$$

Figure 1 shows that regardless of the rise time, if the wire length is longer than a certain length, then the lines can be modeled with RC only because of high signal damping. Interconnects in medium length range require RLC modeling. As the rise time becomes smaller, more interconnects require inductance modeling.

The criteria to identify lines with inductance effects published in [3] and [4] are based on a single transmission line structure as shown in Fig. 2(a). However, most of the onchip interconnects are tree structures as shown in Fig. 2(b). In this work, we will use RC and RLC delay difference as a criteria to perform inductance screening. Previous work suggested parameters to characterize RC and RLC delay on tree structures. For RC tree structures, Elmore suggested that the delay can be characterized with time constant τ [6].

$$\tau = \sum_i R_i C_{iT} \quad (2)$$

where R_i is the resistance of a section in the path, and C_{iT} is the total load capacitance seen from that section.

Ismail[7] published analytic delay models for RLC trees that are based on the second order approximation of the transfer function and preserve the recursive properties of the Elmore model. Closed-form delay models are characterized with two parameters, ζ and ω. ζ and ω for an RLC tree can be calculated as follows[7].

$$\zeta = \frac{1}{2}\frac{\sum_i R_i C_{iT}}{\sqrt{\sum_i L_i C_{iT}}}, \omega = \frac{1}{\sqrt{\sum_i L_i C_{iT}}} \quad (3)$$

where R_i and L_i are the resistance and inductance of a section in the path, and C_{iT} is the total load capacitance seen from that section of the RLC tree.

Delay models proposed in [6] and [7] do not consider input rise time. Since the impact of inductance on delay is a strong function of signal rise time, for the delay based screening criteria, we will use the closed-form RC and RLC delay models considering input rise time published in [8].

This paper is organized as follows: A two-step inductance screening algorithm, models used for inductance screening, and a stand-alone screening tool implementation is presented in Section Ⅱ. Experimental results obtained by running the screening tool on 0.25 μm 0.13 μm and 90 nm test chips and implications on the significance of inductance effects as technology scales are provided in Section Ⅲ. The paper is concluded in Section Ⅳ.

Ⅱ. INDUCTANCE SCREENING TOOL

The inductance screening tool can be positioned between the parasitic RC extraction step and the timing analysis step in the back-end analysis flow as shown in Figure 3. The .SPF, the standard parasitic extraction output file format, and the .LIB, the timing technology library file, are the inputs to the inductance screening tool. Both of them are EDA standard file formats[9~10]. The self inductance estimation that is added to the parasitic extraction will be discussed in this section. Since the significance of inductance effects is a strong function of signal rise time, the rise time information is provided via the .LIB file.

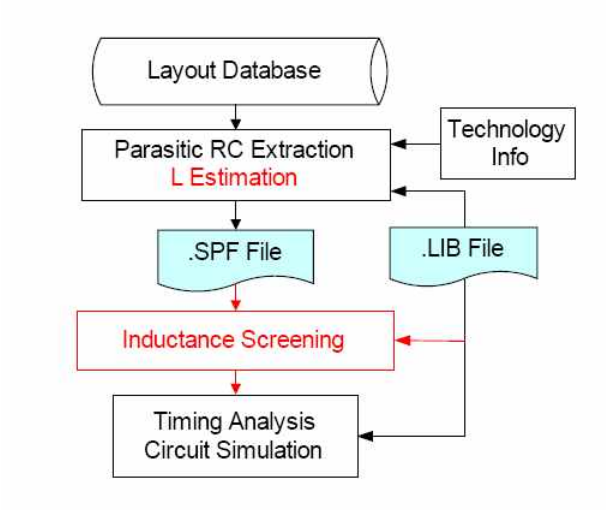


그림 3. Parasitic extraction과 timing 검사 과정. Inductance screening tool은 기준 파일 서식을 기반으로 실행

Fig. 3. Parasitic extraction and timing verification flow. Inductance screening tool is implemented based on the standard file formats.

1. Two-Step Inductance Screening Algorithm

The proposed inductance screening algorithm performs the net-by-net screening in two steps, the pre-screening step, and the main screening step. The pre-screening step selects the nets that may be subjected to inductance effect by testing the following two criteria.

$$t_r \leq 10t \quad (4)$$

$$\zeta \leq 1.3 \quad (5)$$

TOF is the time-of-flight[11], t_r is the signal rise time and ζ is the damping ratio. Equation (4) screens out short wires that can be modeled as lumped

capacitors by comparing the signal rise time and time of flight[3, 11]. In tree structures, it is hard to define the velocity of propagation, which is given as $v_p = 1/\sqrt{LC}$ for transmission lines. For tree-structures, we can replace LC in the expression for v_p with LC summation shown in Equation (3), and we can then derive TOF that is equal to $1/\omega$, where ω is given in Equation (3). Equation (5) screens out long wires that have high signal attenuation.

For the nets selected in the pre-screening step, the main screening step selects the nets which have a large discrepancy between RC and RLC delay. The criteria is to compare the difference of RC and RLC delay estimates to a certain percentage, γ, of the rise time as follows:

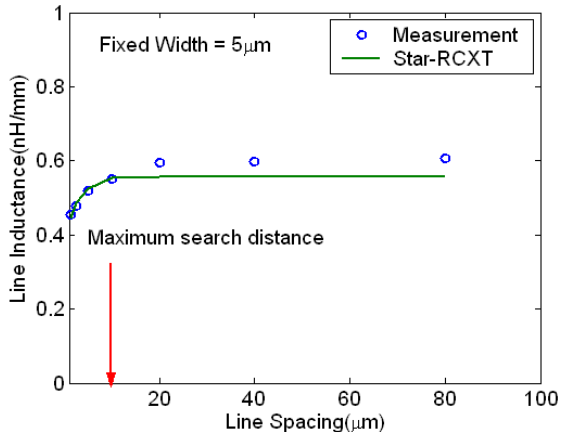
$$t_d(RLC) - t_d(RC) \geq \gamma \bullet t_r \qquad (6)$$

$$\gamma = 0.05 - 0.25$$

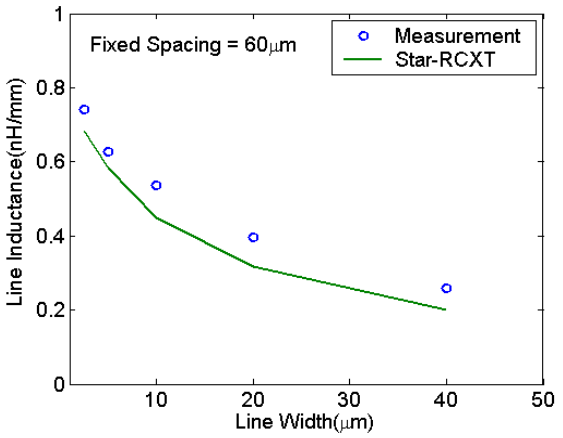
where t_r is the signal rise time, and $t_d(RC)$ and $t_d(RLC)$ are the 50% RC and RLC delay, respectively. determines the selectivity of the inductance screening, usually between 0.1 and 0.3. With γ of 0.2, the screening tool selects nets with a RC and RLC delay difference larger than 20% of the specified rise time. Since a higher clock frequency means a smaller rise time, a faster clock requires a tighter error range in the delay estimation. The acceptable error margin in the delay difference, the right hand side of Equation (6), has been chosen to be proportional to tr. The inductance screening conditions depends not only on the inductance value itself, but also on the resistance and capacitance of the line and the signal rise time. To estimate RC and RLC delay, the closed-form delay models considering input rise time published in [8] are used.

2. Self-Inductance Estimation in Parasitic Extraction Tool

The screening conditions and the delay models used for screening, (4), (5), (6), have a first order dependence on the values of resistance and capacitance, but has a square root dependence on the value of inductance. Hence, even with a low fidelity estimation of self-inductance, inductance screening can be performed with no significant error. Although accurate self-inductance extraction is difficult due to frequency dependent current return path[2], most of the commercial extraction tools now have an option to provide self-inductance estimation values based on certain assumptions. In parasitic extraction, once capacitance is known, low fidelity inductance can be



(a)



(b)

그림 4. 인덕턴스 추출과 측정 비교
(a) 고정된 line width(= 5.3 μm) 에서 line spacing에 따른 그래프 (b) 고정된 line spacing(= 60 μm)에서 line width에 따른 그래프

Fig. 4. Inductance extraction and measurement comparison. (a) Spacing to the ground is varied. Fixed signal width = 5.3 μm. (b) Signal width is varied. Fixed spacing to ground = 60 μm.

found using $v_p = 1/\sqrt{LC}$. Another way is to assume that the return current flows through the closest neighboring lines and use the analytical formula based on partial inductance[12]. In parasitic extraction tools, often there is a rule to search the neighboring environment to define shielding for capacitance extraction. The extraction engine has a limit on the maximum distance it can search around its neighbor for the closest shielding lines. The limit in Star-RCXT engine was 10 μm[10].

Figure 4 compares the inductance values predicted from Star-RCXT and the measurement results of the test chip[13]. The test chip has a number of signal and ground line pairs on metal with different widths and spacings. Figure 4(a) shows how the inductance varies while the distance to the ground line varies with a fixed signal width. The measurement and Star-RCXT prediction match well up to 10 μm, but the matching degrades beyond 10 μm due to the search distance limitation. Figure 4(b) shows the case when the signal line width is varied while the spacing to the ground line is fixed. Since the fixed spacing of 60 μm, is larger than the search distance of Star-RCXT, the substrate is the current return path resulting in a lower accuracy. Nevertheless, the inductance dependence on signal width is predicted correctly. The inductance estimation results may not be accurate enough for circuit simulation, but captures the distance and width dependence with some limitations coming from the limit on the search distance.

3. Inductance Screening Tool Implementation

An overview of the screening tool is shown in Figure 5. The screening tool was implemented in C language. The input file parser reads in the net parasitic information from the .SPF file and the cell pin rise time information from the .LIB file. User input mode (fast, medium, or slow) specifies which rise time should be used from the .LIB file for inductance screening. The pin rise time is used as the signal rise time for I/O pins and as a default rise

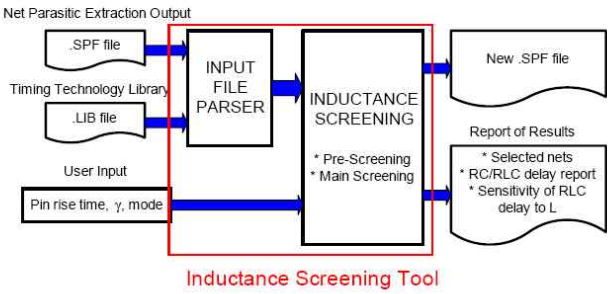


그림 5. 인덕턴스 검사 도구 개요
Fig. 5. Inductance Screening Tool Overview.

time if the library does not exist. γ is explained in the previous section and determines the selectivity of screening. The input file parser parses the net section of the .SPF file net-by-net, forming a graph structure. The input parser reads in the names of the instance pins and subnodes which correspond to the vertexes of the graph structure. Each vertex has a capacitance value associated with it and each edge has a resistance and an inductance associated with it. The vertex and the edge information is saved using static hashing and the graph is formed by mapping the incident edge in the adjacency-list. Starting from the net input vertex, the breadth-first-search spanning tree is defined by marking the parent of each vertex[14].

The .LIB file information is stored in a cell type table containing the min/max and rise/fall time for each pin type. The outputs of the screening tool are a new .SPF file with unnecessary inductors removed and auxiliary output files that report the list of the selected nets. Since the inductance value that is used for inductance screening is not very accurate, the sensitivity of RLC delay to inductance[8] is reported for the selected nets to decide whether more accurate inductance extraction is necessary.

Ⅲ. EXPERIMENTAL RESULTS

In this section, we show the inductance screening results of test chips designed in 0.25 μm, 0.13 μm, and 90 nm technologies. By comparing the results

표 1. 스탠포드 인덕턴스 테스트 칩의 22개의 test structure의 구조. 각각의 test structure는 signal line과 ground line 쌍을 포함

Table 1. Geometries of the 22 test structures in Stanford Inductance test chip. Each test structure consists of a signal and ground line pair.

Net Name	Signal Width(μm)	Spacing to GND(μm)	Net Name	Signal Width(μm)	Spacing to GND(μm)
1	5	5	12	5	20
2	40	60	13	5	40
3	5	70	14	5	80
4	10	75	15	1.25	71.25
5	20	70	16	0.8	71
6	2.5	79	17	5	1.25
7	80	40	18	2.5	10
8	160	40	19	2.5	40
9	5	2.5	20	2.5	2.5
10	5	5	21	0.8	1.25
11	5	10	22	20	1.25

among different technology nodes, we can make predictions on the significance of inductance effects as technology scales. The screening results are verified by running HSPICE simulations on the selected nets. The net length distributions of the selected nets are examined and compared with theoretical predictions.

1. Stanford Inductance Test Chip

The first case is a test chip used in section II.2. to measure line inductance[13]. This chip was designed using 5 metal layer, 0.25 μm technology. The screening was performed for 22, 4 mm signal lines located on the top metal layer, and the geometries are shown in Table I. The signal lines were designed to measure inductance, so devices are not connected to the signal lines. Therefore no .LIB file is available, so the inductance screening tool uses user specified pin rise time. The screening was performed for two different rise times, 50 ps and 150 ps with γ of 0.2. For a rise time of 50 ps, all the nets except NET 21 are selected. It is the narrowest line in the design, so it has the highest resistance. NET 16 is also 0.8 μm wide, so it has the same resistance as NET 21, but the spacing to the ground line is larger. The farther the ground line, the larger the loop size, so NET 16 has a larger inductance than NET 21. For rise time of 150 ps, only 2 nets are selected. For the inductance effect to be visible even at 150 ps, the line should have a very low resistance. So the selected lines are among the widest lines in the design. However, NET 8 with a 160 μm width is not selected. Because inductance decreases logarithmically as width increases, the inductance value for this net is very low, even though the line resistance is also low. To validate the screening results, HSPICE was used to find the RC and RLC delay differences with 150 ps rise time. Figure 6 shows that the two signal lines that have the largest differences from HSPICE simulation are the ones that are selected from the inductance screening tool.

2. ASIC and Full-Custom Test Results

Two commercial ASIC (Application Specific Integrated Circuit) designs, Design 1 and Design 2, and full-custom high speed link design, Design 3, are tested with the inductance screening tool. The specifications of the test chips are summarized in Table II.

For standard cell-based Design 1 and Design 2, when they are tested with their own timing technology library files, around 10% of the total nets are selected in the pre-screening step, but no nets are selected at the main screening step. In order to examine how the inductance effects worsen as rise time decreases, pin input rise time specified by the user is used to perform screening. For Design 1, with the screening criteria of γ = 0.2 and user input rise time of t_r = 30 ps, one net is finally selected. The selected net is a 2 mm global signal line as shown in

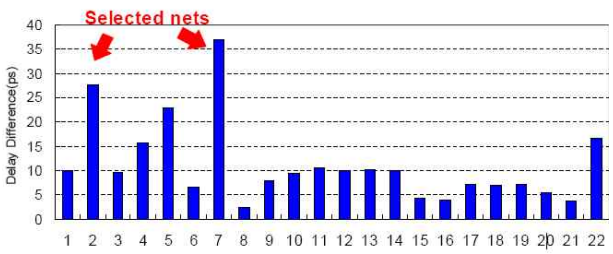


그림 6. 150ps의 rise time으로 HSPICE를 이용하여 simulation 한 test structure의 RC와 RLC delay의 차이

Fig. 6. RC and RLC delay difference for 22 test structures are simulated using HSPICE with rise time of 150 ps.

표 2. 인덕턴스 검사에 사용되는 test chip들의 특성 요약

Table 2. Summary of the test chips used to perform inductance screening.

	Design 1	Design 2	Design 3
Technology	0.13um, 6ML	0.13um, 8ML	90nm, 8ML
Chip size (mm x mm)	4.0 x 1.3	10.3 x 10.3	1.0 x 1.0
# of nets	167K	912K	2.7K
SPF file size (MB)	177	808	57

Figure 7(a). The total number of inductors in the original .SPF file before screening was 671,848. The number reduces to 12 after the screening. Therefore, it would be a great waste of resources to extract inductance and include inductance models for all the nets, especially when only a very small portion of them affect the signal integrity.

For Design 2, the length distributions of the selected nets for different t_r's and γ's are examined. The selected nets have medium lengths, because short wires do not show transmission line effects and very long wires have high signal attenuation. Figure 7(b) shows how the distribution changes as t_r becomes smaller. As rise time gets faster, shorter wires show inductance effects, but the distribution does not spread to longer lines because they have high signal attenuation. The results are in good agreement with the published theoretical predictions [3][4]. Figure 7(c) shows how the distribution changes for different γ's. More nets are selected for a smaller γ. Larger γ means less selective screening, the lines selected in larger γ are the wires with more severe inductive effects. Design 3, a 90 nm test chip, is a full custom design, we do not have any library for the cells. So we estimated the fastest signal rise time to be around 30 ps from the clock speed which was 2 GHz. With this rise time, no nets were selected from the inductance screening tool. The rise time has to be reduced to 8 ps before any line shows inductance effect. The length distributions of the selected nets for different t_r's, 3 ps, 4 ps and 5 ps

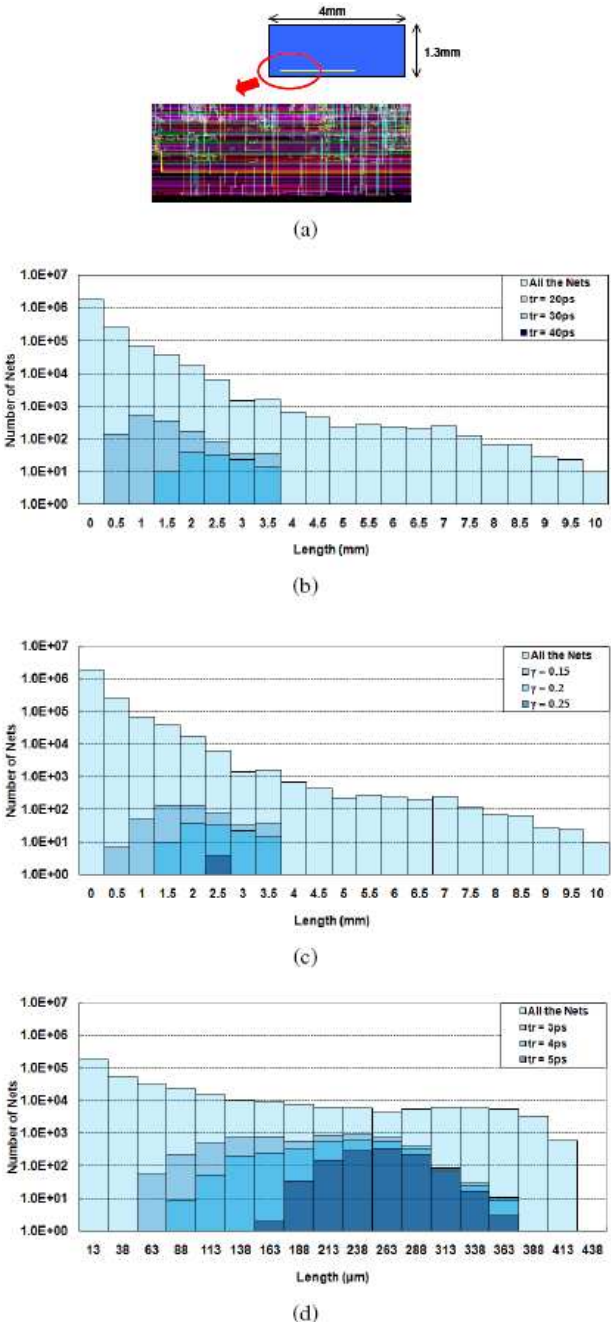


그림 7. Test chip 인덕턴스 감시 결과
(a) Design 1 은 γ = 0.2, t_r = 30 (b) Design 2 에서 다른 t_r을 사용한 그래프 (c) Design 2에서 다른 γ를 사용한 그래프 (d) Design 3 에서 다른 t_r을 사용한 그래프

Fig. 7. Test chip inductance screening results.
(a) Selected net with γ = 0.2 and t_r = 30 from Design 1. (b) Selected net length histogram for different t_r's for Design 2. (c) Selected net length histogram for different γ 's for Design 2. (d) Selected net length histogram for different t_r's for Design 3.

are shown in Figure 7(d). These results strongly support the necessity of the screening tool, since inductance is not a problem for most of the nets in a design.

3. Implications on Technology Scaling

As an experiment, we applied the same user input rise time as an input to the inductance screening tool and compared the results of the three designs which are in different technologies. This is to estimate the possibility of inductance becoming a problem with IC technology and frequency scaling. The results are shown in Table III. As expected, inductance effects is more severe for high operating frequency and hence faster rise time. As technology geometry scales, the area of the interconnect cross section becomes smaller so the line becomes more resistive. From our test results, we can see that inductance problems are worse if the chip operating frequency is pushed higher in older technologies than the newer ones.

표 3. 다른 검사 기준에 따라 NET 이 선택된 개수
Table 3. Number of nets selected with different screening criteria.

γ = 0.2	Design 1	Design 2	Design 3
20ps	13	729	0
15ps	60	1740	0
5ps	18040	78770	8

Ⅳ. CONCLUSION

In this work, we developed a two-step inductance screening tool that can be used in standard back-end analysis flow and applied in a real chip designs. We showed the inductance screening results of IC designs in 0.25 μm, 0.13 μm, and 90 nm technologies. The results show that less than 0.1% of the nets in a design have inductance problems, supporting the necessity of a screening process before performing inductance extraction and delay simulation. Furthermore, we validated the screening results by comparing them with the HSPICE simulation results. Since higher frequency worsens inductance problem and geometry scaling alleviates it, inductance screening tool can provide useful guidelines to circuit designers.

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