An Inherently dB-linear All-CMOS Variable Gain Amplifier

Ji-Wook Kwon and Seung-Tak Ryu

Abstract—**This paper introduces a simple variable gain amplifier (VGA) structure that shows an inherently dB-linear gain control property. Requiring no additional components for dB-linear control, the structure is compact and power efficient. The designed two-stage VGA shows a gain control range of 60dB with the gain error in the range of ±0.4 dB. The power consumption including the output buffer is 20.4 mW from 1.2 V supply voltage with bandwidth of 630 MHz. The prototype was fabricated in a 0.13 μm CMOS process and the VGA core occupies 0.06 mm^2**

Index Terms—**Variable gain amplifier, dB-linear, inherently dB-linear, cascode amplifier**

I. INTRODUCTION

Most communication systems possess a VGA in their receiver path to enhance the system dynamic range [1]. VGAs adjust their gain as the input signal strength changes, and the gain change must settle within a certain time period regardless of the amount of input signal change [2]. In order to realize such a constant settling time of the gain, most VGAs embed a dB-linear gain control capability [2].

Implementing a dB-linear gain characteristic with a CMOS amplifier, however, has not been a trivial work. Unlike BJT amplifier where its V-I curve is inherently exponential, CMOS amplifier needs to manipulate the circuit for dB-linear gain control. Various CMOS VGA

structures have been reported to implement such a function.

Representative method is to use exponential function generator. Relatively linearly gain-controlled amplifiers such as Gilbert cell and signal-summing structure [3-6] could achieve dB-linear characteristics by using a parasitic BJT in CMOS process or MOSFETs in sub-threshold region, respectively.

Robust dB-linear gain control can be implemented by using a negative feedback control [7, 8]. The feedback loop composed of exponential generator and the replica VGA cell produces a dB-linear gain control voltage according to the inverse exponential input voltage. Owing to the feedback loop and VGA replica block, VGA cell does not need to have linear gain control property to the control voltage. Thus, overall VGA can have stable and accurate dB-linear characteristic regardless of the amplifier structure.

As a different approach, pseudo dB-linear designs have been reported [9-11] with only MOSFETs. This approach is to find approximate exponential function without using parasitic BJT or MOSFET in sub-threshold region. Paper [9] and [10] could achieve the dB-linear gain characteristic by controlling the bias current of the input pair and the diode-connected output loads with their own control circuit. However, one critical drawback of this method is that the bandwidth of the amplifier varies as the gain changes, and thus the amplifier showed seriously reduced bandwidth at high gain mode. This limits the application of this technique for wideband system. Paper [11] achieved a pseudo dB-linear characteristic from a cascode amplifier, whose input pair works in triode region, without using additional exponential function circuit. Since the bandwidth of the cascode amplifier does not change regardless of the

control voltage, wide bandwidth could be obtained.

In this paper, the technique in [11] is reviewed qualitatively and quantitatively. In addition, several secondary effects such as body effect, channel length modulation, process and temperature variations are considered. Based on the study, an inherently dB-linear cascode VGA is designed with wide gain range per stage and accurate dB-linear characteristic.

Section II introduces the inherently dB-linear amplifier structure and analyzes its gain characteristic. Section III discusses the circuit non-ideal effects and process and temperature variation effect. Section IV presents the overall architecture of the designed VGA and circuit implementation. Section V presents the experimental results, and finally, conclusions are given in Section VI.

II. INHERENTLY DB-LINEAR VGA CELL

Fig. 1 shows the basic amplifier structure of this work. The input transistors (M_1, M_2) operate in triode region by the properly given control voltage (V_C) while the others (M_0, M_3, M_4) are in saturation region. According to the drain current equation in the triode region, the current through the input transistors and the transconductance (g_m) of it can be expressed as Eqs. (1, 2).

$$I_{M_1,Triode} = \beta_1[(V_{GS1} - V_{TH1})V_{DS1} - \frac{V_{DS1}^2}{2}] \quad (1)$$

$$g_{mM1,Triode} = \beta_1 \cdot V_{DS1} \quad (2)$$

From Eq. (2), the gain of the amplifier can be derived as Eq. (3).

$$A_V = g_{mM1,Triode} \cdot R = \beta_1 \cdot V_{DS1} \cdot R \quad (3)$$

In Eq. (3), β_1 and R are independent of control voltage (V_C). By the relationship between V_C and V_{DS1}, we can obtain the relationship between the control voltage (V_C) and the gain (A_V).

In order to find V_{DS1} as a function of V_C, first, the Eq. 1 can be rewritten as Eq. (4).

$$I_{M_1,Triode} = \beta_1[(V_{G1} - V_{S1} - V_{TH1})V_{DS1} - \frac{V_{DS1}^2}{2}] \quad (4)$$

From Eq. (4), the relationship between V_C and V_{DS1} can be found quantitatively. Except for V_{S1} and V_{DS1}, other conditions such as the bias current ($I_{M1,Triode}$), the size of transistor (β_1), the input DC level (V_{G1}), and the threshold voltage (V_{TH1}) are constant. Therefore, in order to express Eq. (4) with V_C and V_{DS1}, V_{S1} should be expressed with V_C, V_{DS1}, and other constant values:

$$V_{S1} = (V_C - V_{dsat3} - V_{TH3}) - V_{DS1}. \quad (5)$$

By replacing V_{S1} in Eq. (4) with Eq. (5), V_{DS1} is expressed as

$$V_{DS1} = (V_C - A) \pm \sqrt{(V_C - A)^2 + B}$$
$$(A = V_{G1} + V_{dsat3} - V_{TH1} + V_{TH3}, B = 2I_{M1,Triode} / \beta_1) \quad (6)$$

where V_{G1}, V_{dsat3}, V_{TH1}, V_{TH3}, $I_{M1,Triode}$ and β_1 are constants in the same bias condition. Now, we notice that V_{DS1} is the only function of V_C. Then, Eq. (6) can be simplified using Taylor series approximation as Eq. (7).

$$V_{DS1} = e^{(V_C - A)/\sqrt{B}} \quad (7)$$

$$A_V = \beta_1 \cdot R \cdot e^{(-A)/\sqrt{B}} \cdot e^{V_C/\sqrt{B}} = K \cdot e^{V_C/\sqrt{B}} \quad (8)$$

If the input transistors operate in triode region and as long as ($V_C - A$) is small, the amplifier structure in Fig. 1 will have inherently dB-linear characteristic without additional exponential function generation block.

Fig. 2 illustrates the gain versus control voltage (V_C) in log scale based on Eq. (3) and Eq. (6). It proves that V_{DS1} changes quite exponentially for a certain range
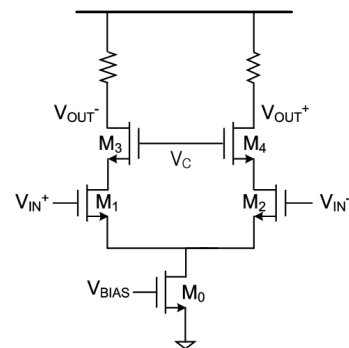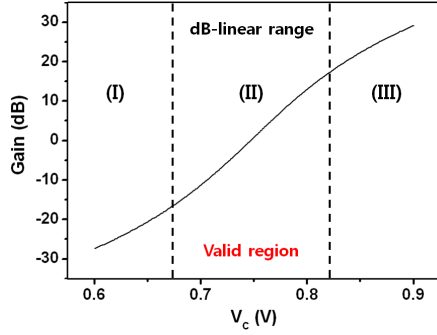

Fig. 1. VGA cell.

Fig. 2. MATLAB simulation of V_C vs. V_{DS1}.

Fig. 4. V_C vs. Gain (Simulation results of VGA cell).

(region (II)) of V_C. Though Eq. (6) reveals the V_{DS1} behavior (and thus the gain behavior, too) depending on A and B, the graph of Eq. (6) will clearly demonstrate it. Fig. 3(a) and (b) present that control voltage versus gain curve can be varied by changing the variable A and B, respectively. The range of the gain can be shifted by adjusting A while the slope of the gain curve (i.e. the achievable gain range) changes by B. As shown in Eq. (6), both variables, A and B are controllable and, thus, we can design the cascode VGA cell in Fig. 1 to have dB-linear gain characteristic with desirable control voltage and gain. Thus, inherently dB-linear property is obtained
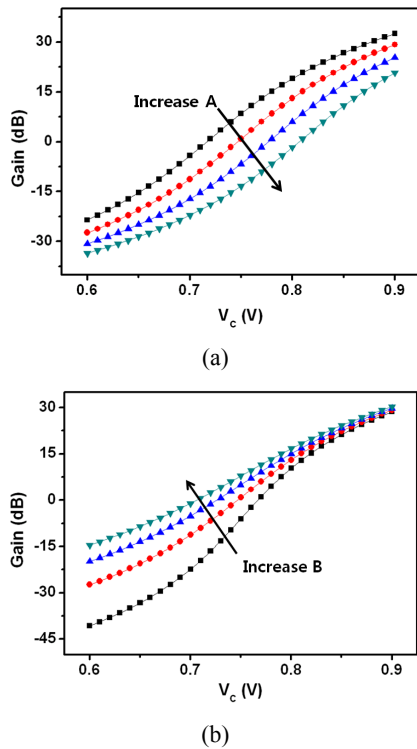
from a simple cascode amplifier in the region (II).

Fig. 4 shows the transistor-level simulation result of the single stage VGA cell in Fig. 1 to verify its dB-linear characteristic. The controllable gain range of the single stage VGA cell is from -17 dB to 6 dB within ±0.6 dB gain step error.

Quantitative analyses with Eqs. (1-8) have assumed that the input transistors operate in triode region and the other transistors operate in saturation region. In the real circuit design, however, as the control voltage increases, the input transistors will gradually enter saturation region and, eventually, the gain no longer depends on V_{DS}. In contrast, as V_C decreases, the source-coupled node also drops (because the input transistors are in triode region) and the current source M_0 is affected by its finite output resistance. Thus, in order for Eq. (8) to be valid, the operation range of transistors must be in their proper region.

III. NON-IDEAL EFFECTS OF CASCODE VGA CELL

Analyses in section II have not counted the variation of mobility, threshold voltage, and bias current on temperature and process variation and other non-ideal effects. For example, the bias condition of transistor might be affected by the body effect and finite output resistance of the current source as the control voltage varies. In this section, we investigate how the dB-linear characteristic of the cascode VGA cell is affected by several representative non-ideal effects.

1. Body Effect

From Fig. 1, we can tell that the drain voltage of the

(a)

(b)

Fig. 3. (a) MATLAB simulation of V_C vs. V_{DS1} according to A, (b) MATLAB simulation of V_C vs. V_{DS1} according to B.
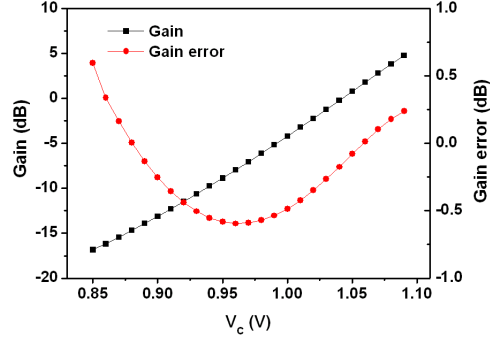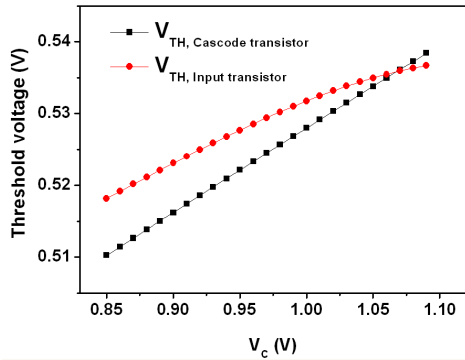
Fig. 5. Body effect of VGA cell.

input transistor pair changes according to V_C, and so does the source voltage of the input transistor. Thus, V_{TH} of input transistor and cascode transistor changes by V_C by the body effect. Fig. 5 shows the simulated threshold voltage of the input transistor (M_1, M_2) and the cascode transistor (M_3, M_4) versus the control voltage (V_C). The threshold variation ranges of the input transistor and cascode transistor are 18 mV and 28 mV, respectively by the body effect. The constant A in Eq. (6) includes the threshold voltages of input transistor and cascode transistor (V_{TH1} and V_{TH3}). Because threshold change direction of both NMOS transistors is the same and difference between the two threshold voltages (V_{TH3} - V_{TH1}) affect the gain equation, the dB-linear gain property is not significantly affected by the V_{TH} variation.

The gain of the circuit in Fig. 1 was simulated with and without body effect in input and cascode transistors. Fig. 6 shows the simulated VGA gain and gain error versus control voltage. In both cases, the linear-in-dB control range is about 23 dB, and the gain error is in the
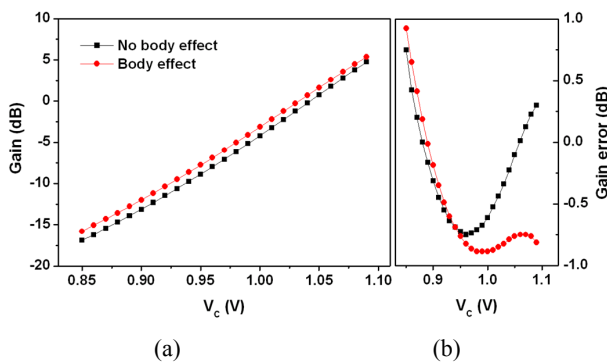
range of ±0.6 dB without body effect and ±0.7 dB with body effect. From the simulation, it appeared that the threshold voltage of input transistor which operates in triode region is more affected by the body effect than the threshold voltage of cascode transistor. Thus, V_{DS} of the input transistor increases slightly by the body effect and the gain of VGA increases. Therefore, the gain curve including body effect is slightly shifted up along the y-axis. Nevertheless, the body effect was turned out to be insignificant in our design, as expected.

2. Finite Output Impedance of Current Source

Fig. 7 shows the simulated VGA gain and gain error versus control voltage according to the gate length of the current source for verifying effect of finite output impedance of the current source. By adjusting the length of M_0 in the schematic of Fig. 1, we can verify how the output impedance of the current source affects dB-linear characteristic. Due to the structural characteristic of the cascode VGA, drain voltage of current source decreases as the control voltage decreases and, thus, the bias current might be reduced because of the finite output impedance of current source. Thus, the gain slope slightly reduces as the control voltage reduces. This behavior is also expected from Eq. (6) and Fig. 3(b). $I_{M1,Triode}$ in B change the slope of gain curve at low gain mode.

Nevertheless, the gain error compared to the ideal dB-linear gain curve does not exceed ±0.6 dB for all cases with gate-length of 0.26 μm, 0.39 μm, and 0.52 μm as shown in Fig. 7. In this design, the length of the current source has been designed to be 0.39 μm for stable design.

(a)　　　　　　　　　(b)

Fig. 6. (a) Gain vs. V_C, (b) Gain error vs. V_C according to body effect.
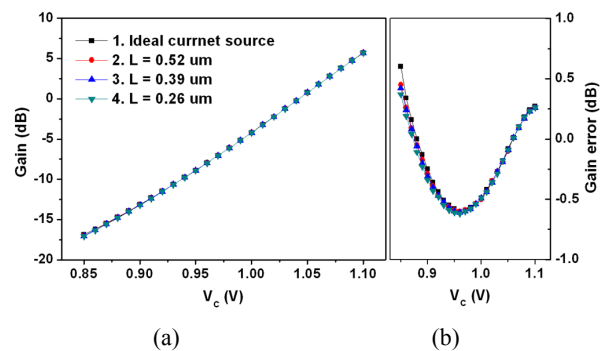

(a)　　　　　　　　　(b)

Fig. 7. (a) Gain vs. V_C, (b) Gain error vs. V_C according to L of current source.

3. PVT Variation Effect on DB-linear Characteristic

DB-linear characteristic of cascode VGA cell will be affected by process corner, supply voltage, and temperature (PVT) variations Table 1 shows how threshold voltage and mobility are affected by process and temperature variation. It shows that the threshold voltage is affected by the process variation more while the mobility is more depends on the temperature. From Eq. (6), we know that threshold voltage change affects the variable A by $V_{TH3} - V_{TH1}$. Because both V_{TH1} and V_{TH3} are the threshold voltages of NMOS, their variations by process and temperature are canceled out and the effect on the dB-linear characteristic is not significant as shown in Fig. 8. Gain error is less than ± 0.7 dB each corner within the almost the same control voltage range.

On the other hand, the variable B in Eq. (6) is directly affected by the process and temperature variation because of β_1. Because the mobility is strongly affected by the temperature variation than the process, the dB-linear characteristic of cascode VGA cell is more affected by temperature variation, and Fig. 9 depicts it.

Since the variable B in Eq. (6) is inversely proportional to mobility, the slope of gain versus control voltage increases as B decreases. Because not only mobility but also V_{TH} and V_{dsat3} change according to temperature

Table 1. Mobility and threshold variation

	Process variation (@ 27°)			Temperature variation (@TT)		
	FF	TT	SS	-25	27	100
Mobility (Normalize)	1.04	1	0.90	1.31	1	0.71
V_{TH}	-60mV	0	+60mV	+20mV	0	-30mV

(a)   (b)

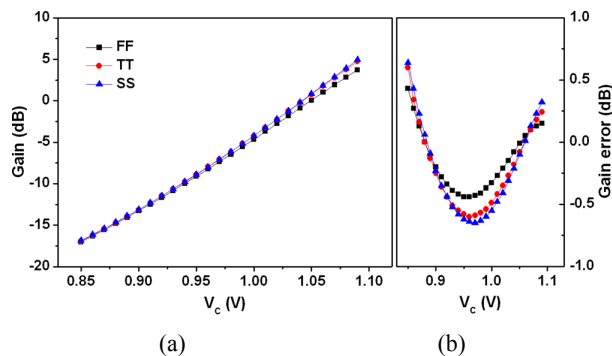**Fig. 8.** (a) Gain vs. V_C, (b) Gain error vs. VC according to process variation.

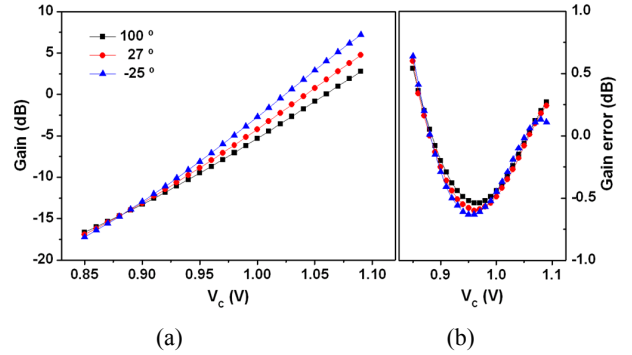(a)   (b)

Fig. 9. (a) Gain vs. V_C, (b) Gain error vs. V_C according to temperature variation.

variation, the gain curve in Fig. 9 is slightly different Fig. 3(b), but direction of slope change is consistent with analysis of section II. As shown in Fig. 9, even though the slope of the gain versus control voltage varies according to temperature variation, the linearity error of gain curve is not affected much. In other words, the gain curve does vary with temperature variation, however, the temperature variation does not affect dB-linear characteristic of the cascode VGA cell. As can be seen in Fig. 9, gain error is less than ± 0.7 dB within control voltage range at each temperature condition.

IV. CIRCUITS IMPLEMENTATION

Based on the studies discussed in Section II, a two-stage VGA was designed as shown in Fig. 10. Simple source-follower configured level-shifter is inserted between the two VGA stages for proper operating condition. A DC offset cancellation loop is composed of an active-RC low-pass filter and a transconductance cell, and the designed lower 3 dB frequency is 260 KHz.

In the prototype, two identical folded-cascode amplifiers are used for VGA cells to achieve wide signal swing and higher gain by using large load resistance. Owing to using only resister as output load without inductive peaking technique [8, 11], we can obtain flat frequency response and compact design without using common mode feedback (CMFB) circuits. As can be seen section III-1, since the body effect does not affect dB-linear characteristic of cascode VGA structure, VGA was designed simply without using deep N-well process. Since we have found that dB-linear characteristic of the cascode VGA is not much affected by the temperature and process variation in section III-3, the VGA does not
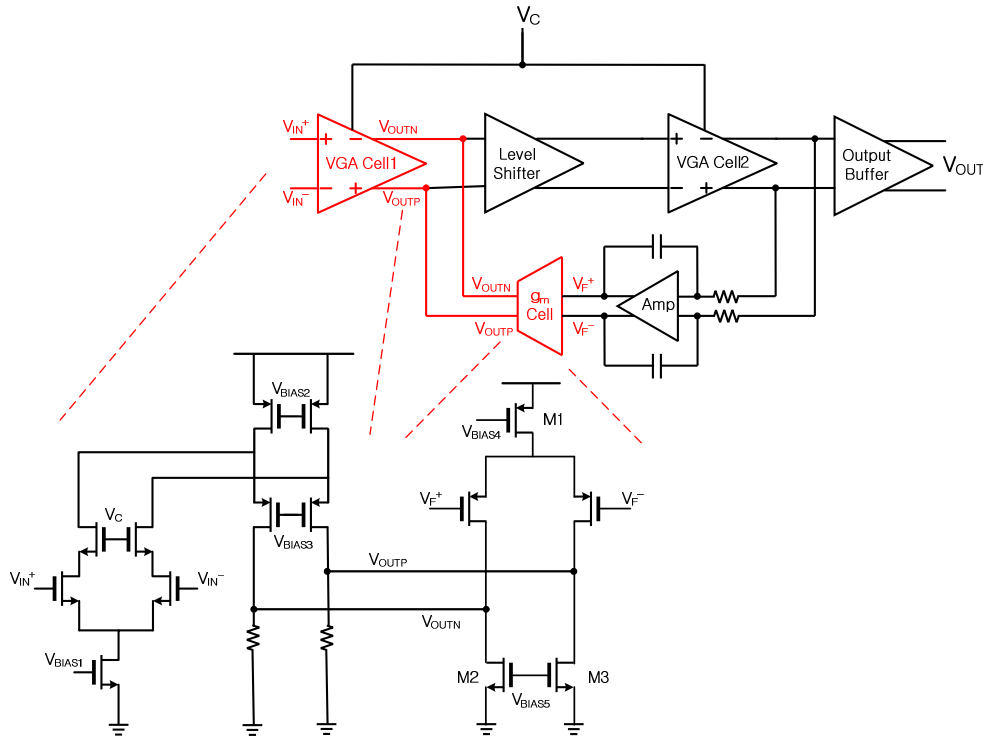
Fig. 10. Block diagram of the overall VGA.

have compensation circuits for process and temperature variation. All the design directions explained so far gives very compact VGA structure.

V. MEASUREMENT RESULTS

The prototype VGA was fabricated in a 0.13 μm CMOS technology for 1.2 V supply voltage. The chip photo is shown in Fig. 11. The entire VGA occupies only 0.06 mm^2 active area owing to the simple structure.

Fig. 12 shows a measured gain control characteristic of the overall VGA. While the control voltage (V_C) varies from 0.66 V to 1.02 V, the gain changes in the range of 60 dB; from -32 dB to +28 dB. The gain linearity error in dB scale is shown in the Fig. 13. The gain linearity error is within ±0.4 dB. This result shows that the cascode VGA has superior dB-linear characteristic. Fig. 14 shows the frequency response of the VGA for different gain setting. It shows quite flat gain over wide band of 630 MHz at the highest gain mode. Fig. 15 shows the measured IIP3 at the gain condition of 3 dB and 20 dB, and the values are 4 dBm and -4 dBm, respectively. The total power consumption including the output buffer is 20.4 mW. The VGA core except for the buffer consumes
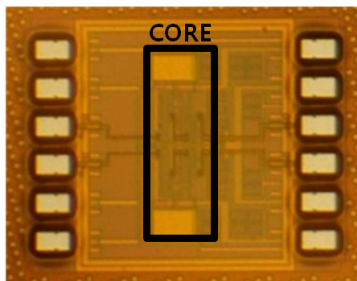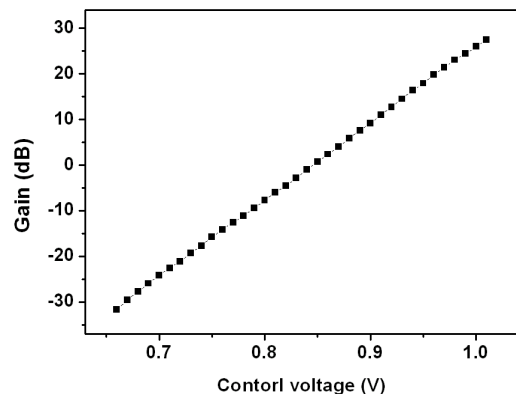

Fig. 11. Chip photo.

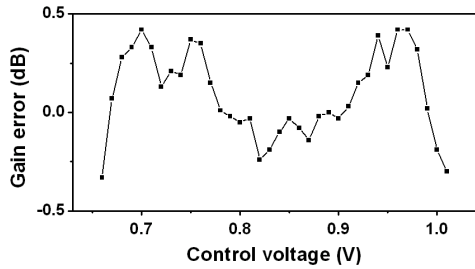**Fig. 12.** Measured control voltage vs. Gain.

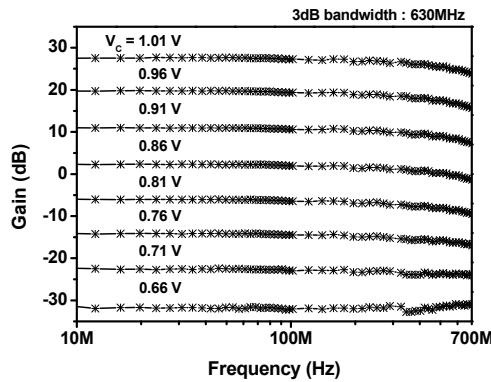**Fig. 13.** Measured control voltage vs. Gain error.

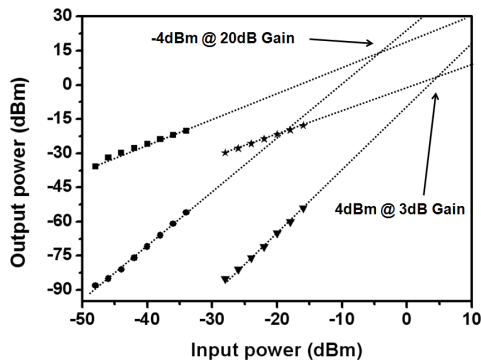**Fig. 14.** Measured frequency response for various gain modes.

Fig. 15. Measured IIP3 at 300 MHz.

16.8 mW. The simulated noise figure at the highest gain mode was 15 dB, which is moderate result compared with previous works [5].

Table 2 compares the performance of this work with previously reported VGAs. While [11] achieves 74 dB gain control range with 3 gain stages and ±1.8 dB linearity error, this design showed 60 dB gain range from a two-stage design and ±0.4 dB linearity error. Due to the optimized design for cascode VGA through qualitative and quantitative analyses, the gain range per one stage is extended and has more accurate dB-linear characteristic compare to [11]. The VGA core area is the smallest among referenced papers. Moreover, the bandwidth of VGA is the widest next to the paper [11].

VI. CONCLUSIONS

This paper introduced an inherently dB-linear VGA cell and analyzes its behavior. Based on the studies, this work's VGA achieves accurate dB-linear characteristic, size competitive design and wide signal bandwidth with relatively low power consumption.

ACKNOWLEDGMENTS

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Table 2. Performance comparison

Reference	[4]	[5]	[6]	[7]	[9]	[9]	[11]	*This work*
Year	2006	2002	2007	2000	2003	2006	2006	
Publish	ASSCC	VLSI	ASSCC	EL	EL	TCAS I	EuMC	
Technology [μm]	0.25	0.25	0.18	0.35	0.18	0.18	0.18	**0.13**
Core area [mm²]	-	2.02	-	0.38	0.18	0.4	0.12	**0.06**
Total power [mW]	74.6	63.3	22.0	32.4	5.4	6.5	23.0	**20.4**
Bandwidth [MHz]	100	280	400	200	350	32	950	**630**
Gain range [dB]	8 ~ 48	-70 ~ 11	-30 ~ 54	-50 ~ 50	-42 ~ 42	-52 ~ 43	-25 ~ 49	**-32 ~ 28**
Number of stages	1	3	2	3	3	2	3	**2**
Gain error [dB]	-	± 3	± 2	-	-	± 1	± 1.8	**± 0.4**

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