Optical Failure Analysis Technique in Deep Submicron CMOS Integrated Circuits

Sunkwon Kim*, Hyongmin Lee*, Hyunjoong Lee*, Jong-Kwan Woo*, Junho Cheon*, Hwan-Yong Kim, Young June Park*, and Suhwan Kim***

Abstract—**In this paper, we have proposed a new approach for optical failure analysis which employs a CMOS photon-emitting circuitry, consisting of a flip-flop based on a sense amplifier and a photon-emitting device. This method can be used even with deep-submicron processes where conventional optical failure analyses are difficult to use due to the low sensitivity in the near infrared (NIR) region of the spectrum. The effectiveness of our approach has been proved by the failure analysis of a prototype designed and fabricated in 0.18 μm CMOS process.**

Index Terms—**Circuit testing, deep submicron CMOS technology, failure analysis, photon emission, picosecond imaging circuit analysis (PICA)**

I. INTRODUCTION

Due to the increasing complexity of circuits and the shrinking of process technologies, the potential types of failure become more varied, making failure analysis more difficult. Many techniques have been used to analyze failures in circuits. Active metal probing is widely used to acquire internal voltages as a basis for analysis, but there are limitations on the size and position of the metal line that can be contacted. The focused ion beam (FIB) is capable of drilling to the metal line of interest from the front or backside of the chip [1]. However, FIB is very time-consuming, since the target locations are often obscured by other lines or by transistors. More significantly, FIB locally alters the electrical properties of transistors. More recently, photon-emission microscopy (PEM) has been introduced for analyzing failures in semiconductor circuits [2]. PEM is reliable and the results are easy to interpret, but it is ineffective in diagnosing timing-related defects. Timing problems can be analyzed by a picosecond integrated circuit analyzer (PICA) [3, 4]. The device is capable of acquiring timing information about internal nodes with a resolution of around 10 ps. However, smaller devices and lower supply voltages of deep submicron technology challenge the PICA technique, due to its lack of sensitivity in the near infrared (NIR) region of the spectrum [5].

We present a new optical approach of failure analysis with sequential circuit that is designed and fabricated in a standard CMOS process and that emits photons based on the PEM concept. In this method, the limits due to deep submicron technologies are overcome by enough photon-emitting time that alleviates the lack of sensitivity in the NIR region. Its quick and effective diagnosis and localization of defects has been proved by the measurement of a prototype designed and fabricated in 0.18 μm CMOS process.

II. BACKGROUND OF OPTICAL FAILURE ANALYSIS

1. Laser Stimulation Techniques

The use of a laser beam to perturb a device-under-test (DUT) while monitoring its behavior was explored and

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developed in the 1980s and 1990s. However, existing techniques are largely restricted to measuring changes in DC voltage levels in the DUT, and are therefore often called static laser stimulation. These methods include light-induced voltage alternation (LIVA) [6], thermally-induced voltage alternation (TIVA) [7], and optical-beam-induced resistance change (OBIRCH) [8]. LIVA is based on photoelectric laser stimulation (PLS), whereas TIVA and OBIRCH are based on thermal laser stimulation (TLS). LIVA images are produced by monitoring the fluctuations in voltage across a constant-current power supply while a laser beam is scanned over the IC. LIVA is highly selective in localizing defects. TIVA and OBIRCH are based on variations in resistance caused by the heat produced when a laser beam irradiates a metal interconnection or a contact via. The effects of this change in resistance on the power demand of the entire IC are used to produce an image.

2. Photon Emission Microscopy (PEM)

PEM is a well-known method of localizing faults in integrated circuits, which is still in development for the defect localization [9]. PEM is based on hot electron emission, which is the intrinsic nature of transistors when current is flowing, and thus is non-invasive and does not alter the electrical properties of the DUT.

Fig. 1 shows how the electrons flowing through an NMOS channel experience an intense electrical field that heats some of these electrons to high energies. In the channel region near the drain, a hot electron causes two distinct effects: the generation of an electron-hole pair by impact ionization and the emission of a NIR photon with energy of about 1.5 eV [10]. This luminescence provides the basis of PEM. The emission intensity N_{PH} is dependent on various parameters, as follows:

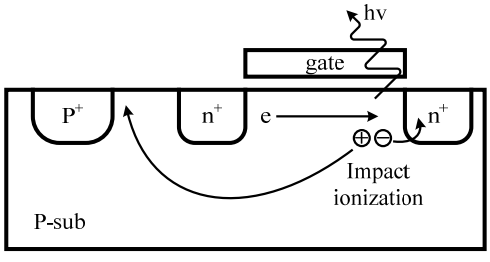

Fig. 1. Hot electron emission and bulk current mechanisms.

$$N_{PH} = A \cdot I_S \cdot \left(V_{DS} - V_{DSsat}\right) e^{-\frac{B}{V_{DS} - V_{DSsat}}}, \qquad (1)$$

where I_S is the source current, V_{DS} is the drain-source voltage, and V_{DSsat} is the drain-source saturation voltage. The parameter A is simply a scale factor, and the second parameter B depends on the MOSFET structure and fabrication technology [11].

PEM is very useful for finding defective locations in non-uniform quiescent or standby mode. In such a mode, current should not flow in a circuit, and therefore hot electron emission should not occur. In a faulty device, however, there is an unwanted current flow, which will induce faint light emission that can be detected by PEM. Light-emitting spots can be pinpointed by overlaying an image of the photon emission on to an image of the IC chip in reflected light. However, since PEM needs to accumulate the NIR luminescence over a significant period, timing information cannot be acquired. Therefore, PEM cannot be used to detect timing-related faults.

3. Picosecond Imaging Circuit Analysis (PICA)

To resolve this drawback, the PICA was developed by Kash and Tsang [3]. The PICA technique is also based on the collection of NIR light emitted from the channel of a CMOS transistor during switching transistors of individual gates. This technique has been proved invaluable for detecting timing-related faults in circuits. It has been extensively utilized to measure propagation delays, clock skews, pulse widths, and slopes.

The photons escape through the substrate of the DUT and are captured by an infrared detector, which records their time of arrival as well as the position on the chip from which they originated as shown in Fig. 2. The resulting images integrate the emissions of all the switched devices in the field of view of the detector. A defect can then be localized visually (by observation if one device appears to perform differently from others) or by extracting the optical waveform (number of photons as a function of time) for a particular device and comparing it to a faultless device, or to a golden model. Extensions of this technique, based on the detection of light emission due to the off-state leakage current (LEOSLC), oxide tunneling current and carrier recombination, have also appeared. However, continuing

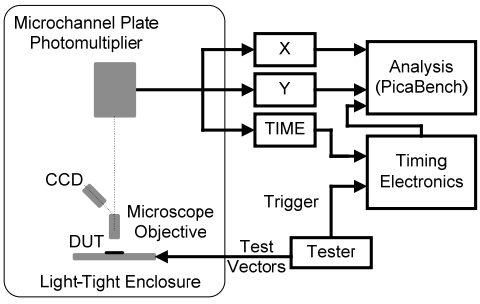

Fig. 2. Basic layout of a PICA tool, showing the microscope used for navigation, the infrared detector, the tester clock and timing electronics.

trend in the semiconductor industry towards smaller devices and lower supply voltages rapidly reduces the effectiveness of PICA, due to the difficulty in achieving adequate sensitivity to the NIR region of the spectrum.

III. Proposed Photon-Emitting Sequential Circuits

Fault detection by optical failure analysis systems becomes more difficult as the technology processes are scaled down to deep submicron (DSM). The system itself such as PEM and PICA may be improved to solve this DSM problem, but it results in cost increase and more complex systems. Another way to approach the problem, as proposed in this paper, is to overcome the limits due to deep submicron technologies by using the simple conventional PEM systems with photon-emitting circuitry assistance.

Most electronic systems contain three types of components: digital logic, memory blocks, and analog or mixed-signal circuits. There are specific design-for-test (DFT) techniques for each type of component: boundary scanning is the most commonly used DFT technique for logic; built-in self-test (BIST) is widely applied to memory; and an analog test bus is used when non-digital elements are present. Among them, scanning was introduced by Williams and Angell [12]. It adds a test mode to the circuit, in which all the sequential circuits such as flip-flops function as shift registers. Then, all the flip-flops can be set to a desired state by loading the corresponding bit pattern into the shift register. Similarly, the updated state of the flip-flops can be observed by reading the bit pattern of the corresponding shift register.

By modifying the sequential components of the circuits to have additional optical features, the concept of DFT with scan can be applied to the optical failure analysis system. In this way, the simple, conventional PEM system can be applied to circuits fabricated in deep submicron CMOS technologies.

When a CMOS gate switches state, transient current flows, and both the NMOS and the PMOS transistors are briefly saturated, which generate photons; but under static conditions, a conventional flip-flop draws no current and there is no observable optical emission. This is why it is not possible to read values stored in sequential circuits using PEM. But this situation can be changed if we augment a sequential circuit with an element that emits photons all the time when the circuit is in a particular state. We therefore propose a SAFF-e, consisting of a sense-amplifier-based flip-flop (SAFF) and a photon-emitting element. The photon-emitting part of the proposed circuit does not output the instantaneous value generated by combinational logic circuits, but outputs the value held by the flip-flop, which is a sequential circuit. This allows PEM to acquire data under static conditions. Hence enough photon-emitting time in the test mode alleviates the difficulties of the lack of sensitivity in the NIR region.

The SAFF was initially seen in StrongArm110 and is now widely used in high-speed systems [13]. It is composed of a very fast pre-charged sense-amplifier stage followed by a set-reset latch. The photon-emitting element with which we augment a SAFF is made up of an off-switch (M1), a driver (M2), and a photon-emission cell (M3). M1 prevents additional power consumption when the chip is in normal operation mode. M2 switches on and off according to the output value nQ of the SAFF, connecting either VDD or high impedance to the drain of the photon emission cell. The photon emission rate of the M3 is determined by the gate voltage (V_g) and the drain voltage (V_d). For example, if the value stored in the SAFF is logical ‘1’, then nQ is ‘0’. In photon-emitting test mode, M1 is turned on and M2 is also turned on since nQ is ‘0’. M3 will then emit photons at a rate determined by V_g. In other words, if the value in the SAFF is logical ‘1’, M3 will light up. Thus the value stored in our SAFF-e structure, shown in Fig. 3, can be traced by PEM in the static condition, and not only when the CMOS is switching but also when in static condition. In normal operation mode, the photon-emitting element

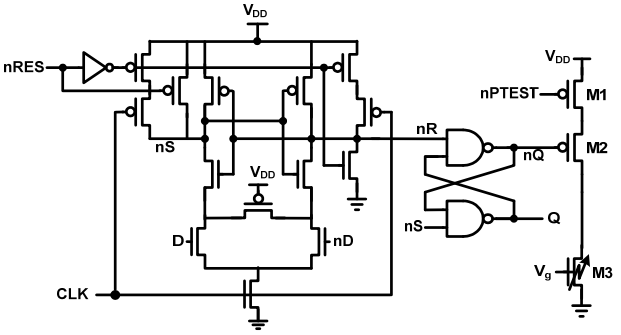

Fig. 3. Photon-emitting flip-flop (SAFF-e) with reset.

of the SAFF-e is completely turned off.

IV. Experimental Results

To assess the effectiveness of our optical failure analysis technique, we designed a 16-bit arithmetic and logic unit (ALU) and fabricated it in 0.18 μm CMOS bulk technology. As shown in Fig. 4, the ALU is connected to two built-in logic block observers (BILBOs) and a 16-bit multiple-input signature register (MISR). Each BILBO provides the ALU with different values. The MISR decides whether the chip passes or fails the test, which depends on the output of the ALU and the previous state of the MISR.

All of the internal SAFF-e states are monitored using the PHEMOS-1000 emission microscope shown in Fig. 5. The states of the SAFF-e circuits in the BILBO logic can be read when these circuits are emitting. Fig. 6(a) shows the environment that we used for the testing of the SAFF-e concept, and (b) is the microphotograph of the

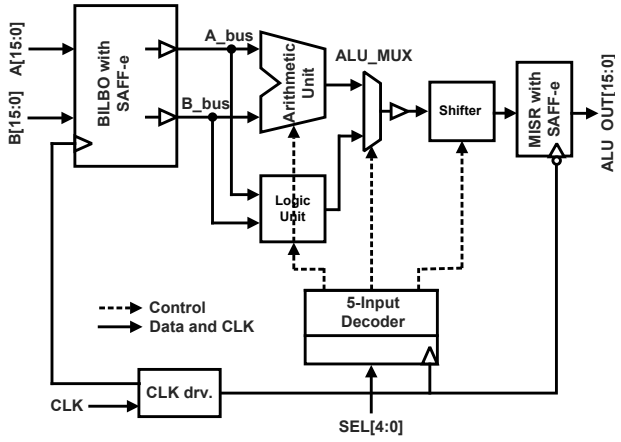

Fig. 4. A 16-bit ALU with logic sub-blocks and photon-emitting flip-flops (SAFF-e).

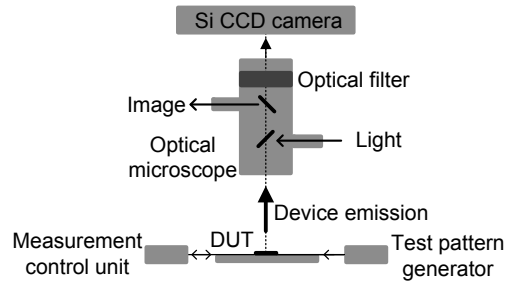

Fig. 5. Optical failure analysis setup with PHEMOS-1000.

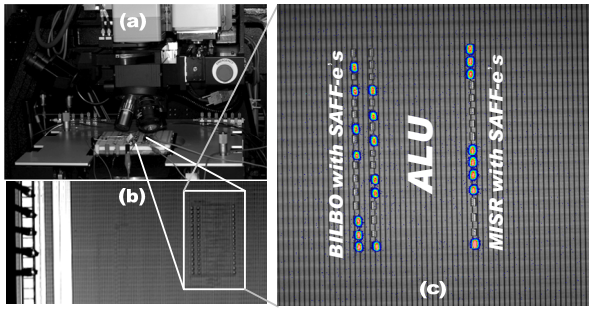

Fig. 6. (a) Optical failure analysis setup, (b) Microphotograph of the test chip and (c) Photon-emission image of the static state of a 16-bit ALU. The BILBO outputs are seen to be both 0 x E14 A and 0 x 8CA8 and the value of the MISR is 0 x 8F08.

test chip. Fig. 6(c) shows a photon-emission image overlaid on the microphotograph.

As shown in Fig. 6, the BILBO outputs are both 0 x E14 A and 0 x 8CA8, and are connected to ALU inputs. Arithmetical operation of the ALU generates the output from these input values. Finally, the value of MISR, which is determined by both the output of the ALU and the previous state of the MISR, is 0 x 8F08. As shown in experimental results, it can monitor all the stored values at every cycle, and can easily detect the fault location even if a circuit is deeply embedded in a chip.

V. Conclusions

We have proposed a new approach for optical failure analysis which employs a CMOS photon-emitting circuitry, consisting of a flip-flop based on a sense amplifier and a photon-emitting device. It allows the states of all the internal flip-flops, deeply buried inside a chip, to be monitored every cycle in a contactless and non-invasive way. This method can be used even with deep-submicron processes where conventional optical failure analyses are difficult to use due to the low

sensitivity in the near infrared (NIR) region of the spectrum. The photon-emitting device is designed not to consume power when an optical output is not required. The effectiveness of our approach has been proved in the failure analysis of a prototype implemented in 0.18 μm CMOS process.

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REFERENCES

[1] C. Boit, R.Schlangen, U.Kerst, and T.Lundquest, "Physical Techniques for Chip-Backside IC Debug in Nanotechnologies," *IEEE Design & Test of Computers*, 2008, pp.250-257.

[2] C. Boit, ''Fundamentals of Photon Emission (PEM) in Silicon- Electroluminescence for Analysis of Electronic Circuit and Device Functionality,'' *Microelectronics Failure Analysis Desk Reference, 5th ed., ASM Int'l*, pp.356-368, 2004.

[3] J. A. Kash and J. C. Tsang, "Dynamic Internal Testing of CMOS Circuits Using Hot Luminescence," *IEEE Electron Device Lett.*, Vol.18, No.7, pp.330-332, 1997.

[4] J. Tsang, J. Kash, and D. Vallett, "Picosecond Imaging Circuit Analysis," *IBM J. Res. Develop.*, 44(4) pp.583-603 , 2000.

[5] F. Stellari, A. Tosi, F. Zappa, and S. Cova, "CMOS circuit testing via time-resolved luminescence measurements and simulations," *IEEE Trans. Instrum. Measur.*, Vol.53, No.1, pp.163-169, Feb., 2004.

[6] E. I. Cole Jr., J. M. Soden, J. L. Rife, D. L. Barton, and C. L. Henderson, "Novel Failure Analysis Techniques Using Photon Probing in a Scanning Optical Microscope," *Proc. International Reliability Physics Symposium (IRPS)*, pp.388-398, Apr., 1994.

[7] E. I. Cole Jr., P. Tangyunyong, D. A. Benson, and D. L. Barton, "TIVA and SEI Developments for Enhanced Front and Backside Interconnection Failure Analysis," *Proc. European Symposium on Reliability of Electron Devices (ESREF)*, pp.991-996, Oct., 1999.

[8] K. Nikawa and S. Inoue, "New Capabilities of OBIRCH Method for Fault Localization and Defect Detection," *Proc. Sixth Asian Test Symposium (ATS)*, pp.214-219, Jul., 1997.

[9] W. Chunlei, L. Zhai, W. Wang, G. Song, L. Jinglong, Y. Joe, and M. Motohiko, "Defect Localization Using Photon Emission Microscopy Analysis with the Combination of OBIRCH Analysis," *17th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, pp.1-6, 2010.

[10] F. Stellari, F. Zappa, S. Cova, and L. Vendrame, "Tools for non-invasive optical characterization of CMOS circuits," *IEDM Tech. Dig.*, pp.487-490, 1999.

[11] A Tosi, A Dalla Mora, F Pozzi, and F Zappa, "Modeling and Probing Hot-Carrier Luminescence From MOSFETs," *IEEE Electron Device Lett.*, Vol.29, No.4, Apr., 2008.

[12] Michael J.Y. Williams and James B. Angell, "Enhancing Testability of Large-Scale Integrated Circuits via Test Points and Additional Logic," *IEEE Trans. Comput.*, Vol.22, No.1, pp.46-60, Jan., 1973.

[13] M. Matsui, H. Hara, Y. Uetani, L. Kim, T. Nagamatsu, and et al., "A 200 MHz 13mm^2 2D DCT macrocell using sense-amplifying pipeline flip-flop scheme," *IEEE J.Solid-State Circuits*, Vol.29, No.12, pp.1482-1490, Dec., 1994.

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