

Dependency of Tunneling Field-Effect Transistor (TFET) Characteristics on Operation Regions

Min Jin Lee and Woo Young Choi

Abstract—In this paper, two competing mechanisms determining drain current of tunneling field-effect transistors (TFETs) have been investigated such as band-to-band tunneling and drift. Based on the results, the characteristics of TFETs have been discussed in the tunneling-dominant and drift-dominant region.

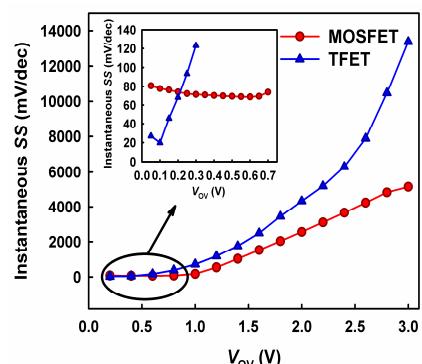
Index Terms—Tunneling field-effect transistor, band-to-band tunneling, drift, tunnel resistance, channel resistance

I. INTRODUCTION

A TFET is considered as one of the most promising candidates to replace a MOSFET. It is because the subthreshold swing (SS) of the TFET can be smaller than 60 mV/dec at room temperature, which is the physical limit of the MOSFET [1-4]. However, the TFET has suffered from smaller on current (I_{ON}) than the MOSFET at the same channel length (L_{CH}). It is originated from the fact that the SS of the TFET is a function of the gate voltage (V_{GS}) unlike that of the MOSFET [2] and the physical reason is the large tunneling barrier. Fig. 1 shows that the TFET has a smaller instantaneous SS than the MOSFET at low overdrive voltage (V_{OV}). V_{OV} is defined as the difference between V_{GS} and threshold voltage (V_T). In this work, V_T of TFETs is defined as V_{GS} when drain current (I_{DS}) is 10^{-15} A/ μ m. However, at high

V_{OV} , the instantaneous SS of the TFET increases more abruptly than that of the MOSFET. It is problematic in that I_{ON} of the TFET cannot exceed that of the MOSFET.

Fig. 2 compares the on resistance (R_{ON}) of the MOSFET and TFET. The R_{ON} of the MOSFET consists of source resistance (R_S), drain resistance (R_D) and channel resistance (R_{CH}). On the other hand, the R_{ON} of the TFET has an additional tunnel resistance (R_{TUN}). R_{CH} is determined by drift mechanism which is related to channel mobility. R_{TUN} is determined by band-to-band tunneling mechanism which is related to the tunneling barrier between the source and channel region. It should be noted that R_{ON} of the TFET has both R_{CH} and R_{TUN} . It means that I_{DS} of the TFET is determined by both drift and band-to-band tunneling while I_{DS} of MOSFETs is determined only by drift mechanism. Thus, it can be inferred that TFETs can have two different operating regions depending on the values of R_{CH} and R_{TUN} . When R_{TUN} is dominant, TFETs are operated in the tunneling-dominant region where band-to-band tunneling determines I_{DS} . When R_{CH} is dominant, TFETs are operated in the



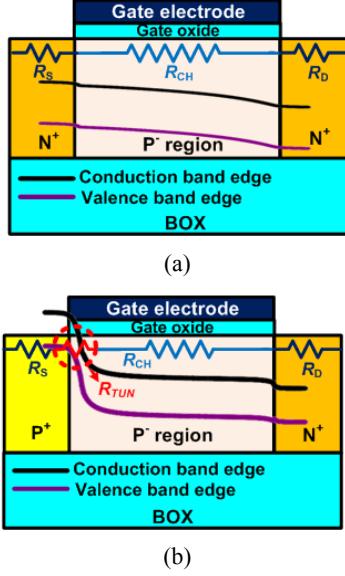


Fig. 2. R_{ON} components of (a) a MOSFET and (b) TFET.

drift-dominant region where drift mechanism determines I_{DS} .

In this paper, we have adjusted R_{TUN} and R_{CH} by performing device simulation in order to investigate the electrical characteristics of tunneling-dominant and drift-dominant TFETs. This paper consists of two parts. First, the extraction method of R_{TUN} , R_{CH} and R_{SD} is explained. R_{SD} is defined as the sum of R_S and R_D . Second, the electrical characteristics of TFETs will be discussed in the tunneling-dominant and drift-dominant region.

II. EXTRACTION METHOD OF R_{ON} COMPONENTS

Single-gate silicon-on-insulator (SOI) TFETs have been simulated by using Silvaco ATLAS [5]. Nonlocal band-to-band tunneling [6], doping and temperature dependent mobility model, band-gap narrowing, Fermi-Dirac and Shockley-Read-Hall recombination model have been used in the simulation. The simulated TFET has a gate oxide thickness of 2 nm, a channel width (W_{CH}) of 1 μm , a buried oxide thickness of 150 nm and an SOI layer thickness of 50 nm. N⁺ poly-Si gate is used. The doping concentrations of the channel (N_B), source (N_S) and drain region (N_D) are 5×10^{17} , 1×10^{19} and $1 \times 10^{19} \text{ cm}^{-3}$, respectively. Quantum mesh has been used at the surface of the SOI layer.

For quantitative analysis, each component of R_{ON} has

been extracted. In the first place, Fig. 3 shows the extraction method of R_{CH} . R_{ON} is plotted by dividing I_{DS} by the drain voltage (V_{DS}) from TFETs with various L_{CH} 's. V_{OV} and V_{DS} are fixed at 1 and 0.1 V, respectively. The line slope in Fig. 3 indicates R_{CH} per L_{CH} (ρ_{CH}). However, the problem of this method is that the line slope is too small to measure because the ratio of R_{CH} to R_{ON} is extremely small. It makes the accurate extraction of R_{CH} difficult. Thus, for higher accuracy, we have decreased channel mobility by a factor of 1, 0.1, 0.05 and 0.01. Those factors are defined as mobility factor (MF) in this paper. It means that R_{CH} increases by a factor of 1, 10, 20 and 100 because R_{CH} is inversely proportional to channel mobility. By adjusting MF , ρ_{CH} can be extracted accurately as shown in Fig. 4.

For example, at the same V_{OV} , when channel mobility decreases by a factor of 10, ρ_{CH} becomes 10x larger. In order to extract the genuine value of ρ_{CH} which is defined as ρ_{CH} when MF is 1, the extracted ρ_{CH} needs to be calibrated by the reciprocal of MF . Fig. 5 shows extracted ρ_{CH} 's with various MF 's. When calibrated by the reciprocal of MF 's, genuine ρ_{CH} 's are located in the

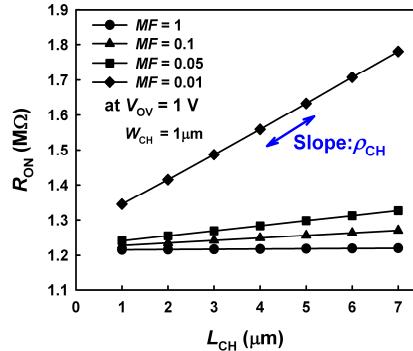


Fig. 3. R_{ON} vs. L_{CH} graph in order to extract R_{CH} .

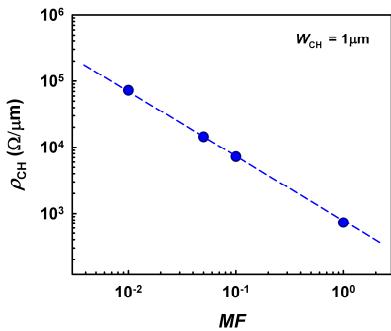


Fig. 4. ρ_{CH} with the variation of MF .

same curve as shown in the inset of Fig. 5. It confirms the validity of the proposed extraction method. Next, R_{SD} is extracted. We use the fact that MF 's affect R_{CH} and R_{SD} regardless of R_{TUN} . Depending on the value of MF , R_{ON} 's are written as

$$R_{ON(MF=1.0)} = R_{CH(MF=1.0)} + R_{SD(MF=1.0)} + R_{TUN} \quad (1a)$$

$$\begin{aligned} R_{ON(MF=0.5)} &= R_{CH(MF=0.5)} + R_{SD(MF=0.5)} + R_{TUN} \\ &= 2R_{CH(MF=1.0)} + 2R_{SD(MF=1.0)} + R_{TUN} \end{aligned} \quad (1b)$$

When Eq. (1a) is subtracted from Eq. (1b), R_{TUN} disappears while R_{CH} and R_{SD} remain as follows:

$$R_{ON(MF=0.5)} - R_{ON(MF=1.0)} = R_{CH(MF=1.0)} + R_{SD(MF=1.0)} \quad (2)$$

R_{SD} is derived as

$$R_{SD(MF=1.0)} = R_{ON(MF=0.5)} - R_{ON(MF=1.0)} - R_{CH(MF=1.0)} \quad (3)$$

Fig. 6 shows that the average value of extracted R_{SD} is 588 Ω and constant regardless of V_{OV} . Also, as V_{OV} increases, R_{CH} decreases, which makes R_{SD} larger than R_{CH} . Finally, R_{TUN} is extracted as follows:

$$R_{TUN} = R_{ON} - R_{CH} - R_{SD} \quad (4)$$

Based on the abovementioned results, we defined intrinsic R_{ON} (R_{ON_int}), which excludes R_{SD} as

$$R_{ON_int} = R_{ON} - R_{SD} = R_{TUN} + R_{CH} \quad (5)$$

Fig. 7 shows R_{ON_int} as a function of L_{CH} for the

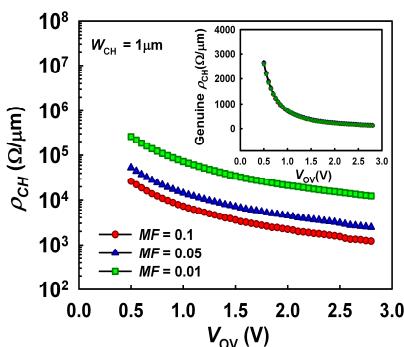


Fig. 5. ρ_{CH} with the variation of V_{OV} at $V_{DS} = 0.1$ V. Also, inset figure shows genuine ρ_{CH} which is calibrated by the reciprocal of MF .

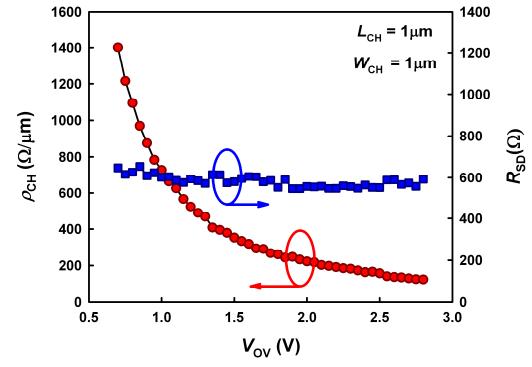


Fig. 6. Comparison of ρ_{CH} and R_{SD} extracted from a 1- μm TFET at $V_{DS} = 0.1$ V.

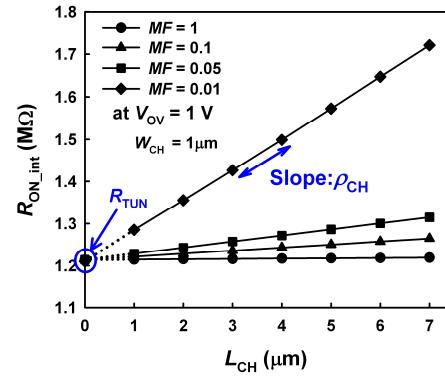


Fig. 7. R_{ON_int} vs. L_{CH} graph in order to extract R_{TUN} .

extraction of R_{TUN} . Unlike Fig. 3, every line meets at one y-intercept which indicates R_{TUN} because MF 's only affect R_{CH} rather than R_{TUN} . In order to confirm the validity, we compared extracted R_{TUN} with theoretical values which is calculated by the following equation [7]:

$$R_{TUN} = A \frac{4\pi^3 \hbar^2 W_{TUN}}{\sqrt{2m^* q^3 \sqrt{E_G}}} \exp\left(\frac{4\sqrt{2m^*} W_{TUN} \sqrt{E_G}}{3q\hbar}\right) \quad (6)$$

where A is constant, q is elementary charge, m^* is electron tunneling effective mass, W_{TUN} is tunneling barrier width, E_G is bandgap energy and \hbar is Dirac constant. For the calculation of theoretical values, As V_{OV} increases, W_{TUN} decreases and its decreasing rate becomes smaller as shown in Fig. 8(a). W_{TUN} have been extracted automatically at each V_{OV} by using device simulation as follows. From the simulated energy band diagrams, the minimum distance between valence band and conduction band has been extracted as shown in inset of Fig. 8(a). A and m^* have been calibrated carefully to fit extracted R_{TUN} with the theoretical value. Fig. 8(b) shows

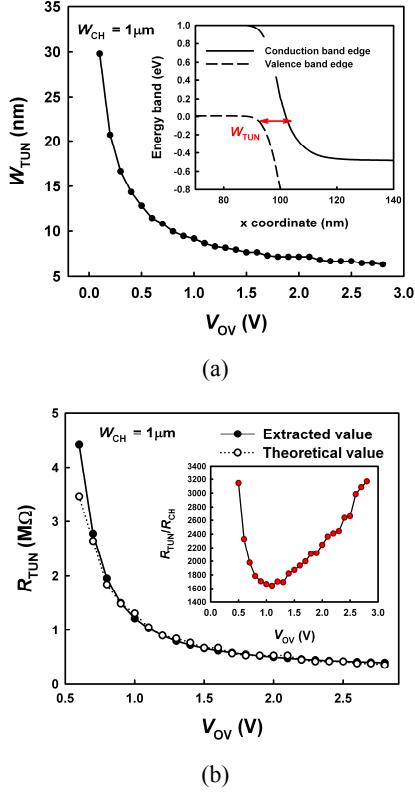


Fig. 8. (a) Extracted W_{TUN} with the variation of V_{OV} at $V_{DS} = 0.1$ V. Inset figure shows the definition of W_{TUN} . (b) R_{TUN} compared with theoretical values and inset figure shows the ratio of R_{TUN} to R_{CH} with the variation of V_{OV} at $V_{DS} = 0.1$ V.

that the extracted R_{TUN} fits theoretical R_{TUN} within 5.4%. Thus, it is confirmed that R_{TUN} is related only to tunneling mechanism rather than drift mechanism.

Although R_{TUN} is not a function of V_{TUN} from Eq. (6), V_{TUN} affects W_{TUN} and R_{TUN} actually. V_{TUN} means the voltage drop across the tunneling junction which is defined as

$$V_{TUN} = \frac{R_{TUN}}{R_{SD} + R_{TUN} + R_{CH}} V_{DS} \quad (7)$$

As MF decreases, R_{CH} increases and V_{TUN} decreases. It increases W_{TUN} and R_{TUN} . In order to further confirm the validity of the extraction method, we have observed ΔV_{TUN} , ΔW_{TUN} and ΔR_{TUN} with the variation of MF at $V_{OV} = 1$ V. Inset of Fig. 8(b) shows the ratio of R_{TUN} to R_{CH} . As shown in inset of Fig. 8(b), the ratio of R_{TUN} to R_{CH} is minimum at $V_{OV} = 1$ V, which is the worst case. V_{TUN} at $MF = 0.01$ is 91% of V_{TUN} at $MF = 1$ as shown in Fig. 9. However, ΔW_{TUN} and ΔR_{TUN} are smaller than ΔV_{TUN} . Because W_{TUN} is nearly saturated at $V_{OV} = 1$ V as

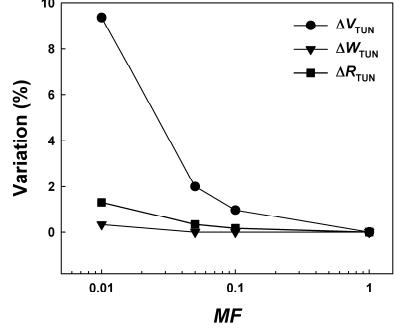


Fig. 9. ΔV_{TUN} , ΔW_{TUN} and ΔR_{TUN} with the variation of MF .

shown in Fig. 8(a), W_{TUN} shows little change with the variation of V_{TUN} . Thus, ΔR_{TUN} is 1% and it confirms the validity of the proposed extraction method.

III. TUNNELING-DOMINANT TFETS VS. DRIFT-DOMINANT TFETS

From now on, the electrical characteristics of TFETs will be investigated in the tunneling-dominant and drift-dominant region. In the first place, tunneling-dominant TFETs will be discussed because most of TFETs from literature are classified into tunneling-dominant TFETs. Simulation conditions of tunneling-dominant TFETs are summarized in Table 1. It is observed that in the case of tunneling dominant TFET, R_{TUN} is ~ 2000 times larger than R_{CH} as shown inset of Fig. 8(b). In the case of tunneling-dominant TFETs, R_{TUN} is a dominant factor determining R_{ON} and instantaneous SS becomes larger as V_{OV} increases. It means that the tunneling-dominant TFET may have lower I_{ON} than the MOSFET even if the former has lower instantaneous SS than the latter at low V_{OV} . The I_{ON} of the TFET is lower than the MOSFET with the

Table 1. Simulation conditions of tunneling-dominant and drift-dominant TFET

	Tunneling-dominant	Drift-dominant
MF	1	1
m^* factor	1	0.15
L_{CH}	1 μm	
Gate oxide thickness	2 nm	
Channel width	1 μm	
Buried oxide thickness	150 nm	
SOI layer thickness	50 nm	
Gate material	N^+ poly-Si	
N_B , N_S and N_D	5×10^{17} , 1×10^{19} and $1 \times 10^{19} \text{ cm}^{-3}$	

same L_{CH} , which due to R_{TUN} rather than R_{CH} because I_{DS} of the tunneling-dominant TFET is determined only by band-to-band tunneling. Fig. 10 shows that I_{DS} matches the tunneling current (I_{TUN}) well which is defined as

$$I_{TUN} = V_{DS} / R_{TUN} \quad (8)$$

As explained in Eq. (6), R_{TUN} is a strong function of W_{TUN} . As V_{OV} increases, W_{TUN} decreases and its decreasing rate becomes smaller as shown in Fig. 8a. It makes R_{TUN} and R_{ON} decrease less abruptly as V_{OV} increases, which causes I_{DS} saturation at high V_{OV} .

Conventional TFETs have suffered from low I_{ON} because they are operated in the tunneling-dominant region. Thus, the best way of boosting I_{ON} is reducing R_{TUN} . Some pioneering research results have been reported for the purpose of low R_{TUN} [3, 8]. As a result, recently, I_{ON} of TFETs have risen at a steady pace [9, 10]. In particular, III-V TFETs may achieve larger tunneling current compared with Si TFETs due to their smaller bandgap energy and smaller electron mass [11, 12]. Further, TFETs with gate-drain overlap structures to suppress ambipolar behavior will have larger R_{CH} than MOSFETs, which makes drift-dominant TFETs more feasible [13]. If R_{TUN} is reduced successfully down to the R_{CH} in the future, TFETs will be operated in the drift-dominant region where I_{DS} is determined by drift mechanism unlike tunneling-dominant TFETs. In the drift-dominant region, TFETs show electrical characteristics similar to MOSFETs. For the investigation of drift-dominant TFETs, m^* has been 1x, 0.8x, 0.6x, 0.4x, 0.2x and 0.15x decreased. Fig. 11 shows that R_{TUN} decreases as m^* factor decreases while inset of Fig. 11 shows that ρ_{CH} is constant regardless of m^* factor. According to

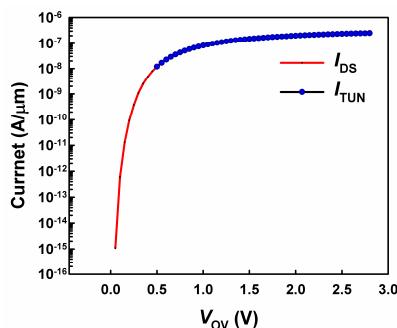


Fig. 10. I_{DS} compared with I_{TUN} of a tunneling-dominant TFET at $V_{DS} = 0.1$ V.

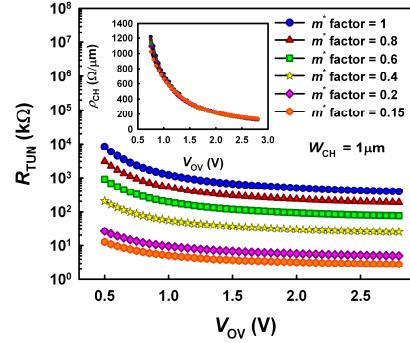
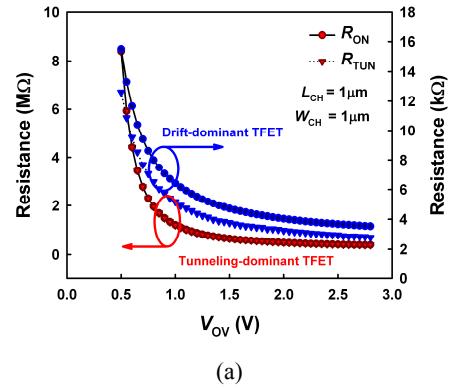


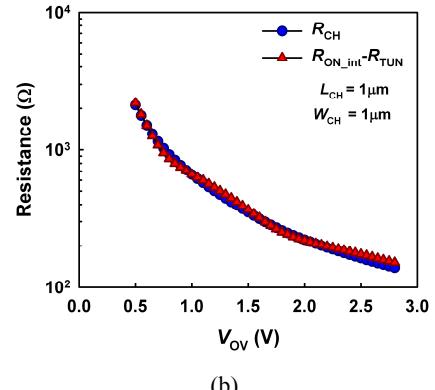
Fig. 11. Extracted R_{TUN} with the variation of m^* . Also, inset figure shows ρ_{CH} of the reference TFET with the variation of m^* .

simulation results, when m^* factor is 0.15, the ratio of R_{TUN} to R_{CH} is ~ 10 . It implies that I_{DS} is greatly affected by drift mechanism. Thus, in this work, the TFET whose m^* factor is less than 0.15 is defined as a drift-dominant TFET as shown in Table 1.

Drift-dominant TFETs are distinguished from tunneling-dominant TFETs in three viewpoints. First, drift-dominant TFETs are dominated by R_{CH} . Fig. 12(a)



(a)



(b)

Fig. 12. Extracted R_{ON} and R_{TUN} (a) in the case of tunneling-dominant and drift-dominant TFETs, (b) Extracted R_{CH} compared with $R_{ON_int} - R_{TUN}$ in the drift-dominant TFETs shown in (a).

compare R_{TUN} with R_{ON} in the case of tunneling-dominant and drift-dominant TFETs. The drift-dominant

TFET shows considerable difference which is equal to R_{CH} as shown in Fig. 12(b). It proves that drift mechanism plays an important role in determining I_{DS} in the case of drift-dominant TFETs. Second, I_{DS} of tunneling-dominant TFETs is independent of L_{CH} while I_{DS} of drift-dominant TFETs is dependent on L_{CH} as shown in Fig. 13. Finally, tunneling-dominant and drift-dominant TFETs show different temperature dependence [14]. Fig. 14 shows that I_{DS} of tunneling-dominant TFETs increases as temperature increases. It is because of E_{G} reduction at elevated temperature. On the other hand, I_{DS} of drift-dominant TFETs decreases as temperature increases. It is because channel mobility is reduced with increasing temperature.

To sum up, currently, the best way of achieving large I_{ON} is the reduction of R_{TUN} because most of TFETs operate in the tunneling-dominant region. However,

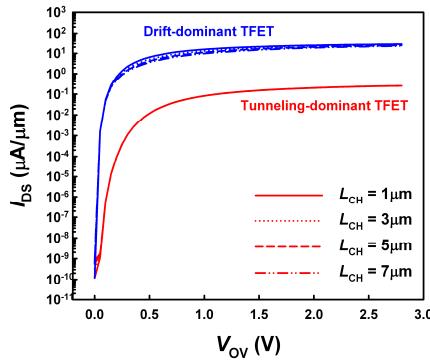


Fig. 13. Dependence of transfer curves on L_{CH} in the case of tunneling-dominant and drift-dominant TFETs.

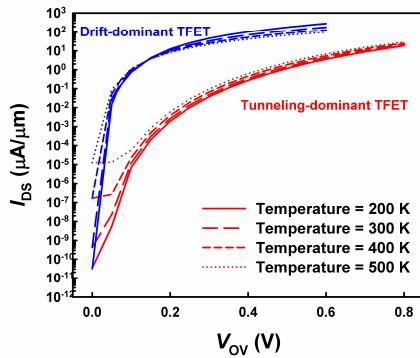


Fig. 14. Dependence of transfer curves on temperature in the case of tunneling-dominant and drift-dominant TFETs at $V_{\text{DS}} = 0.9$ V.

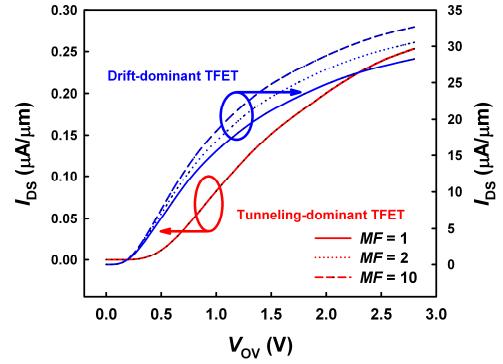


Fig. 15. Improvement of channel mobility in the case of tunneling-dominant and drift-dominant TFETs.

continuous reduction of R_{TUN} makes tunneling-dominant TFETs drift-dominant. Thus, for more I_{ON} boosting of drift-dominant TFETs, higher channel mobility will be necessary as in the case of conventional MOSFETs. Fig. 15 shows that channel mobility has no influence on I_{DS} in the tunneling-dominant TFET. However, in the case of the drift-dominant TFET, I_{ON} is affected by channel mobility.

IV. SUMMARY

The extraction method of R_{CH} and R_{TUN} has been proposed for TFETs. Based on the results, we classified the operation region of TFETs into two categories: the tunneling-dominant and drift-dominant region. In the tunneling-dominant region, because I_{DS} is dominated by R_{TUN} rather than R_{CH} , the instantaneous SS increases with increasing V_{OV} which is related to W_{TUN} saturation. The reduction of R_{TUN} makes tunneling-dominant TFETs drift-dominant. In the drift-dominant region, like MOSFETs, mobility engineering will be necessary for higher I_{ON} .

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REFERENCES

- [1] W. Y. Choi, B.-G. Park, J. D. Lee, T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *Electron Device Letters, IEEE*, Vol.28, No.8, pp.743-745, Aug., 2007.
- [2] Q. Zhang, W. Zhao, A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *Electron Device Letters, IEEE*, Vol.27, No.4, pp.297-300, Apr., 2006.
- [3] V. Nagavarapu, R. Jhaveri, J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: A novel high performance transistor," *Electron Devices, IEEE Transactions on*, Vol.55, No.4, pp.1013-1019, Apr., 2008.
- [4] S. Cho, M-C. Sun, G. Kim, T. I. Kamins, B-G. Park, J. S. H. Jr, "Design optimization of a type-I heterojunction tunneling field-effect transistor (I-HTFET) for high performance logic technology," *Journal of Semiconductor Technology and Science*, Vol.11, No.3, pp.182-189, Sep., 2011.
- [5] *Atlas User's Manual*, Silvaco, Santa Clara, CA, Jul., 2010.
- [6] E. O. Kane, "Theory of tunneling", *J. Appl. Phys.*, Vol.32, No.1, pp.83-91, Jan., 1961.
- [7] R. B. Fair, H. W. Wivell, "Zener and avalanche breakdown in As-implanted low-voltage Si n-p junctions," *Electron Devices, IEEE Transactions on*, Vol.23, No.5, pp.512-518, May, 1976.
- [8] K. K. Bhuwalka, J. Schulze, I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the $\delta p+$ Layer," *Japanese Journal of Applied Physics*, Vol.43, No.7A, pp.4073-4078, Jul., 2004.
- [9] W.-Y. Loh, K. Jeon, C. Y. Kang, J. Oh, P. Patel, C. Smith, J. Barnett, C. Park, T.-J. King, H.-H. Tseng, P. Majhi, R. Jammy, C. Hu, "The sub-60 nm Si tunnel field effect transistors with $I_{on} > 100 \mu A/\mu m$," in *Proc. Eur. Solid-State Device Res. Conf.*, pp.162-165, Sep., 2010.
- [10] H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, J. Lee, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides," *Electron Devices, IEEE Transactions on*, Vol.58, No.9, pp.2990-2995, Sep., 2011.
- [11] S. Datta, "Compound semiconductor as CMOS channel material: Déjàvu or new paradigm?" in *Proc. 66th IEEE Device Res. Conf.*, pp.33-36, Jun., 2008.
- [12] A. Zubair, S. A. Siddiqui, O. F. Shoron, Q. D. M. Khosru, "Impact of bandgap and effective mass on the transport characteristics of tunneling FET," in *Proc. IEEE NMDC*, pp.47-51, Oct., 2010.
- [13] A. S. Verhulst, W. G. Vandenberghe, K. Maex, G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Appl. Phys. Lett.*, Vol.91, No.5, p.053102, Jul., 2007.
- [14] P. F. Guo, L. T. Yang, Y. Yang, L. Fan, G. Q. Han, G. S. Samudra, Y. C. Yeo, "Tunneling field-effect transistor: Effect of strain and temperature on tunneling current," *Electron Device Letters, IEEE*, Vol.30, No.9, pp.981-983, Sep., 2009.



Min Jin Lee was born in Seoul, Korea, in 1987. She received the B.S. degree in 2010 from Sogang University, Seoul, Korea, where she is currently working toward the M.S. degree in the Department of Electronic Engineering. Her current research interests include tunneling field-effect transistor (TFET), nanoscale novel devices and anti-fuse memory.



Woo Young Choi was born in Incheon, Korea, in 1978. He received the B.S., M.S. and Ph. D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea in 2000, 2002 and 2006, respectively. From 2006 to 2008, he

was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA as a post-doctor. Since 2008, he has been a member of the faculty of Sogang University (Seoul, Korea), where he is currently an Assistant Professor with the Department of Electronic Engineering. He has authored or coauthored over 110 papers in international journals and conference proceedings and holds 15 Korean patents. His current research interests include fabrication, modeling, characterization and measurement of CMOS/CMOS-compatible semiconductor devices and nano-electromechanical (NEM) memory cells.