Ambipolarity Factor of Tunneling Field-Effect Transistors (TFETs)

Jung-Shik Jang and Woo Young Choi

***Abstract*—The ambipolar behavior of tunneling field-effect transistors (TFETs) has been investigated quantitatively by introducing a novel parameter: ambipolarity factor (*v*). It has been found that the malfunction of TFET can result from the ambipolar state which is not on- or off- state. Therefore, the effect of ambipolar behavior on the device performance should be parameterized quantitatively, and this has been successfully evaluated as a function of device structure, gate oxide thickness, supply voltage, drain doping concentration and body doping concentration by using *v*.**

***Index Terms*—Ambipolarity factor (v), transistor parameter, tunneling field-effect transistor, low voltage**

I. INTRODUCTION

Recently, environmentally-friendly innovative devices have attracted researchers' attention for higher energy efficiency. One of the most promising devices is a tunneling field-effect transistor (TFET) [1-10]. TFETs are expected to achieve low power consumption because they have a subthreshold swing less than 60 mV/dec at room temperature and lower off-current than MOSFETs.

Fig. 1 shows the structure and band diagrams of a conventional silicon-on-insulator (SOI) TFET. In the case of an n-channel TFET, the source and drain regions are p- and n-type doped, respectively. Drain current (I_D) is controlled by gate voltage (V_G) through band-to-band tunneling (BTBT) process. When V_G is low, the tunneling barrier width between the source and channel is so wide that only few electrons can pass, i.e. off-state. On the other hand, when V_G is positively high, the tunneling barrier width between the source and channel is narrow enough for many electrons to pass, i.e. on-state. Interestingly, when V_G is negatively high, the tunneling barrier width between the channel and drain narrows, which induces tunneling current. It is called the ambipolar state. Because the ambipolar state is a unique property of TFETs, it needs to be investigated rigorously.

In this paper, the effect of ambipolar state on off-current will be evaluated quantitatively by introducing an ambipolarity factor (*v*).

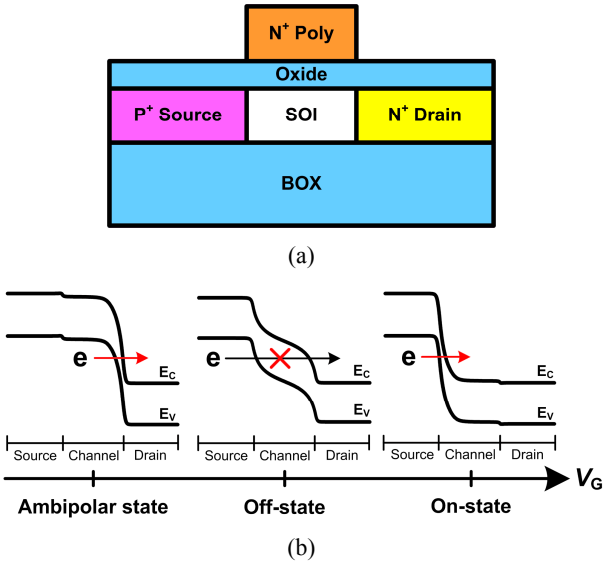

Fig. 1. (a) Conventional n-channel SOI TFET structure, (b) Band diagrams of the TFET in ambipolar, off- and on-state. As VG increases, the TFET experiences ambipolar, off- and on-state sequentially.

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II. AMBIPOLARITY FACTOR (v)

In order to observe the operation of TFETs, device simulation was performed by using Silvaco ATLAS [11]. Nonlocal BTBT model which takes into account the spatial variation of the energy bands and the spatial discord of generation/recombination of opposite carrier types was used including bandgap narrowing effect. Gate leakage was ignored in simulation. Source doping concentration (N_S) and drain doping concentration (N_D) were 10^{20} cm^{-3}, respectively. Body doping concentration (N_B) was 10^{14} cm^{-3}. Channel length (L_{ch}), gate oxide thickness (t_{ox}) and SOI layer thickness (t_{SOI}) were 50 nm, 2 nm and 30 nm, respectively. Gate workfunction was set to 4.17 eV. Drain voltage (V_D) was fixed at 1 V and source was grounded. Fig. 2 shows the three components of I_D of TFETs: on-current, p-i-n diode saturation current (I_{leak}) and ambipolar current. I_D is minimal in the off-state and increases in on- or ambipolar states as the magnitude of V_G increases.

The unusual current increase in ambipolar state can cause a serious problem in terms of circuit design. For example, in the case of a two-input TFET NAND gate, as shown in the inset of Fig. 2, if the upper n-TFET input signal is low and the lower n-TFET input signal is high, the output signal can be low because V_G of upper n-TFET is relatively lower than the source voltage due to the source degeneration topology, which means ambipolar state.

Moreover, Fig. 3 shows on- and ambipolar current increase abruptly and the range of V_G where I_D is minimal decreases when L_{ch} becomes smaller than 100 nm. Finally, it is observed that minimum I_D (I_{min}) in I_D-V_G curve increases when L_{ch} becomes smaller than 25 nm, which means that the ambipolar current determines the off-current of short-channel TFETs. Therefore I_D is composed of only on-current and ambipolar current in the case of short-channel TFETs, whereas I_D is composed of three kinds of currents in the case of long-channel TFETs. In other words, when long-channel TFETs are turned off, off-current is determined by I_{leak}. However, in the case of short-channel TFETs, ambipolar current enhances the off-current which is determined by BTBT current higher than I_{leak}.

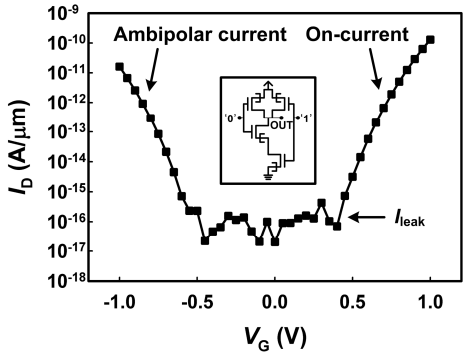


Fig. 2. Simulated I_D-V_G curve of an SOI TFET. I_D consists of three components: on-current, I_{leak} and ambipolar current. The inserted figure shows a 2-input NAND gate. Squared bracket indicates the location of the tunneling junction.

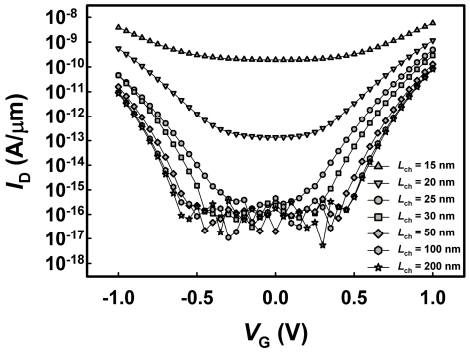


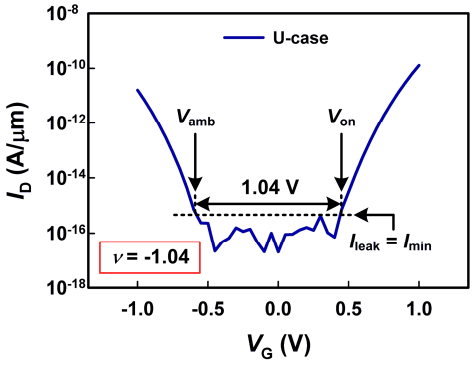
Fig. 3. I_D-V_G curves with L_{ch} ranging from 15 to 500 nm. As L_{ch} decreases, BTBT current increases and also off-current.

Therefore, in order to evaluate the effect of ambipolar state on off-current quantitatively, we introduce a v which is defined as

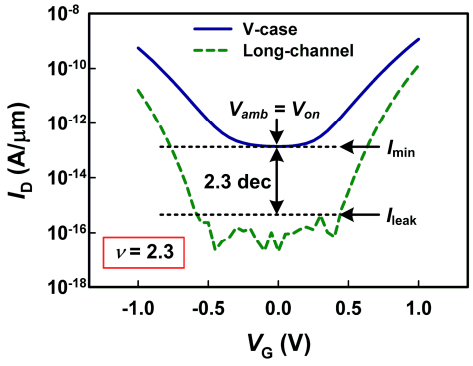
$$v = [\log(I_{leak}) - \log(I_{min})] - \frac{|V_{on} - V_{amb}|}{A} \quad (1)$$

where V_{on} and V_{amb} are the gate voltages when on- and ambipolar current start to exceed I_{min}, respectively. A is defined as 1 V which is used for unit conversion therefore v has no physical unit. I_{leak} could be set to systematic leakage current if I_{leak} is not flat with respect to V_G. v is extracted from I_D-V_G curves when V_D is fixed at supply voltage (V_{DD}) because v has the meaning when the TFETs operate in the circuits. The absolute value is needed for the difference between V_{on} and V_{amb} for v to be used for both n- and p-channel TFETs.

Fig. 4 shows the extraction method of v from the I_D-V_G curve. As discussed in Fig. 3, the shape of I_D-V_G curve can be classified into two cases: the case when $I_{min} = I_{leak}$ at large L_{ch} and the case when $I_{min} > I_{leak}$ at small L_{ch}. The former and latter cases are defined as U- and V- case,



(a)



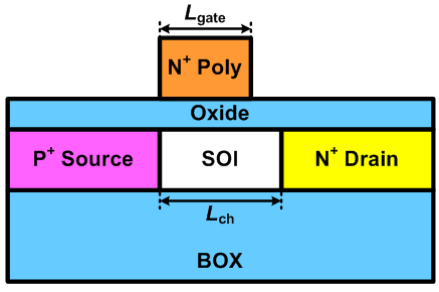
(b)

Fig. 4. The extraction method of v for (a) U-case and (b) V-case.

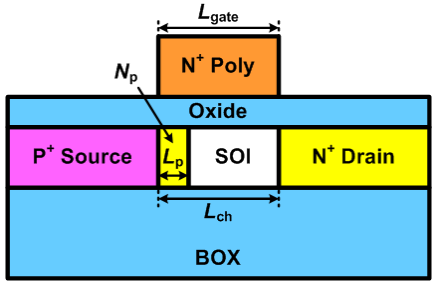
respectively. In the U-case, v is determined only by the voltage difference between V_{on} and V_{amb}, which makes v negative. In the V-case, V_{on} becomes equal to V_{amb}, and v is determined only by the current difference between I_{min} and I_{leak}, which makes v positive. In this case, I_{leak} can be extracted from a long-channel test TFET. Because of its long channel, the test TFET corresponds to the U-case, which makes I_{leak} extraction easier. When v was highly negative, off-current was not affected by ambipolar current. However, as v increases, the difference between V_{on} and V_{amb} becomes smaller. Finally, when v exceeds zero, off-current begins to be determined by ambipolar current. Therefore, lower v values are desirable in terms of ambipolar behavior.

III. Application of Ambipolarity Factor

From now on, the effect of the ambipolar behavior on TFET performance will be discussed by using v. Because general scaling rules of TFETs have not been established yet, various kinds of devices parameters such as t_{ox}, V_{DD}, N_D and N_B have been varied independently. Conventional TFETs shown in Fig. 1(a) have been compared with short-gate TFETs [4] and PNPN MOSFETs [6]. L_{ch} and t_{SOI} were fixed at 50 and 30 nm, respectively. Fig. 5 shows the structures of short-gate TFETs and PNPN MOSFETs. In the case of conventional TFETs and PNPN MOSFETs, the gate length (L_{gate}) is equal to L_{ch}. However, short-gate TFETs have an L_{gate} of 40 nm and an L_{ch} of 50 nm due to their drain-underlap structure. There is a trade-off between ambipolar current and on-current in terms of drain-underlap length. In this work, we selected 10 nm as an optimized drain-underlap length. The pocket doping concentration (N_p) and pocket width (L_p) of PNPN MOSFETs are 4×10^{19} cm^{-3} and 4 nm, respectively. Short-gate TFETs are designed to suppress the ambipolar current thanks to wide tunneling barrier width between the channel and drain, while PNPN MOSFETs are designed to boost on-current thanks to narrow tunneling barrier width between the source and channel due to fully depleted pocket. Thus, as shown in Fig. 6, short-gate TFETs show less severe ambipolar behavior than conventional TFETs while PNPN MOSFETs show more severe ambipolar behavior than conventional TFETs. Therefore the superior technology for TFETs can be distinguished by comparing v of several kinds of TFETs.



(a)



(b)

Fig. 5. Device structures of (a) short-gate TFET and (b) PNPN MOSFET.

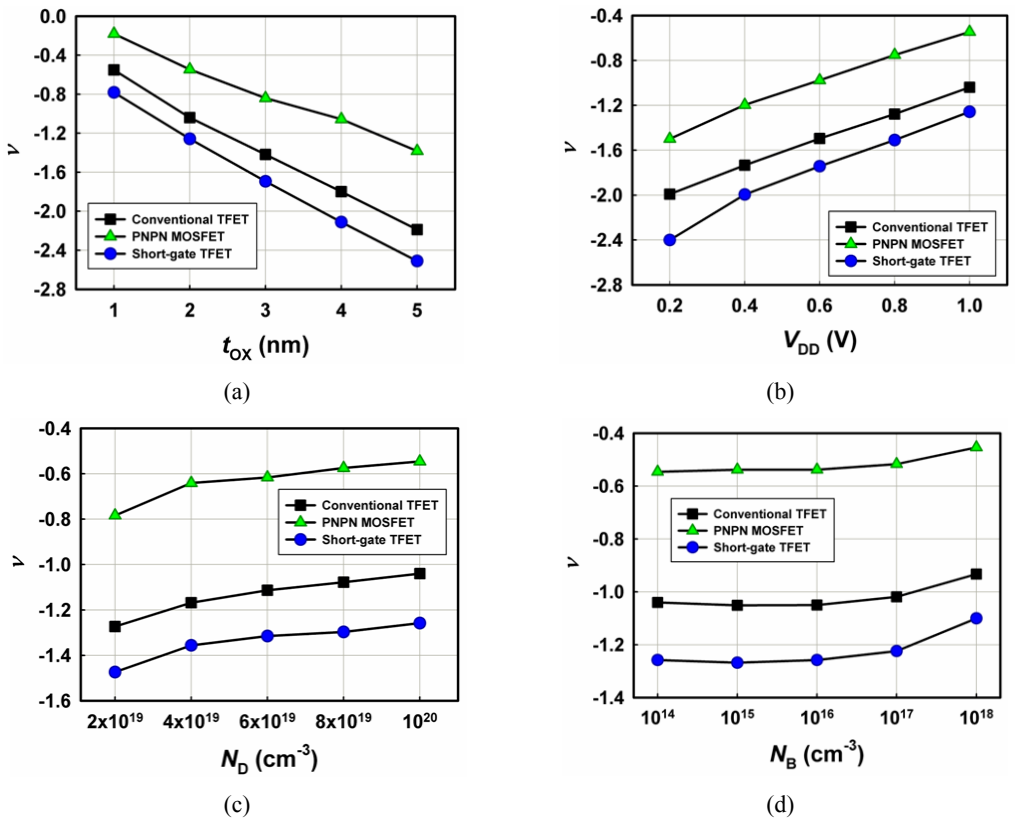


Fig. 6. The effect of (a) t_{ox}, (b) V_{DD}, (c) N_D, (d) N_B on v.

Fig. 6(a) shows the effect of t_{ox} on v. As t_{ox} decreases, v increases because the coupling ratio between the gate and channel rises as t_{ox} becomes smaller and then both on- and ambipolar current increase. Fig. 6(b) shows the effect of V_{DD} on v. As V_{DD} decreases, v decreases. It is because the reverse bias at the tunneling junction between the channel and drain is decreased, and the tunneling probability and ambipolar current decrease. Fig. 6(c) shows the effect of N_D on v. As N_D decreases, v decreases because it makes tunneling barrier width between the channel and drain so wide that ambipolar behavior is suppressed [8]. Note that it is physically the same phenomenon with V_{DD} lowering because both N_D lowering and V_{DD} lowering result in the upward-moving of energy band of drain side, thus tunneling barrier width between the gate and drain increases. However, V_{DD} lowering is more effective engineering solution than N_D lowering, and it can be found by comparing the v values. It shows one of the reasons why v is useful when optimizing device parameters. Fig. 6(d) shows the effect of N_B on v. At low N_B, v is constant because the tunneling barrier width between the channel and drain is too wide for electrons to pass. However, at high N_B, v decreases with increasing N_B. It is because the abrupt junction between channel and drain is formed as N_B increases. Therefore tunneling barrier width between the channel and drain is so narrow that electrons can pass it.

To sum up, it is recommended that TFETs have thick gate oxide and low operation voltage, lightly doped drain and body to suppress the ambipolar behavior. Also, introducing novel structures such as short-gate TFETs can be considered. However, it should also be noted that ambipolarity is suppressed generally at the sacrifice of on-current. Therefore, when designing TFETs, on-current as well as v needs to be considered in terms of performance and power consumption.

IV. CONCLUSIONS

The effect of ambipolar behavior on TFETs has been evaluated by using ambipolarity factor v. Because low-power consumption is one of the biggest advantages of TFETs, suppressing ambipolar current is as important as boosting on-current. The introduction of v makes the

analysis of ambipolarity easier. It has been confirmed that ambipolarity can be suppressed effectively by introducing novel device structures and optimizing t_{ox}, V_{DD}, N_D and N_B.

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