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A Unified Analytical One-Dimensional Surface Potential Model for Partially Depleted (PD) and Fully Depleted (FD) SOI MOSFETs

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Abstract—**In this work, we present a unified analytical surface potential model, valid for both PD and FD SOI MOSFETs. Our model is based on a simplified one dimensional and purely analytical approach, and builds upon an existing model, proposed by Yu et al. [4], which is one of the most recent compact analytical surface potential models for SOI MOSFETs available in the literature, to improve its accuracy and remove its inconsistencies, thereby adding to its robustness. The model given by Yu et al. [4] fails entirely in modeling the variation of the front surface potential with respect to the changes in the substrate voltage, which has been corrected in our modified model. Also, [4] produces self-inconsistent results due to misinterpretation of the operating mode of an SOI device. The source of this error has been traced in our work and a criterion has been postulated so as to avoid any such error in future. Additionally, a completely new expression relating the front and back surface potentials of an FD SOI film has been proposed in our model, which unlike other models in the literature, takes into account for the first time in analytical one dimensional modeling of SOI MOSFETs, the contribution of the increasing inversion charge concentration in the silicon film, with increasing gate voltage, in the strong inversion region. With this refinement, the maximum percent error of our model in the prediction of the back surface potential of the SOI film amounts to only 3.8% as compared to an error of about 10% produced by the model of Yu et al. [4], both with respect to MEDICI simulation results.**

Index Terms—**SOI MOSFET, PD and FD, surface potential, unified analytical model**

I. INTRODUCTION

With bulk MOSFETs being driven to their performance limits in terms of delay and power dissipation considerations, in the process of meeting the increasing requirements of the newer technology nodes, efforts have been continuously made to find a reliable substitute for them. SOI devices, due to their various advantages, viz., low parasitic capacitances and leakage currents, better resistance against the short channel effects [1], improved subthreshold swing [2], etc., have emerged as an important alternative to the bulk MOSFETs.

Starting from the one-dimensional analytical model of the threshold voltage for thin film SOI MOSFETs, published by Lim and Fossum in 1983 [3], several analytical models have been suggested in the literature for modeling the surface potential and the current-voltage characteristics of SOI MOSFETs. We will focus on developing one-dimensional models due to the inherent simplicity of this approach. The model proposed by Yu et al. [4] is one of the most recent simplified one-dimensional analytical models, which evaluates the surface potential for both PD and FD SOI MOSFETs, using a single unified expression. This model is completely free of iterations unlike the surface potential

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models given by Sleight and Rios [5] and by Bolouki et al. [6].

However, a careful study of the model given by Yu et al. [4] exposes some weak points in it, viz., inability to correctly model the dependence of the front surface potential on the substrate voltage, self-inconsistent results due to misrepresentation of the operating modes of SOI devices, and ignoring the contribution of the inversion charge while expressing the back surface potential of the SOI film. These need to be corrected in order to maintain the accuracy and reliability of the model. Thus, the goal of our work is to modify and improve the surface potential model given by Yu et al. [4] so as to increase not only its robustness but also its accuracy. We have taken the help of MEDICI simulations and theoretical results from other authentic sources, to support our arguments wherever needed.

The work has been presented in the following sequence. Section II, which has four sub-sections, deals with the refinement of the existing model [4], as well as the development of new models. The first sub-section (II.1) discusses the effect of substrate voltage on the front surface potential in the FD SOI case, while the second sub-section (II.2) presents our modified models for the front and back surface potentials. The third sub-section (II.3) deals with the further refinement of the model by including the effect of the inversion charge on the surface potential, which, to the best of our knowledge, is the first attempt in the literature in analytical one-dimensional modeling of SOI MOSFETs.

The subthreshold I-V model, using our model for the surface potentials, is given in sub-section II.4. The results of our model, which showed a significant improvement in the accuracy with regard to the back surface potential as compared to those reported in [4], both with respect to MEDICI simulation results, are presented in Section III. This section also presents the results of the I-V model, where it is shown that the model of [4] produces meaningless and unphysical results, whereas our model portrays the behavioral dependence accurately, supported by theory [3, 7, 8]. The summary and conclusion of the work is presented in Section IV.

II. THE MODEL

In this section, we first introduce the surface potential model proposed by Yu et al. [4] in order to highlight its basic features. Then we investigate its solutions as provided in [4] under different operating modes of SOI MOSFETs, so as to evaluate their predictions. This is followed by adjustments to the model wherever it fails to capture the true device characteristics, as reported in the literature.

Fig. 1 shows the structure of an n-channel SOI MOSFET. The Si film (also known as the channel) is p-type, having a doping concentration N_{ch} and thickness t_{si}, the thickness of the field oxide is t_{fox}, while the buried oxide thickness is t_{box}. The substrate also is p-type, having a doping concentration N_{sub}. The y-coordinate is taken to be along the channel, while the x-coordinate is perpendicular to it. The terminal voltages applied at the gate and drain are V_G and V_D respectively, both measured with respect to the source, which is grounded in our work.

According to [4], the operating zone of an SOI device is determined by two factors: the state of the front-surface and the degree of depletion attained by the silicon film. These operating zones and their corresponding front surface potential expressions are [4]: (i) PD-accumulation $\left(\psi_{sa}^{p}\right)$, (ii) PD-depletion $\left(\psi_{sd}^{p}\right)$, (iii) PD-strong inversion $\left(\psi_{si}^{p}\right)$, (iv) FD-subthreshold $\left(\psi_{ss}^{f}\right)$, and (v) FD-strong

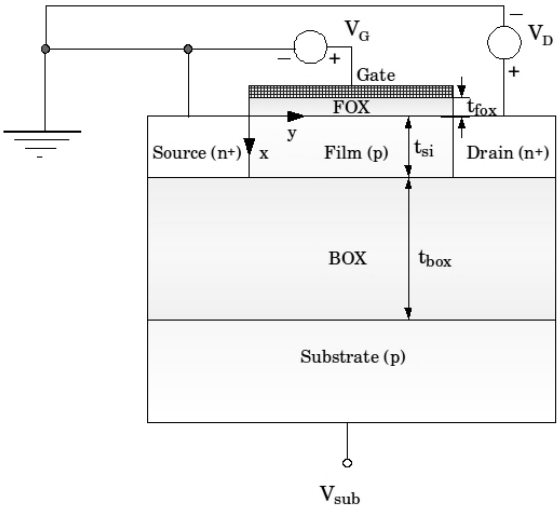

Fig. 1. The structure of an n-channel SOI MOSFET. The y-coordinate is along the channel, while the x-coordinate is perpendicular to it. The terminal voltages V_G and V_D are referenced with respect to the source, which is grounded.

inversion $\left(\psi_{si}^{f}\right)$. The solutions for each of these five elementary regions are summarized in [4]. As illustrated in [4], the front surface potential ψ_{sf} is solved for each of these five regions, and the solutions thus obtained are combined using standard smoothing functions [4] in a methodical way, so as to arrive at the unified surface potential expression, valid for both PD and FD cases. It [4] also uses a simple expression to relate the back surface potential (ψ_{sb}) to ψ_{sf}, as discussed in detail later in Section II.2.

1. Effect of the Substrate Voltage on the Front Surface Potential for the FD SOI Case

According to [7], if the silicon film is fully depleted and if a positive potential is applied at the substrate, then both the front gate and the substrate compete for having a share of the depletion charge created in the film. Fig. 2 shows the MEDICI simulation results of the variation of the absolute potential (with respect to ground) in the silicon film, due to the application of a positive bias of around 1 V at the front gate and 4 V at the substrate. Now, if the substrate voltage V_{sub} is raised, then the share of the depletion charge in the Si film controlled by it also increases. Since the total depletion charge in the film is constant, hence, the contribution of the front gate to the total depletion charge is bound to reduce. This should lead to a concomitant rise in the front surface potential, leading to an increase in the inversion layer charge, which causes a reduction in the threshold voltage of the device.

This phenomenon can be summarized as follows: for a fixed V_G, an increase in V_{sub} produces a corresponding increase in ψ_{sf}, causing the inversion layer electron concentration to rise, thereby lowering the threshold voltage of the SOI MOSFET [3, 8]. However, an unusual behavior is observed if the surface potential in FD-subthreshold $\left(\psi_{ss}^{f}\right)$, using its expression as given in [4], is plotted as a function of V_{sub}, as shown in Fig. 3. On increasing the substrate voltage, ψ_{ss}^{f} rises initially, however, after reaching a maximum, it starts to fall off with further increase in V_{sub}. This behavior is not in agreement with that suggested by the theory [7, 8], which predicts that ψ_{ss}^{f} should increase monotonically with increasing V_{sub}.

The source of this fallacy is that, though the substrate voltage term had been taken into account in [4] while writing the potential balance equation, yet ψ_{sf} had been reported to be independent of V_{sub}. Though the relation between ψ_{sf} and ψ_{sb} employed in [4] is strictly valid only when the substrate terminal is grounded, however, since the final model given in [4] explicitly includes the term V_{sub}, therefore, there is no apparent reason to believe that

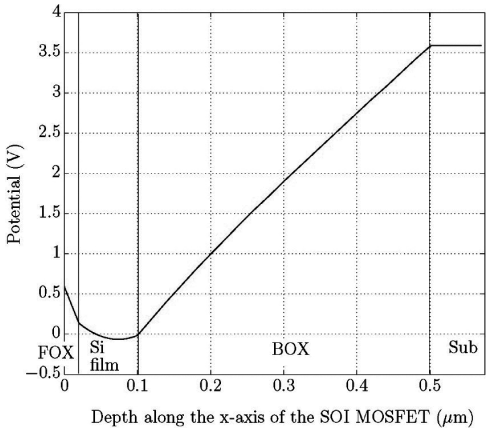

Fig. 2. The variation of potential in the FD-subthreshold region along the x-axis of an SOI MOSFET, simulated in MEDICI, with V_G = 1 V and V_{sub} = 4 V (note that due to the gate and substrate contact drops, the actual gate and substrate voltages are not exactly same as the applied biases). Device parameters are: $N_{ch} = 10^{17}$ cm^{-3}, $N_{sub} = 10^{18}$ cm^{-3}, t_{si} = 80 nm, t_{fox} = 20 nm, and t_{box} = 400 nm.

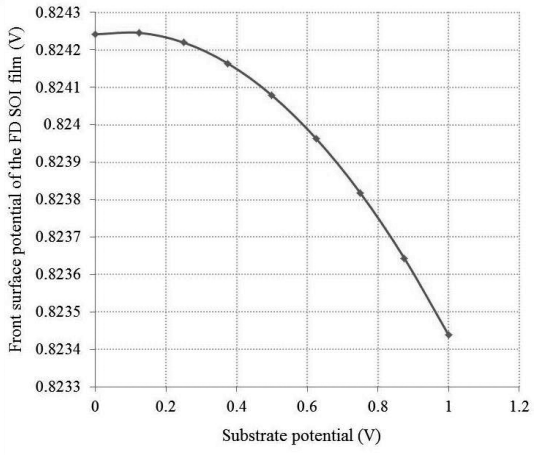

Fig. 3. Front surface potential in FD-subthreshold region as a function of the substrate potential at a fixed gate bias of 0.3 V, as predicted by [4]. Device parameters: $N_{ch} = 10^{17}$ cm^{-3}, $N_{sub} = 10^{18}$ cm^{-3}, t_{si} = 94 nm, t_{fox} = 10 nm, and t_{box} = 347 nm.

the substrate is always grounded. A careful derivation substantiates the fact that indeed the expression for the back surface potential (ψ_{sb}) must have a substrate voltage dependent term, as it can be shown by solving the one-dimensional Poisson's equation along the x-axis (i.e., along the vertical cross-section of the device) of the silicon film that ψ_{sb} is given by [9]:

$$\psi_{sb} = \psi_{sf} - \alpha + \beta\left(V_{sub} - \psi_{sb}\right) \tag{1}$$

where $\alpha = qN_{ch}t_{si}^2/(2\varepsilon_s)$, with q being the Coulomb charge, and ε_s is the permittivity of Si. The term β appearing in Eq. (1) is expressed as $\beta = C'_{box}/C'_{si}$, where C'_{box} (= ε_{ox}/t_{box}, with ε_{ox} being the permittivity of SiO_2) is the buried oxide capacitance per unit area, and C'_{si} (= ε_s/t_{si}) is the Si film capacitance per unit area.

For contemporary technology, the value of β is typically very small (~ 10^{-2} or so), and, hence, Eq. (1) can be reduced to:

$$\psi_{sb} \simeq \psi_{sf} - \alpha + \beta V_{sub} \tag{2}$$

It is to be noted here that a small value of β does not make the last term in Eq. (2) redundant, since it may be non-negligible as compared to the difference between ψ_{sf} and ψ_{sb}, especially for the thin film FD SOI case, where substrate depletion is quite possible and a potential drop may develop at the BOX-substrate interface too [9]. Using Eq. (2) for ψ_{sb} instead of the one given in [4], in order to derive the expression for ψ_{ss}^f, following a procedure similar to that adopted in [4], we get:

$$\psi_{ss}^f = \frac{V_g - \frac{C'^2_{box}}{C'^2_{fox}}\left(V'_{sub}+\alpha\right) - \sqrt{\frac{C'^2_{box}}{C'^2_{fox}}\left(V_g - V'_{sub} - \alpha\right)^2 + \left(1 - \frac{C'^2_{box}}{C'^2_{fox}}\right)(\alpha - \beta V_{sub})\gamma^2}}{\left(1 - \frac{C'^2_{box}}{C'^2_{fox}}\right)} \tag{3}$$

where $V_g = V_G - V_{FF}$, with V_{FF} being the front gate flatband voltage, $V'_{sub} = V_{sub} - V_{FB}$, with V_{FB} being the back gate (i.e., the substrate for this case) flatband voltage, C'_{fox} (= ε_{ox}/t_{fox}) is the front oxide capacitance per unit area, and γ $\left(=\sqrt{2q\varepsilon_s N_{ch}}/C'_{fox}\right)$ is the body effect coefficient for the Si channel.

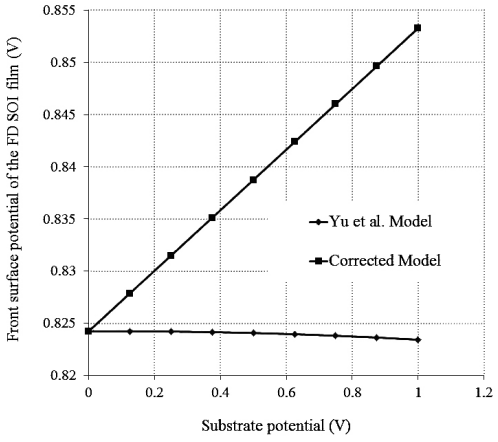

Fig. 4. Front surface potential in FD-subthreshold region as a function of the substrate potential, as predicted by our modified model [Eq. (3)]. The results obtained from [4] are also shown. Note that our modified model is able to capture the correct (monotonic) behavior of the front surface potential, as reported in theory [7, 8]. Device parameters and bias are the same as those in Fig. 3.

The variation of ψ_{ss}^f with respect to V_{sub}, as predicted by Eq. (3), is plotted in Fig. 4, which shows that an increase in V_{sub} for a given gate voltage (V_G) always produces a concomitant rise in ψ_{ss}^f, which is also confirmed theoretically [3, 7, 8]. Though in the FD-strong inversion region, ψ_{sf} is almost pinned at approximately ($2\phi_F + V_{CB}$), where ϕ_F [= $\phi_t \ln(N_{ch}/n_i)$, with ϕ_t (= kT/q, where k is the Boltzmann constant and T is the absolute temperature) being the thermal voltage, and n_i is the intrinsic carrier concentration of Si] is the bulk potential of the Si channel, and V_{CB} is the amount of split between the Fermi levels of the channel and the bulk, yet for the sake of completeness, it is important to include the effect of substrate bias while expressing ψ_{si}^f, which, following our procedure given above, gets modified to:

$$\psi_{si}^f = 2\phi_F + V_{CB} + \phi_t \ln\left\{\frac{\frac{1}{\gamma^2}\left[\left(V_g - f_\psi^f\right)^2 - \frac{C'^2_{box}}{C'^2_{fox}}\left(V'_{sub} - f_\psi^f + \alpha\right)^2\right] - \alpha + \beta V_{sub}}{\phi_t\left[1 - \exp\left(\frac{\beta V_{sub} - \alpha}{\phi_t}\right)\right]}\right\} \tag{4}$$

where f_ψ^f, being a smoothing function [10], retains its original form and is still given by the expression reported in [4], with the only exception that it uses the modified form of the term ψ_{ss}^f, as given by Eq. (3).

2. Front and Back Surface Potentials

In [4], a relation between ψ_{sf} and ψ_{sb}, derived assuming full-depletion of the film, was used to evaluate these parameters for an SOI device with $N_{ch} = 10^{17}$ cm^{-3}, t_{si} = 150 nm, and grounded substrate, in the strong inversion region and under full depletion. It was reported in [4] that for this device, the difference $\Delta\psi_s$ (= $\psi_{sf} - \psi_{sb}$) between these two potentials, is constant (i.e., independent of V_G) with a value of 0.75 V. However, when we applied Eq. (2) (which should give identical results here as the substrate is grounded) in order to find $\Delta\psi_s$ for this case, it gave us a result of 1.725 V.

Since the difference between the two results was too large to be ignored, we performed a thorough investigation, and came up with the following observation. In order to fully deplete the device with the specifications given above, the critical gate voltage (V_C) required, evaluated from its expression given in [4], is approximately 1 MV! Hence, within the practical limits of the gate bias, this device can never be fully depleted. However, the results reported in [4] is under the assumption of full depletion of the channel region, whereas in reality, the device is actually only partially depleted. Thus, there is an inconsistency in the results reported in [4].

A notable fact is that both the channel doping and the channel thickness cannot be arbitrarily increased, while also maintaining the FD status of the Si film. The maximum width $X_{d,max}$ of the depletion region that can be created in the channel under the front oxide by the application of a gate field, is reduced at higher channel doping. Once $X_{d,max}$ is reached, the electrons in the inversion layer will prevent any further significant increase in the film depletion charge, by screening the gate field [11]. Hence, it is necessary to ascertain beforehand, whether an SOI device can really be operated in the FD mode. A first hand estimate can be obtained from the condition that for an SOI device to work in the FD mode, the following relation between the maximum depletion width and the film thickness must hold:

$$X_{d,max} = \sqrt{\frac{2\varepsilon_s\left(2\phi_F + n\phi_t\right)}{qN_{ch}}} \geq t_{si} \qquad (5)$$

where we have used the assumption of pinning of the surface potential in the strong inversion region. The value of the parameter n in Eq. (5) ranges from 4 to 6 [11]. Based on the MEDICI simulations conducted by us on the SOI MOSFETs, with the device parameters taken from [4], a value of 4 for n provided the best estimate for the pinned value of the surface potential, and hence, was selected as the optimal choice for our simulations. Thus, by using Eq. (5), the operating mode of an SOI device can be known in advance, and hence, any error arising due to misinterpretation of the operating region of the device can be avoided.

3. Effect of the Inversion Charge

While deriving Eq. (2), the contribution of the inversion charge was not taken into account [9], which, on strict grounds, limits its validity only to the weak inversion region of the SOI MOSFET operation. In the strong inversion region, as the gate voltage is increased, the level of inversion in the channel increases too, building up the inversion layer electron concentration. In Fig. 5, we show the MEDICI simulation results of the variation of the electric field along the depth at around the middle of the Si channel for two different gate voltages (V_G) of 1.8 V and 3 V for an FD-SOI device.

In this figure, note that at higher gate bias, the area

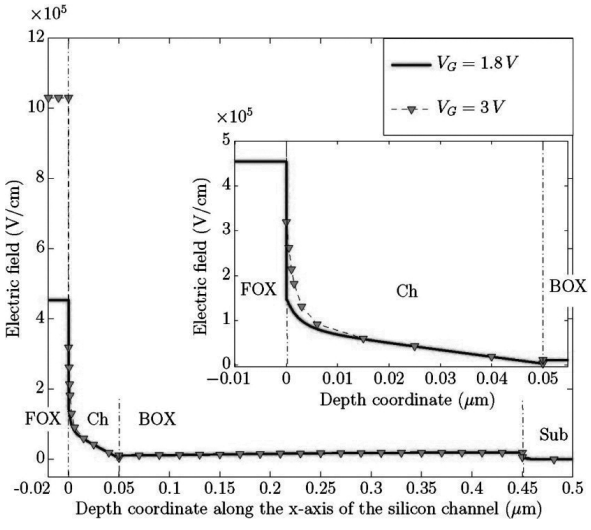

Fig. 5. Electric field along the x-axis at around the middle of the Si channel, at two different gate voltages V_G = 1.8 V and 3 V, for an FD SOI device simulated in MEDICI. Inset: Magnified view at the FOX-channel interface. Device parameters are the same as that for Fig. 2, with the exception that tsi has been further scaled down to 50 nm.

under the curve in the channel region near the FOX-film interface is increased, which points to the fact that there is a greater potential drop across the inversion layer. Consequently, this potential drop cannot be neglected as compared to that across the fully depleted silicon film. This is especially important for thin film devices, where the drop across the depletion layer is already small due to the smaller amount of the available film depletion charge, and also because the inversion layer occupies a finite portion of the film thickness.

Thus, it can be inferred from the above discussion that, with an increase in V_G, the difference between ψ_{sf} and ψ_{sb} of an FD SOI film increases too in the strong inversion region, which was indeed found to be true from MEDICI simulations of SOI devices having a wide range of substrate doping, channel thickness, and front and buried oxide thicknesses. The model of Yu et al. [4] failed to bring out this fact, where not only the difference between ψ_{sf} and ψ_{sb} remained constant in the strong inversion region, but also their results deviated significantly from those obtained by MEDICI simulations, particularly so for ψ_{sb}.

A careful survey of the literature reveals that almost all the available models based on a purely one-dimensional analytical approach [5, 6, 9] have ignored the contribution of the inversion charge while computing ψ_{sb} for the case of FD SOI MOSFETs, as they all utilize a relation similar in form to Eq. (1), which is devoid of any term that can model the effect of the inversion charge build-up in the strong inversion region. To include this effect in our one-dimensional model of the surface potential for FD SOI devices, we propose a simple modification to Eq.(2) in the FD-strong inversion region as:

$$\psi_{sb} = \psi_{sf} - \alpha + \beta V_{sub} - mV_G \tag{6}$$

with m being an empirical parameter, and from extensive MEDICI simulations for devices having different combinations of channel doping N_{ch} (10^{16}-10^{17} cm^{-3}) and channel thickness t_{si} (50-100 nm), its value was found to lie within a range of 0.02 to 0.04.

The relationship expressed by Eq. (6) between the front and back surface potentials is sufficiently accurate for values of the gate voltage as high as 10 V. For even higher values of gate voltages, we might require a better model, since under such a condition, the dependence of the surface potential on the gate voltage is not strictly linear. However, noting that the present technology advocates low voltage operation, such a high value (i.e. 10 V and beyond) of the gate voltage will never be practical, and hence, Eq. (6) becomes valid for the typical values of the gate voltage used in the current technology. Moreover, a simple relationship such as the one presented in Eq. (6) is desirable for easy inclusion into any further analysis [4]; therefore, it is reasonably practical to use it in the calculation of the surface potentials.

Thus, using the relation given by Eq. (6) instead of Eq. (2) in order to compute the front surface potential in the FD-strong inversion region [4], we get:

$$\psi_{si}^{f} = 2\phi_F + V_{CB} + \phi_t \ln\left\{\frac{\frac{1}{\gamma^2}\left[\left(V_g - f_\psi^f\right)^2 - \frac{C_{box}'^2}{C_{fox}'^2}\left(V_{sub}' - f_\psi^f + \alpha + mV_G\right)^2\right] - \alpha + \beta V_{sub} - mV_G}{\phi_t\left[1 - \exp\left(\frac{\beta V_{sub} - \alpha - mV_G}{\phi_t}\right)\right]}\right\} \tag{7}$$

The unified model for the front surface potential, valid in all regions of SOI operation, is now obtained by combining the elementary solutions of the variables ψ_{sa}^{p}, ψ_{sd}^{p}, and ψ_{si}^{p}, as given in [4], along with the solutions of the variables ψ_{ss}^{f} and ψ_{si}^{f}, as given by Eqs. (3, 7) respectively, with the help of the smoothing functions [4], following the procedure similar to that used in [4].

In order to calculate the overall back surface potential for a given front surface potential, we define the relation between ψ_{sf} and ψ_{sb} for an FD SOI film in such a way that it smoothly changes from Eq. (2) in the weak inversion region to Eq. (6) in the strong inversion region, i.e., the proposed form of ψ_{sb} is given by:

$$\psi_{sb} = \psi_{sf} - \alpha + \beta V_{sub} - \frac{mV_G}{1 + r_1 \exp\left(-\frac{\psi_{sf} - 2\phi_F}{r_2\phi_t}\right)} \tag{8}$$

where r_1 and r_2 are dimensionless fitting parameters, each having a nominal value of unity, however, can be tuned to obtain greater accuracy.

4. Subthreshold I-V Characteristics

For further insight into how our model portrays the I-V characteristics, we used the surface potential values

obtained from our model and that of [4] in the I-V model reported in [4], with a small modification to include the effect of the substrate voltage on the drain current. This modification pertains to the expression of the difference in the front surface potentials between the source and drain sides of the channel, denoted by $\psi^{f}_{sL0,subthreshold}$ Eqs. (8b-8d) in [4]). The new expression for $\psi^{f}_{sL0,subthreshold}$ includes the effect of the substrate voltage as well, and is expressed as:

$$\psi^{f}_{sL0,subthreshold} = \frac{\sqrt{\frac{C'^{2}_{box}}{C'^{2}_{fox}}\left(V_g - V'_{sub} - \alpha\right)^2 + \left(1 - \frac{C'^{2}_{box}}{C'^{2}_{fox}}\right)\left(\alpha - \beta V_{sub} + \lambda_0\right)\gamma^2} - \sqrt{\frac{C'^{2}_{box}}{C'^{2}_{fox}}\left(V_g - V'_{sub} - \alpha\right)^2 + \left(1 - \frac{C'^{2}_{box}}{C'^{2}_{fox}}\right)\left(\alpha - \beta V_{sub} + \lambda_L\right)\gamma^2}}{\left(1 - \frac{C'^{2}_{box}}{C'^{2}_{fox}}\right)} \quad (9)$$

where

$$\lambda_0 = \phi_t \exp\left(\frac{\psi^{f}_{s0} - \phi_B - V_{Sb}}{\phi_t}\right)\left[1 - \exp\left(-\frac{\alpha - \beta V_{sub}}{\phi_t}\right)\right] \quad (10)$$

and

$$\lambda_L = \phi_t \exp\left(\frac{\psi^{f}_{sL} - \phi_B - V_{Db}}{\phi_t}\right)\left[1 - \exp\left(-\frac{\alpha - \beta V_{sub}}{\phi_t}\right)\right] \quad (11)$$

with ψ^{f}_{s0}, ψ^{f}_{sL}, V_{Sb}, V_{Db}, and ϕ_B all being as defined in [4]. All the parameters used in the I-V model have the same values as reported in [4]. The results are presented at the end of Section III.

III. RESULTS

The solutions for the overall front and back surface potentials (ψ_{sf} and ψ_{sb} respectively), using our proposed modification, are plotted in Fig. 6 along with those predicted by the original model of Yu et al. [4], and both are compared with the results obtained from the MEDICI simulations. The values of all the parameters used in the simulations are listed in Table 1. As can be observed from the figure, throughout all the operating regions, our model results for both ψ_{sf} and ψ_{sb} show a very close match with those obtained from MEDICI simulations. In particular, in the strong inversion region, our model results for ψ_{sb} show a much superior match with those obtained from MEDICI simulations, as compared to that of the results reported in [4]. We attribute this to the inclusion of the effect of inversion charge on the back surface potential, which has been attempted in our work for the first time in the literature [please refer to Eq. (8)].

Table 1. The values of parameters used in simulations

Parameter (Unit)	Value
N_{ch} (cm^{-3})	10^{17}
N_{sub} (cm^{-3})	10^{18}
t_{si} (nm)	50
t_{fox} (nm)	20
t_{box} (nm)	400
n	4
m	0.03
r_1	1
r_2	1

Please note that in Fig. 6, we have kept the substrate voltage (V_{sub}) zero, in order to compare our results with that obtained from [4]. However, this effectively nulls the contribution of V_{sub} in determining the surface potentials, and hence, in Fig. 6, the curves of Ψ_{sf} obtained from our model and [4] appear to be the same. However, we have shown that V_{sub} can indeed influence Ψ_{sf}, as in the FD-subthreshold region where, as depicted in Fig. 4, our model predicts a rise in Ψ_{sf} with respect to an increase in V_{sub}, which is quite consistent with theory [3, 7, 8], while [4] predicts incorrect values of Ψ_{sf}.

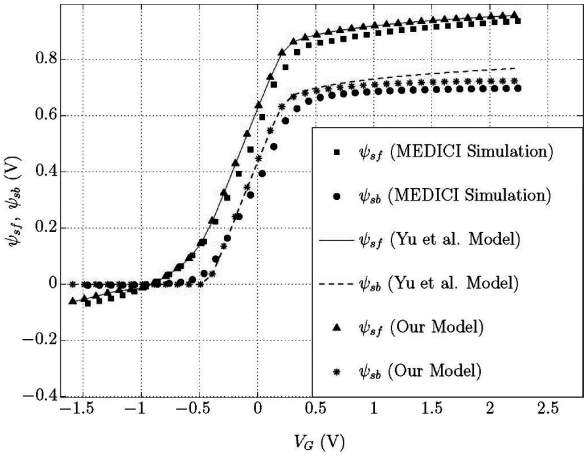

Fig. 6. Overall ψ_{sf} and ψ_{sb} of an SOI MOSFET as a function of the gate voltage VG, obtained from MEDICI simulations, [4], and our model. The values of the parameters used in the simulations are listed in Table 1. V_{sub} has been kept at 0 V for a meaningful comparison of our results with those reported in [4].

The accuracy achieved by our model can be confirmed through Fig. 7, which plots the percent error in the prediction of ψ_{sb} in the strong inversion region with respect to MEDICI simulation results, for the SOI MOSFET whose surface potential characteristics are shown in Fig. 6, both for Yu et al. model [4] and for our model. It is found that the percent error produced by our model is always smaller as compared to that of Yu et al. model [4], with the maximum error of our model (for the range of gate voltage used in the simulation) being only 3.8%, while [4] produces a maximum error of almost 10%.

In order to observe the effect of our surface potential models on the subthreshold I-V characteristics, we used Eqs. (9-11) of our model, in the I-V model reported in [4], and the results obtained from our model and that of [4] are shown in Fig. 8, for a device having the same dimensions, doping concentrations, and bias conditions as in Fig. 3. In Fig. 8, the variation of the drain current has been shown with respect to the variation in the substrate voltage (V_{sub}), with the gate voltage fixed at a constant value. All the other parameter values are kept the same as that reported in [4].

As explained in Section II.1**,** theory [3, 7, 8] states that Ψ_{sf} increases with an increase in V_{sub}, hence, we should expect a rise in the electron concentration at the front surface, which in turn, will amount to an increase in the drain current. However, from Fig. 8, it is clear that the model of Yu et al. [4] fails to capture this behavior – a careful observation shows that [4] predicts a droop in the drain current with increasing V_{sub}, which directly contradicts with the theory. On the other hand, the drain current characteristic obtained from our model correctly demonstrates this effect, thus establishing its consistency with the theory given in the literature [7, 8]. We would also like to assert that here we showed only the subthreshold I-V characteristics, since under strong inversion, the effect of V_{sub} on the surface potential is not marked, due to the pinning of the latter.

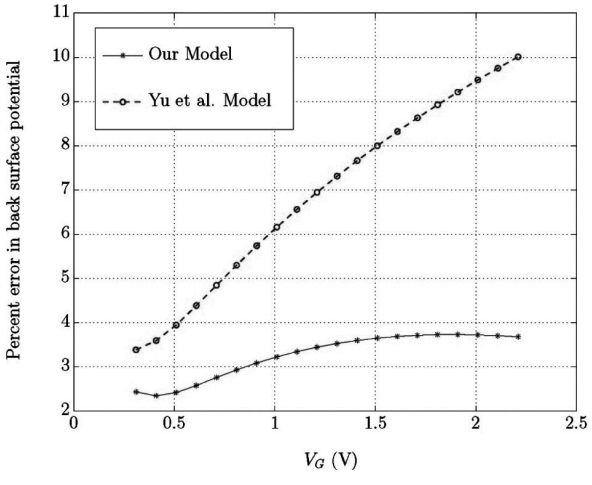

Fig. 7. The percent error in the computation of ψ_{sb} as a function of VG in the strong inversion region, obtained from our model and that reported in [4] (as shown in Fig. 6), both with respect to MEDICI simulation results.

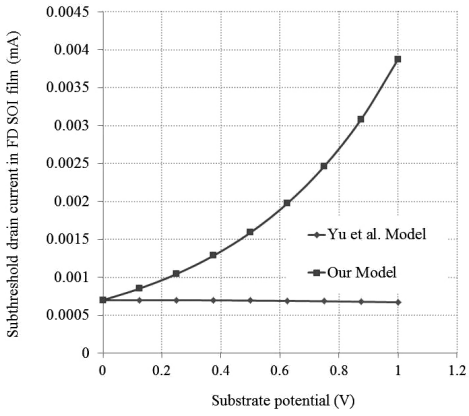

Fig. 8. The drain current in the FD subthreshold region as a function of the substrate voltage (V_{sub}), with a constant gate voltage (V_G) and drain-source bias (V_{DS}) of 0.3 V and 50 mV respectively, obtained from our model and that reported in [4]. Device parameters: W/L = 7.83 μm/0.28 μm, source and drain series resistances R_S = R_D = 70 Ω, and the remaining parameters are the same as those in Fig. 3.

IV. SUMMARY AND CONCLUSION

We worked upon the analytical surface potential model for SOI MOSFETs given by Yu et al. [4] to rectify its physically unjustifiable results, and also to improve its accuracy. Yu et al. model [4] completely fails to capture the dependence of the front surface potential of an FD SOI film on the substrate voltage. This was corrected by modifying the expression relating ψ_{sf} and ψ_{sb} used in [4], and then recalculating the front surface potential using this modification. With this improvement, the model presented in [4] provides an accurate solution of the surface potentials under any biasing scheme, over the entire operating region of SOI MOSFETs.

In [4], an SOI MOSFET is assumed to be in full depletion, while on the contrary, our calculation shows that for the chosen device parameter values, it can operate only in the PD mode. This misrepresentation

leads to contradictory results produced by the model, and thus, makes it self-inconsistent. In our work, the source of this error has been traced and the need for predetermining the mode of operation of an SOI device has been emphasized. A criterion for this has also been suggested in the form of Eq. (5).

The model is improved further by incorporating the effect of increasing inversion charge concentration in the strong inversion region as the gate voltage is increased, in the determination of the surface potentials for an FD SOI film. This is an entirely new contribution to the one-dimensional analytical modeling of the surface potentials for SOI MOSFETs and yields reasonably good results for low values of gate voltages, as confirmed by MEDICI simulations. The final overall corrected and updated unified surface potential model is not only robust, but also has improved accuracy over [4], as is evident from Fig. 6 and Fig. 7.

Finally, in this work, we have preserved the analytical format of the surface potential model as that reported in [4], while building upon and improving it further. Through MEDICI simulations, we have shown that our model is more accurate than that reported in [4]. Also, our model shares the similar range of operating conditions/device structures as those reported in [4], other than a reasonably practical limit of a maximum gate voltage of 10 V, which is well consistent with the current technology. We have also demonstrated that the current-voltage model correctly portrays the dependence of the drain current on the substrate voltage, whereas [4] completely fails to do so, as discussed towards the end of the Results section. This further establishes the usefulness of our analytical surface potential model quite firmly.

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