A CMOS Outphasing Transmitter Using Two Wideband Phase Modulators

Sungho Lee*, Kihyun Kim, Jaehoon Song**, Kang-Yoon Lee***, and Sangwook Nam****

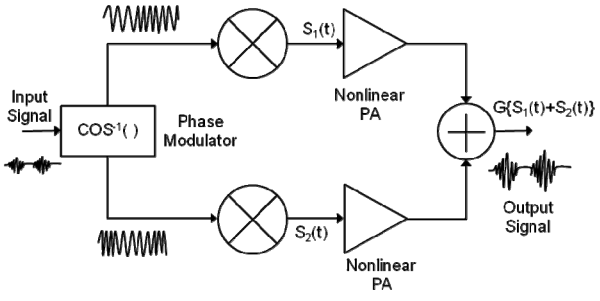
Abstract—**This paper describes a CMOS outphasing transmitter using two wideband phase modulators. The proposed architecture can simplify the overall outphasing transmitter architecture using two-point phase modulation in phase-locked loop, which eliminates the necessity digital-to-analog converters, filters, and mixers. This architecture is verified with a WCDMA signal at 1.65 GHz. The prototype is fabricated in standard 130 nm CMOS technology. The measurement results satisfied the spectrum mask and 4.9% EVM performance.**

Index Terms—**CMOS, outphasing, phase modulator, PLL, transmitter, two-point modulation**

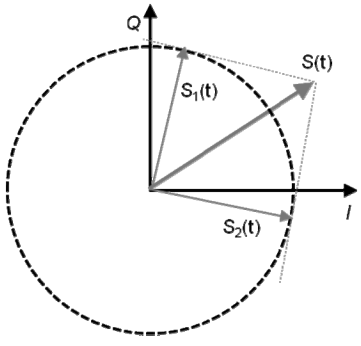
I. INTRODUCTION

Radio frequency (RF) power amplifier (PA) is one of the most critical blocks in an RF transmitter, since the power consumption in mobile terminal has been important with various wireless functions. Therefore, to increase overall power efficiency in RF transmitters, various approaches including pulse modulation, envelope tracking and outphasing technique in RF PA have been investigated in architecture level and circuit level [1-4].

Among them, outphasing technique has potential by relying on the fact that two constant-envelope signals are amplified and combined to make up the output, as shown in Fig. 1. Since signals driving the amplifiers do not bear any information on their amplitudes, there is no demand on the linearity of the amplifiers, and they can be biased in their compression points for maximum power efficiency [4-5]. Therefore, by adopting nonlinear and highly efficiency PA, such as Class-D, Class-F, highly efficiency transmitter can be achieved. However, phase up-conversion processing part contains burdens having complex configuration and the wide bandwidth with



(a)



(b)

Fig. 1. (a) Conventional outphasing transmitter architecture and (b) Outphasing operating principle.

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* Korea Electronics Technology Institue (KETI), Kyunggi-do 463-816, Korea.
** Applied Electromagnetics Laboratory, School of Electrical Engineering, Institute of New Media and Communications (INMC), Seoul National University, Seoul 151-744, Korea.
*** Department of Electronics Engineering, Konkuk University, Hwayang-dong, Gwangjin-gu, Seoul, Korea.
E-mail : 2sungho@gmail.com

order of tens of MHz. Moreover, the signal separation is also required in the phase up-conversion block.

In this paper, we adopted two RF phase modulators which employ two-point modulation technique for direct modulation using phase locked loop (PLL). The two-point modulation technique can circumvent the limited bandwidth issue using injecting signal with two paths. Also, direct modulation eliminates the necessity of digital-to-analog converters, filters, and mixers.

Section II reviews the conventional architectures and their performance limited issues. Section III shows the design of the proposed outphasing transmitter. Section IV, V and VI show the measurement results, discussion and conclusion, respectively.

II. CONVENTIONAL SCS TECHNIQUES

Until now, various outphasing signal generators have been developed. In the first group, the signal is decomposed into two out-phasing signals by a block, called a signal component separator (SCS), in baseband, as shown in Fig. 2(a). Then, this I/Q pairs of signals are up-converted to RF by two mixers. The SCS can be realized with either analog circuits [6-7] or a DSP [8-10]. In either case, a significant portion of the circuit is still analog, and any mismatch in phase or amplitude between two paths can potentially ruin the performance of the whole transmitter. Also, this I/Q signal path is used twice to generate two outphasing signals. Therefore, four digital-to-analog converters, four reconstruction filters, and two up-conversion mixer are required, which can lead to large area and high power consumption [11]. Moreover, each block can deteriorate signal linearity. The signal separation can be done in IF/RF domain. In this method, two outphasing signals are built directly in RF, provided that the variable envelope signal is already available.

Fig. 2(b) shows a block diagram of the transmitter in which, $s(t)$ is fed to a 90-degree phase-shifting network followed by a variable gain amplifier (VGA) [12-13]. With proper gain control, the output of the VGA will be an estimate of e(t). In the feedback path, the power of the generated outphasing signals $2s_1(t)$ and $2s_2(t)$ are detected and compared with a reference value (ref). The

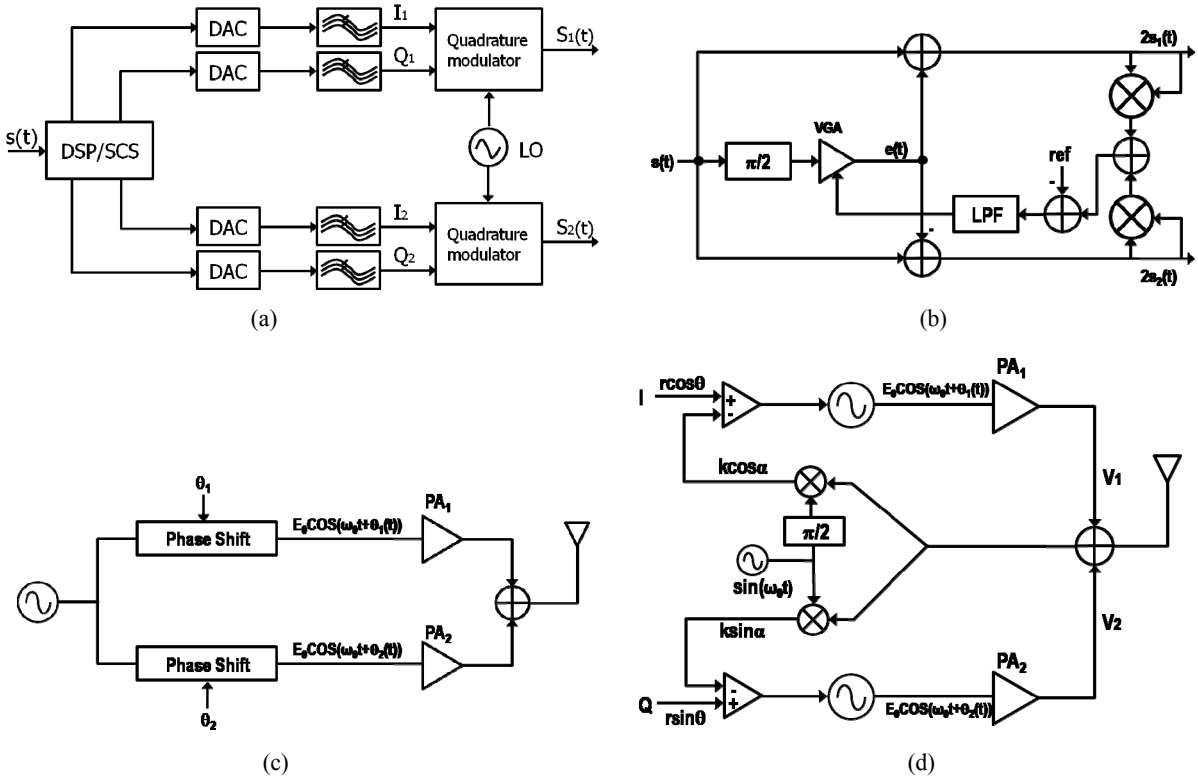

Fig. 2. Various RF up-converting signal separator. (a) Cartesian structure, (b) Analog-domain signal separation, (c) Phase shifter, and (d) Combined analog locked loop universal modulator.

error signal passes through a loop filter and adjusts the gain of the VGA. With a closed loop form, two outphasing signals are generated without any digital processing. Thus, this structure can be applied at IF stage or RF stage. However, this structure also suffers from linearity and harmonic issues from mixers.

In Fig. 2(c), outphasing signals are created by passing the constant phase and constant variable output of an oscillator through two delay lines. Provided that $\theta_1(t)$ and $\theta_2(t)$ in Fig. 2(c) and the carrier frequency are known, the amount of the delays are calculable. The delay line can be realized with an LC network [14] or active circuits [15]. The trouble is that an LC network consumes a large area, especially in the case of low-frequency carriers; also, it is extremely difficult to realize digitally. The poor noise performance of the active delay lines makes them too difficult to conform to stringent standards, such as Enhanced Data Rates for GSM Evolution (EDGE).

Finally, in the Fig. 2(d), a Combined Analog Locked-Loop Universal Modulator (CALLUM) transmitter incorporates the component separation and up-conversion simultaneously by employing two VCOs [16]. With appropriate control signals, two VCOs can generate the desired phase-modulated components of a LINC system. These components are then amplified and combined to produce the output. To generate feedback signals for a closed loop, the output is down-converted signal and two resulting error signals feed the VCOs. All of the research in the field uses this main principle and adds peripheral circuits to reduce the error and mismatch and to improve the stability. The main disadvantages of CALLUM transmitter are instability and pulling problems. Two oscillators and two Pas are all operating in the same frequency and different phases. Oscillators can be pulled by each other and by PAs. The need for extra mixers and oscillators for down-conversion is another weak point.

III. PROPOSED OUTPHASING TECHNIQUES

The proposed architecture can simplifies the overall outphasing transmitter architecture using two-point phase modulation in phase-locked loop, which eliminates the necessity digital-to-analog converters, filters, and mixers. Fig. 3 shows the proposed architecture of the outphasing transmitter. It consists of two phase modulators and two power amplifiers, and a power combiner. The phase modulator has roles of RF up-conversion and phase modulator for outphasing signal. And the PA amplifies phase modulated RF signals. In this section, the two main parts will be described.

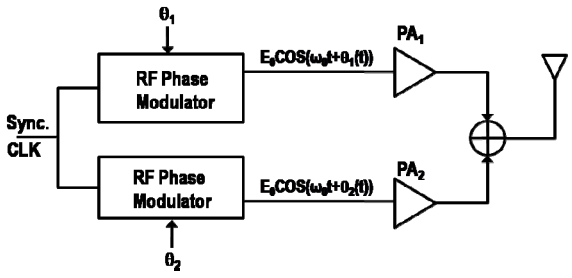

Fig. 3. Proposed outphasing transmitter architecture.

1. Phase Modulator

Phase modulator is formed by conventional phase-locked loop with delta-sigma modulation. LC VCO tunes center frequency at 1.65 GHz. Original signal is separated into two constant-envelope outphasing signals. The outphasing signals can be up-converted by PLL using phase modulation. In the PLL, PLL bandwidth must be widened to accommodate the modulated spectrum. However, the loop bandwidth trades-off phase noise. A narrow loop bandwidth low-pass filters the quantization noise with increasing lock-time.

Recently, two-point modulated technique is verified in GSM application which used only phase-modulated signals [17]. The results showed the wideband modulation can be applicable. Therefore, to expand the modulation bandwidth beyond the PLL loop bandwidth, as is necessary in wide-band modulations such as WCDMA, the two-point modulation is adopted in this work. Fig. 4 shows the block diagram of phase modulator using two-point modulation. The two-point modulation structure is the same as that used in [17]. Using two modulation points, the PLL bandwidth can be the noise floor is lower than -137 dBm/Hz. To satisfy the noise floor, the PLL bandwidth should be small to suppress the quantization noise from the delta-sigma modulator. However, too small bandwidth can the locking time make slow. Thus, considering this trade-offs, the PLL bandwidth was set to 250 KHz. When WCDMA signal is applied using the two-point modulation, the gain and

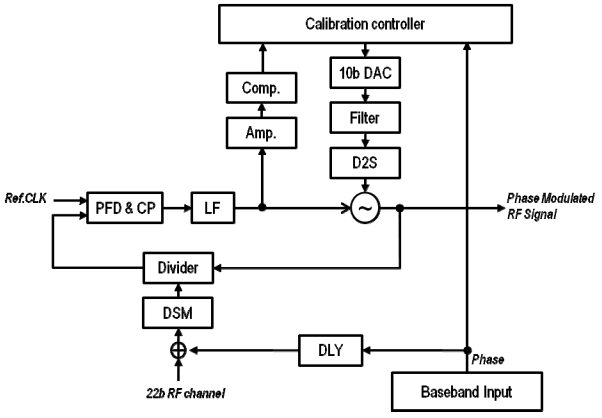

Fig. 4. Block diagram of phase modulator using two-point modulation technique.

timing mismatch specification is much tightened than narrow bandwidth signal (e.g. GSM signal). With a behavioral simulation, the gain and timing requirements are investigated, at least 10 ns timing mismatch and 1% gain mismatch should be guaranteed in the two-point modulation. Moreover, from WCDMA EVM specification of 17.5%, the phase error of the synthesizer should be smaller than half. As 17.5% of EVM is corresponding to the 10 degree phase error, the phase error of the phase modulator should be less than 5 degree. Thus, 2.5% phase error was set to design target for design margin. Fig. 5 shows the resultant simulation results for the phase modulator.

To achieve outphasing signals with two PLLs, two PLLs should be synchronized with RF signals. Thus, to synchronize two PLLs, timing-related blocks such as Primary/Secondary counter, Phase-frequency detector and delta-sigma modulator (DSM) should be operated with the same reset signal.

2. Class-D Power Amplifier

As quarter-wave transmission lines are used for power combiner, the PA should act as voltage source under phase change. In voltage-mode Class D amplifiers, two transistors are used in tandem with the result that their combination acts approximately like a voltage source at all times. The use of CMOS technology for Class D amplifier is especially attractive, because of the availability of complementary switching devices.

However realistic CMOS inverter-based RF switches have demerits of voltage breakdown and nonlinearity, which degraded overall efficiency. Fig. 6 shows a schematic of the fabricated class-D PA cell. The class-D PA uses 1.2 V transistors (L=130 nm) for fast switching and low on-resistance. Cascoded inverter topology allows a PA output voltage swing of 0-2 Vdd. Nominal supply voltage of the given technology, Vdd, is set to 1.2 V. Thus, when PMOS transistors are turned-on, each PMOS transistor has voltage drop of Vdd, which prevents transistor breakdown. And, NMOS transistors are turned-on, same voltage drop happens. This topology guarantees that the devices are not stressed beyond the allowable voltage limits for reliability and lifetime. The transistor width of output stage is set to 6400 um of PMOS and 3200 um of NMOS, respectively.

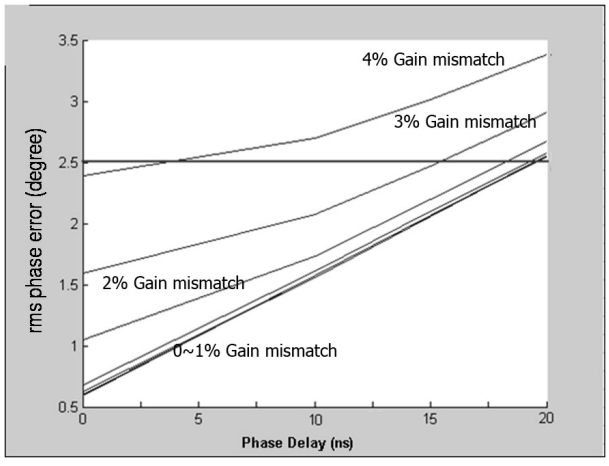

Fig. 5. Behavioral simulation results of rms phase error according to delay and gain mismatches in phase modulator.

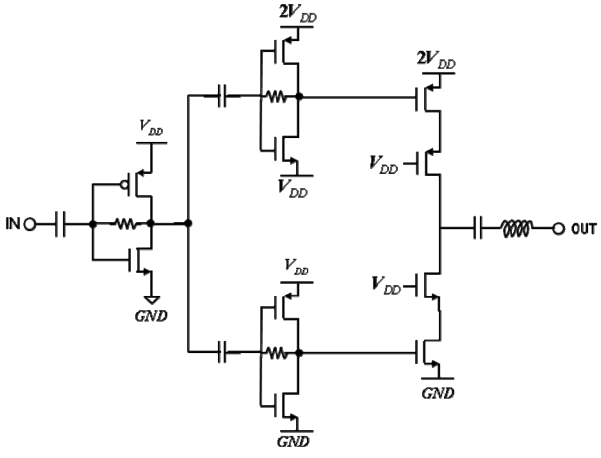

Fig. 6. Schematic of Class-D PA.

IV. MEASUREMENT RESULTS

Fig. 7 shows the detailed designed structure of the proposed outphasing transmitter. DSMs, 10-bit digital-to-analog converters, and digital phase signal generators are located in external FPGA board and fed into the prototype. The transmitter chip was fabricated in standard 130 nm CMOS technology. A die photo of the transmitter is depicted in Fig. 8. The total active area is 1.5 mm × 2.4 mm. In order to make the measurements possible, two Class-D PAs, two phase modulators, LPF and digital control logic including serial-to-parallel interface (SPI) were integrated on the chip.

Two transmission lines on PCB were used for the power combiner to combine the two outphasing signals. Regarding measurement setup, a PC generates the baseband modulation data with channel information through 22-bit delta-sigma modulation, and loads it on the FPGA board. The integrated DACs on FPGA generate two analog phase signal for VCO path. Fig. 9 shows the measured phase error of one-side PLL. The measured rms phase error is 1.7 degree, which satisfies the designed target. Fig. 10 shows the final RF output spectrum. By combining outphasing signals, the spectrum mask conforms the WCDAM mask. The measured output signal power was 19 dBm. To analyze the RF signal's quality, EVM test was conducted. The best measured EVM performance was 4.9%, as shown in Fig. 11.

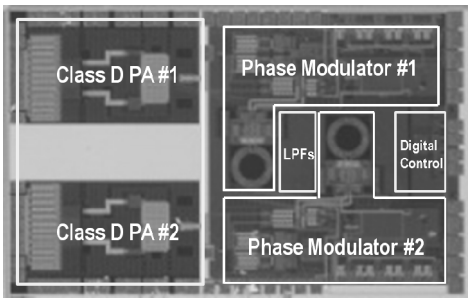

Fig. 8. Fabricated chip microphotograph.

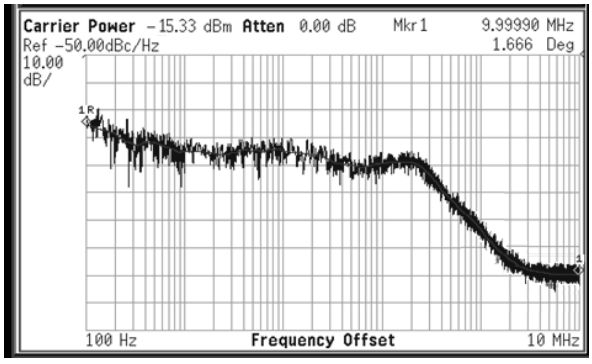

Fig. 9. Measured phase error of one-side PLL.

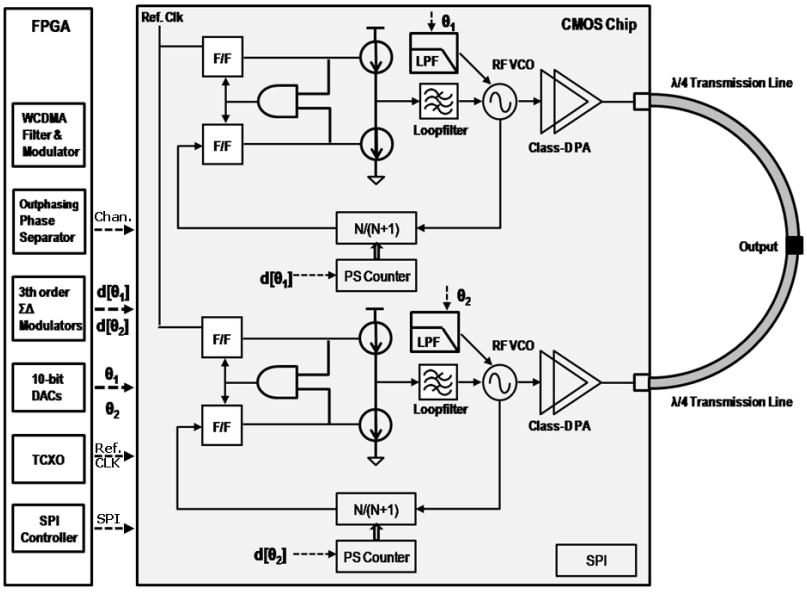

Fig. 7. Fabricated chip micro photograph.

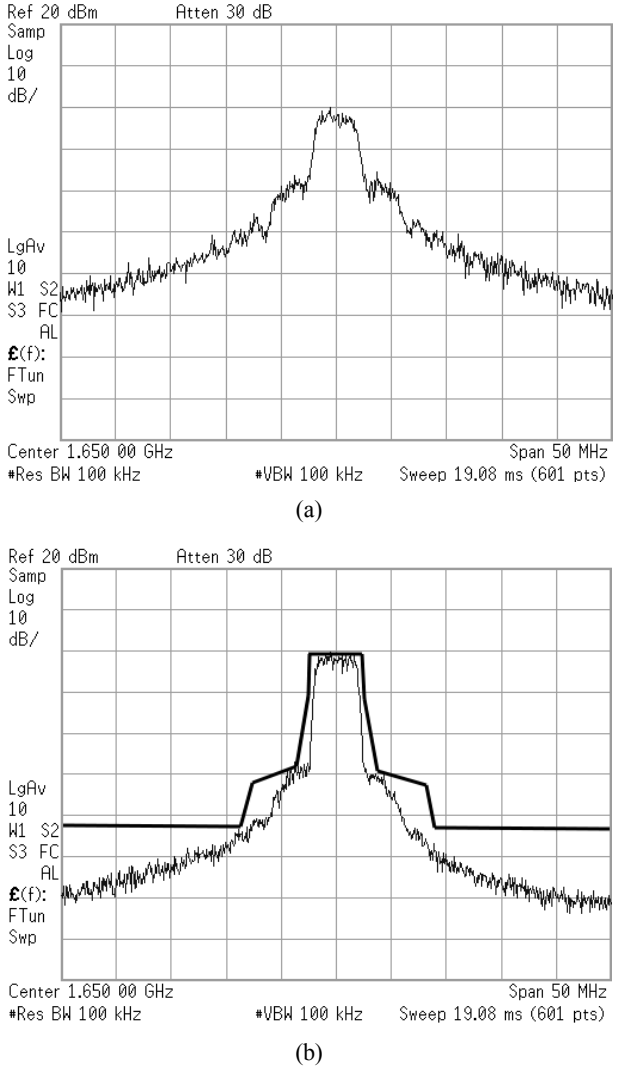

Fig. 10. (a) Measured output spectrum before combining and (b) Measured output spectrum after combining.

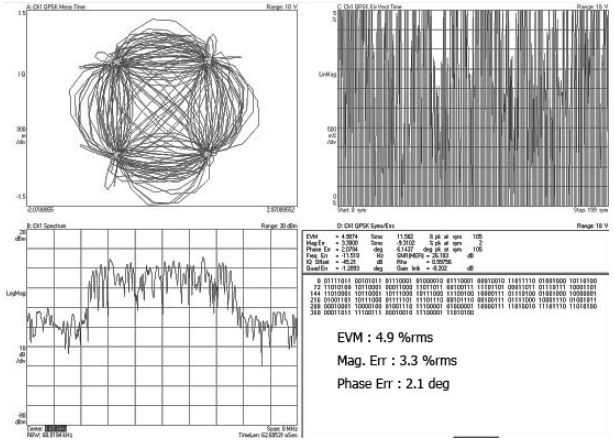

Fig. 11. Measured EVM performance.

V. DISCUSSION

The EVM performance index is described as:

$$E_{VM} = 100 \cdot \sqrt{[1+M^2]-2M\cos(\varphi_e)}\,. \qquad (1)$$

M is gain error between reference and measured signal and φ_e is phase error, respectively. The main two factors of impairing EVM performance are phase error and gain error. However, in the MSK modulation, constant enveloped signal is used, which means that gain error does not affect EVM performance.

In the phase modulator using two-point modulation, main performance limitation is gain mismatch between two paths. And, the varactor's gain mismatch in the path of two-point modulation affects the phase mismatch in the RF up-converted signal Therefore, in the outphasing architecture using two-point modulation, the phase error caused by gain mismatch of two-point modulation affects the combined signal's EVM performance. The outphasing amplifier output in the presence of phase errors $\Delta\phi$ can be described by

$$\begin{aligned} S(t) &= S_1(t) + S_2(t) \\ &= G_0 r_{\max}\cos[\omega_c t+\theta(t)-\psi(t)]+G_0 r_{\max}\cos[\omega_c t+\theta(t)+\psi(t)+\Delta\phi] \\ &= 2G_0\cos\left(\frac{1}{2}\Delta\phi\right) r(t)\cos\left[\omega_c t+\theta(t)+\phi_0+\frac{1}{2}\Delta\phi\right] \\ &\quad -2G_0\sqrt{r_{\max}^2-r^2(t)}\sin\left(\frac{1}{2}\Delta\phi\right)\cos\left[\omega_c t+\theta(t)+\phi_0+\frac{1}{2}\Delta\phi\right] \end{aligned} \qquad (2)$$

, where ω_c is the carrier frequency and $\psi(t)$ is outphasing angle. The last expression is obtained by first combining the phase distortion terms and then abstracting $\psi(t)$ out of the phase angle. The spectrum regrowth stems from the phase distortion of the summed signal. The first term in Eq. (2) contributes to the desired signal, and the last term adds to the out-of-band spectrum, as a consequence of incomplete cancellation of the wideband quadrature signal $e(t)$. The reason of effect to the out-of-band spectrum will be described in the following part. From Eq. (2), the phase error from the gain mismatch in the two-point modulation affects the gain error as well as phase error in EVM performance. Moreover, the phase error increases unwanted adjacent signal spectrum.

Combining Eq. (1) and first term of equation Eq. (2),

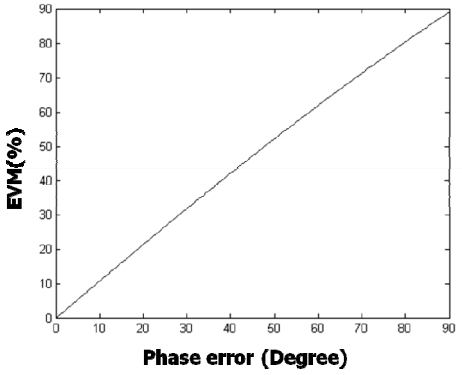

Fig. 12. Simulated EVM performance from phase mismatch in outphasing transmitter.

new EVM equation can be calculated as

$$E_{VM} = 100 \cdot \sqrt{[1+\{1+\cos\left(\frac{1}{2}\Delta\phi\right)\}^2] - 2\{1+\cos\left(\frac{1}{2}\Delta\phi\right)\}\cos\left(\frac{1}{2}\Delta\phi\right)} \\ = 100 \cdot \sqrt{2-\cos\left(\frac{1}{2}\Delta\phi\right) - \cos^2\left(\frac{1}{2}\Delta\phi\right)}. \quad (3)$$

Fig. 12 shows the simulated EVM performance due to the phase mismatch in the outphasing transmitter. Because the varactor's gain mismatch in the two-point modulation affects directly phase mismatch in the outphasing structure, maximum acceptable gain mismatch can be decided regarding EVM performance as shown in Fig. 12.

VI. CONCLUSIONS

This paper describes a CMOS outphasing transmitter using two wideband phase modulator. The proposed architecture can simplify the overall outphasing transmitter architecture using two-point phase modulation in phase-locked loop. This structure can be utilized in various RF applications.

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Sungho Lee received the B.S. and M.S. degrees in electrical engineering from Sogang University, Seoul, Korea, in 1998 and 2000, and the Ph. D. degree from Seoul National University in 2011, respectively,

From 2000 to 2009, he was a senior design engineer with the GCT semiconductor, San Jose, CA., where he worked on various RF transceiver developments for wireless communication applications, including WCDMA, PHS, GSM and S/T DMB. Since 2010, he has been a senior researcher with Korea Electronics Technology Institute (KETI), Kyunggi-do, Korea.

His research interests include RF/analog circuits analysis/design of RF transceivers, power amplifiers and high performance data converters in nanometer CMOS technology.

Kihyun Kim received the B.S. degree in electrical engineering from Korea Aerospace University, Gyeonggi, Korea, in 2008, and the M.S. degree from Seoul National University, Seoul, Korea, in 2010, where he is currently working toward the Ph.D. degree in electrical engineering. His research interests include in CMOS implementation of wireless communication transceivers in biomedical engineering.

Jaehoon Song received the B.S. degree in electrical Information and communication engineering semi-conductor systems engineering from Sungkyunkwan University, Gyeonggi, Korea, in 2010. He is currently pursuing the M.S. degree in electrical engineering from Seoul National University, Korea. His research interests include in CMOS implementation of millimeter-wave radar.

Kang-Yoon Lee was born in Jeongup, Korea, in 1972. He received the B.S., M.S. and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively.

From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/ PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. Since 2005, he has been with the Department of Electronics Engineering, Konkuk University, where he is currently an Assistant Professor.

His research interests include implementation of CMOS RF transceiver, analog integrated circuits, and analog/ digital mixed-mode VLSI system design.

Sangwook Nam (S'87–M'88) received the B.S. degree from Seoul National University, Seoul, Korea,in 1981. The M.S. degree from the Korea Advanced Institute of Science and Technology (KAIST), Seoul, Korea, in 1983, and the Ph.D. degree from the University of Texas at Austin, in 1989, all in electrical engineering.
From 1983 to 1986, he was a Researcher with the Gold Star Central Research Laboratory, Seoul, Korea. Since 1990, he has been a Professor with the School of Electrical Engineering and Computer Science, Seoul National University. His research interests include analysis/design of electromagnetic (EM) structures, antennas and microwave active/passive circuits.