A 3 ~ 5 GHz CMOS UWB Radar Chip for Surveillance and Biometric Applications

Seung Jun Lee*,, Jong Ok Ha*,**, Seung Hwan Jung*,**, Hyun Jin Yoo*,**, Young-Hoon Chun***, Wan-Sik Kim***, Noh Bok Lee****, and Yun Seong Eo*,****

Abstract—**A 3-5 GHz UWB radar chip in 0.13 μm CMOS process is presented in this paper. The UWB radar transceiver for surveillance and biometric applications adopts the equivalent time sampling architecture and 4-channel time interleaved samplers to relax the impractical sampling frequency and enhance the overall scanning time. The RF front end (RFFE) includes the wideband LNA and 4-way RF power splitter, and the analog signal processing part consists of the high speed track & hold (T&H) / sample & hold (S&H) and integrator. The interleaved timing clocks are generated using a delay locked loop. The UWB transmitter employs the digitally synthesized topology. The measured NF of RFFE is 9.5 dB in 3-5 GHz. And DLL timing resolution is 50 ps. The measured spectrum of UWB transmitter shows the center frequency within 3-5 GHz satisfying the FCC spectrum mask. The power consumption of receiver and transmitter are 106.5 mW and 57 mW at 1.5 V supply, respectively.**

Index Terms—**Ultra wide band (UWB), biometric radar, sub-sampling, high speed T&H, digital UWB impulse generator**

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* RF Circuit And System Lab., Kwangwoon University, Seoul 139-701, Korea
** Silicon R&D., 409-16 Wolgye-Don, Nowon-Gu, Seoul 139-701, Korea
*** LIG NEX1., 148-1, Mabuk-dong, Giheung-gu, Yong In, Geyonggi, 446-798 Korea
**** Agency for Defense Development., P.O. Box 132, Songpa, Seoul 138-600, South Korea
E-mail : luckynineteen@hanmail.net

I. INTRODUCTION

In this paper, a CMOS radar chip is implemented for the surveillance applications. The operation frequency is decided to be 3-5 GHz of low side band of UWB. As for the detection resolution, in order to monitor the moving objects or human and even respiratory rate, the accurate resolution such as 1cm or less is required, and therefore, the very high sampling frequency up to 16.7 Gs/s is necessary. Considering the practical CMOS integrated circuits, such a fast sampling clock generation and the sample & hold circuit are very hard to be realized. To dissolve these problems, several reports [1] present the correlator based architecture adopting the delay generator such as DLL (Delay Locked Loop) circuit. As an alternative solution, the sub-sampling architecture or equivalent time sampling is considerable and the timing clock can be generated from the DLL [2]. In later case, DLL makes the clocks spaced at equal and fine time offset (several tens ps). For example, once the UWB signal is transmitted and reflected from the target, the reflected impulse is received and sampled at the given time with the DLL clock. In order to achieve equivalent time sampling, the impulse transmission and reception are repeated and sampled by the offset-time shifted clock with the offset time 50 ps in every recursive process. However, the repeated process requires too much time and the high resolution monitoring may be impractical. Hence, 4-channel time interleaved samplers, which is already adopted in the reference [2], is also used in this work. Using the time interleaved sampler the monitoring time becomes 4 times shorter than the single channel architecture. Conclusively, the radar range of 15 m is

divided into 512 coarse range bins, which corresponds to 2.93 cm for each bin, and each coarse bin is divided into 4 fine range bins with a resolution of 7.3 mm. The fine time offset is 50 ps and coarse time offset 200 ps.

The RF front end is composed of 3 - 5 GHz wideband LNA, single to differential (S2D) amplifier, and 4-way RF power splitter. The S2D amplifier eliminates the need of hardly available and bulky off-chip balun and RF power splitter equally distributes the RF power to each channels. In order to track and hold the fast UWB impulse signal up to 5 GHz, the shunt peaking and cross coupled feedback amplifier as the first stage amplifier is proposed. Using this circuit topology, the gain bandwidth product of the first stage amplifier is extended sufficiently to cover up to 5 GHz.

And the analog signal processing (ASP) block including from T&H/S&H to output buffer amplifier has also the variable gain amplifier and integrator, which adaptively control output signal level.

With regard to the UWB transmitter, the digital impulse generator topology is employed, while the center frequency and the bandwidth of UWB signal can be digitally tunable. Moreover, for the sake of the spectral mask, the Gaussian shaping architecture is proposed and developed. The UWB radar chip is implemented in 0.13 μm CMOS process. The digital signal processing part is not provided and the signal capture and digital signal processing are not achieved. Therefore, only the measured results of the required RF and analog performance will be presented in this paper.

II. UWB RADAR ARCHITECTURE

Fig. 1 shows the architecture of the designed UWB biometric radar chip. The received signal reflected by object is amplified by the wideband LNA at the first stage. To generate the differential signal, a wideband single to differential circuit (S2D) is designed and integrated on chip instead of the off chip balun. The converted differential UWB signal is adaptively amplified again by RF VGA. As the final stage of RF front end, the RF power splitter equally distributed the RF impulse power to the 4 ASP (Analog Signal Processing) channels. Since the RF power arrived at each ASP input must be equal in magnitude and phase, the RF power splitter should be designed deliberately

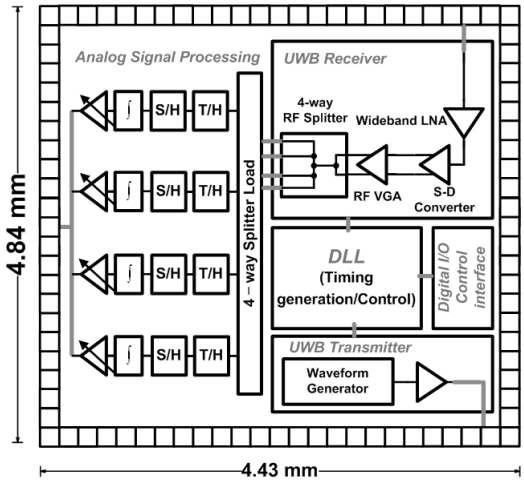


Fig. 1. Architecture of UWB biometric radar transceiver.

considering the parasitic capacitance and inductance caused by long RF interconnection lines. The T&H and S&H circuit, which is the first stage of ASP, tracks and samples the very fast UWB impulse signal. In order to meet these requirements, a new T&H circuit employing the cross coupled feedback topology is proposed to remove the parasitic effects and enhance the gain bandwidth product [3]. The 50 ps offset-timed clocks generated by FB (Fine Bin) DLL are injected into 4 ASP channels respectively, and the time interleaved sampling is achieved. In ASP block, the repetitively sampled signals are integrated several thousand times and amplified to enhance the signal to noise ratio. Finally, the integrated and averaged signal is sampled again by slow speed S&H and is handed over to the digital signal processing part.

The transmitter is made by only digital logic to reduce the current consumption and size, and Gaussian shaping topology is proposed to easily satisfy the FCC EIRP regulations.

III. CIRCUIT DESIGN

1. UWB RF Front-End

The RF front-End includes the LNA, S2D amplifier, RF VGA, and RF power splitter. The LNA is designed using active feedback structure to achieve the wideband input matching from 3 GHz to 5 GHz. Fig. 2 shows the circuit schematic of the designed wide-band LNA using active voltage-current feedback and its simplified small

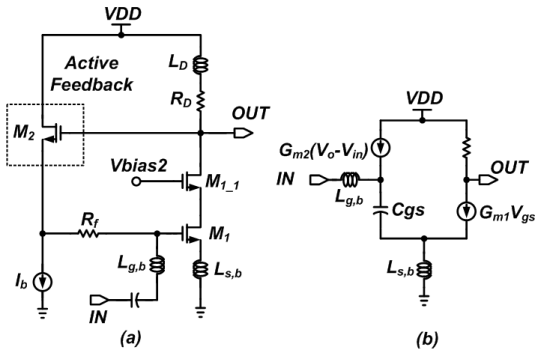


Fig. 2. (a) Wide-band active feedback LNA, (b) Small signal equivalent circuit.

signal equivalent circuit [4]. Similar to the previously reported dual feed wide-band LNA [5], the voltage-current feedback provides the input impedance of 50 ohm, which is equal to R_f divided by the voltage gain, whereas the noise increase slightly because of high R_f. Consequently, the active feedback topology gives wide-band input matching and low noise performance. Also, in order to obtain a broadband response, the shunt peaked load is employed for the output load using the R_D and L_D, since the inductorless wideband LNA is limited by parasitic input capacitance of the subsequent stage.

The S2D amplifier consists of two stages. The first stage converts a single ended signal to differential one and the following fully differential stage behaves as the source follower buffer. The RFVGA is a conventional differential amplifier with digitally controlled shunt switches for the gain control [6].

The RF power splitter distributes the power to the following ASP blocks and has 4 differential output port, as shown in Fig. 3. The 4-way splitter uses the shunt peaking inductor to compensate for the parasitic capacitance at the output node and achieve the wide band

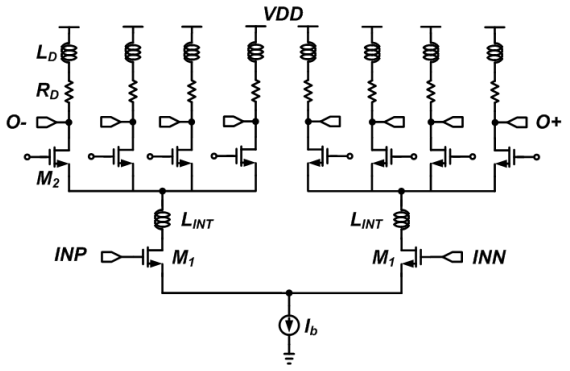


Fig. 3. 4-way active RF power splitter.

characteristics. Because the power splitter contains the physically long interconnection lines due to the large size of on-chip inductor, the gain and phase mismatch between the channels would happen and make it hard to achieve the equivalent time sampling. Therefore, considering the effect of interconnection lines in the circuit design is very important and the design assisted by EM simulation is indispensable.

2. Analog Signal Processing Block

Because the ASP block should sample the very fast UWB impulse signal, the T&H circuit as the first stage of ASP is very important. Fig. 4(a) shows the proposed T&H circuit that enables the wide band sampling up to 5 GHz using cross coupled feedback and shunt peaking topology. Even though the previously used track & hold circuit uses the inductor shunt peaking as shown in Fig 4 (b), it is very difficult to achieve the sufficient wide band characteristics. The output impedance of the cross coupled pair can be driven as following eq. (1).

$$Z_{OUT} = \frac{-1}{g_m}\left[1+\frac{g_m}{s2C_s}\right] \tag{1}$$

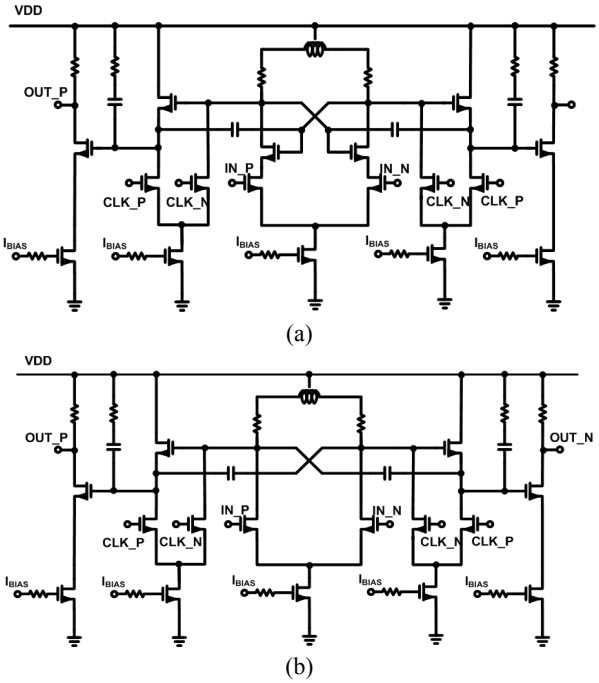


Fig. 4. Track & hold circuits. (a) Proposed T&H circuit using cross coupled pair, (b) Conventional T&H circuit.

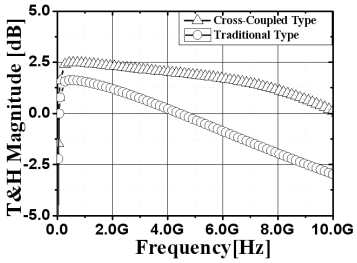


Fig. 5. Bandwidth comparison between proposed cross coupled type and conventional type T&H.

The output impedance is the series combination of the negative resistance and the negative capacitance. As a results, the negative resistance and capacitance generated by the cross coupled pair compensate the output load capacitance (C_{gs} of the following switching gate plus parasitic capacitance) and gives the extension of the gain bandwidth product of the track & hold circuit.

Fig. 5 shows the comparison of the simulated frequency response between the cross coupled type and the conventional shunt peaking topology. It is easily recognized that the proposed cross coupled type combined with the shunt peaking achieves much wider bandwidth than the conventional one.

Following the high speed T&H and S&H, the VGA and integrator circuit amplifies and integrates the received small signal to enhance the signal to noise ratio. As illustrated in Fig. 6, the integrator is a typical active RC circuit with the tunable resistor for the integrator gain control. Finally, the amplified and integrated slow signal is sampled again at the last stage of ASP and handed over to the digital processing part.

Fig. 7 shows the simulated transient result of T&H circuit output using the generated UWB signal source. The T&H circuit of each channel can sample the impulse signal at each 50 ps offset timed instance and hold each voltage value. This allows the sample of 200 ps period with the 50 ps resolution, and ultimately, the scanning time of the radar chip becomes four times faster than the single channel architecture.

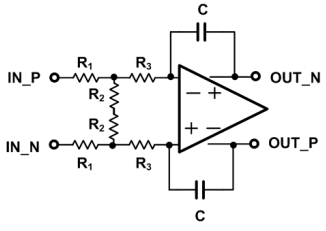


Fig. 6. Integrator circuit for UWB ASP.

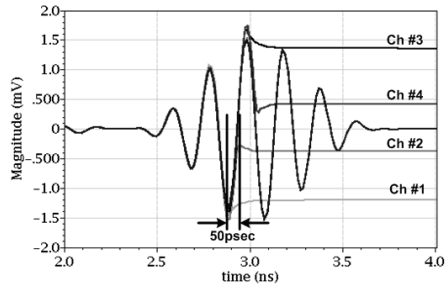


Fig. 7. Transient result of cross coupled type T&H.

3. Delay Loop Lock

In the equivalent time sampling architecture, the timing circuitry is the most important circuit block and determines the accuracy of ranging discrimination. The equally spaced clocks are generated in DLL. Two DLLs as shown in Fig. 8 are used so that one is for the coarse

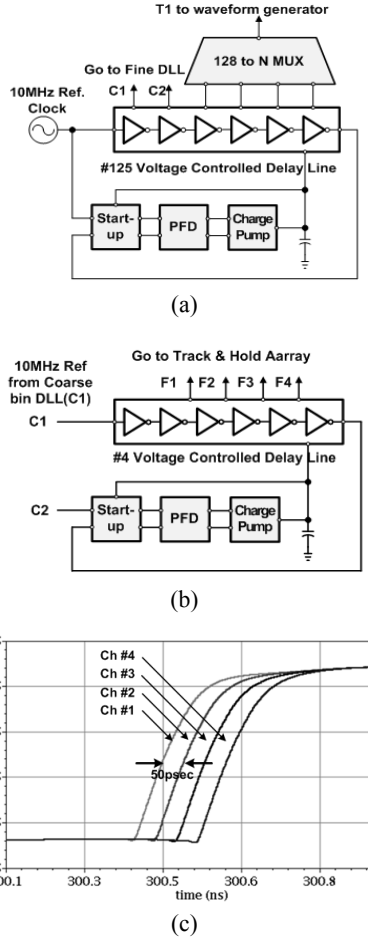


Fig. 8. (a) Coarse bin DLL, (b) Fine bin DLL, (c) Simulated offset-timed clocks of fine bin DLL.

range bins (CB) and the other for the fine range bins (FB). The coarse range bins needs 200 ps time spaced clocks and the fine range bins 50 ps spaced clocks, which is equal to the 200 ps divided by the number of the channels. The external 10 MHz clock generated by crystal oscillator is used as the reference clock for the CB DLL and one of the output clocks of CB DLL is used as the reference clock for the FB DLL. The circuit topology of DLL is a conventional analog DLL type using voltage controlled delay line (VCDL) cell. The Fig. 8(c) shows the simulated offset-timed clocks generated from FB DLL circuit and the 50 ps offset can be achieved.

4. Pulse Generator

The LC oscillator based UWB impulse generator has drawbacks such as restriction of the center frequency tunable range caused by LC tank Q, higher current consumption, and large chip size due to on chip inductor. However, since our target frequency is temporarily 3-5 GHz and will be extended to 3-10 GHz, the digital impulse generator is chosen rather than the oscillator based pulse generator. The pulse generator using a digital logic uses the very small time delay (τ) cell to obtain the high center frequency [7]. Fig. 9 shows the simplified block diagram of the proposed pulse generator. The pulse generator consists of a time delay cell, pulse detector and combiner, and then the generated pulses are amplified through the driver amplifier. The delay cell provides a variable time delay signal to D-F/F array and then the delayed signals through D-F/Fs are detected by EX-OR. The center frequency is determined by the delay time (τ) and the number of pulse decides a frequency bandwidth.

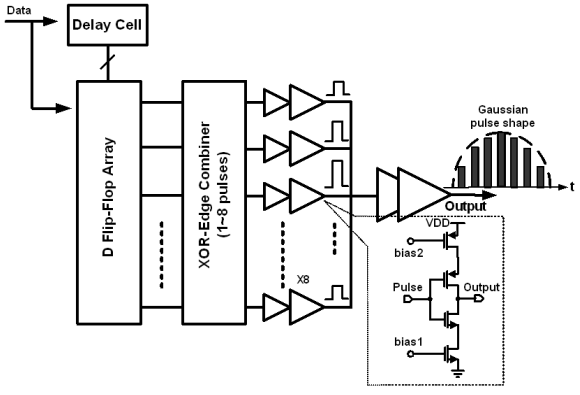
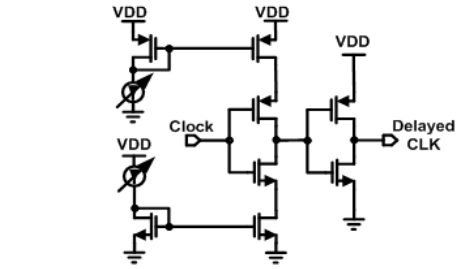
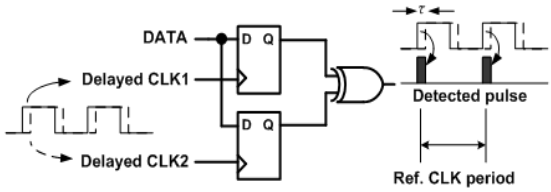


Fig. 9. Simple block diagram of UWB pulse generator.



(a)



(b)

Fig. 10. (a) Schematic of a time delay cell, (b) Pulse edge detector of a pulse generator.

Therefore, the center frequency and bandwidth are trimmable by controlling the delay time and number of pulses. Fig. 10 shows the time delay cell and the pulse detector. The delay cell adopts the inverter topology with current steering, which is controlled to delay the reference clock signal (10 MHz) provided from DLL by increasing or decreasing a current and the delayed clock is delivered to pulse detector array. The D-F/F and EX-OR are detecting a difference between delayed clocks. Finally, the center frequency is determined by a detecting pulse (1/2 τ) and number of pulse (N) decides a bandwidth. For instance, to generate 4 GHz impulse of 500 MHz bandwidth, the required delayed time is 125 ps (τ) and the pulse duration is 2 ns for 500 MHz bandwidth which requires the eight pulses. The digitally generated pulses have a high side lobe in the frequency spectrum inherently. This side lobe should be rejected as much as possible due to its effect to the other bands. In general, to obtain pure main lobe, the band pass filter (BPF) is needed at output. To solve these problems, our impulse generator employs a Gaussian pulse shaping topology. The Gaussian pulse shaping makes a side lobe to be suppressed greatly than the main lobe. Our Gaussian pulse shaper has the parallel connected different sized amplifiers to achieve the different amplitudes, respectively. The Gaussian pulse shaper is shown in Fig. 9. The generated pulse train is added at output node of the Gaussian pulse shaper. Therefore, the Gaussian pulse

shaper is carefully designed considering the parasitic capacitance of the output node to obtain the proper amplitude of the impulse. And then the generated pulses are amplified by the inverter buffer and power amplifier. The power dissipation of the output amplifiers accounts for a large proportion of the total power consumption of the transmitter. The matching of the output DA is carried out using off chip components.

IV. MEASURED RESULTS

The UWB radar chip is fabricated using 0.13 μm CMOS process. As shown in Fig. 11, the measured gain and NF of the RF front-end are 17 dB and 9.5 dB, respectively. The s-parameters of RF front end are measured with the auxiliary buffer amplifier only for the test purpose. Due to the unexpected parasitic effects, the gain and NF degrades drastically above 5 GHz. The operation of the DLL is only measured at the control voltage of VCDL cell and we checked whether the DLL is under lock or not. Fig. 12 shows ASP output signal when the RF receiver input is 3 GHz + 5 kHz CW signal instead of the UWB impulse. The integration time is 10 μs or 100 kHz clock is used for the integrator while the 10 MHz clock is used for T&H circuit. The 3 GHz RF signal is sampled at the high speed T&H and S&H, and integrated 100 times during 10 μs. The 5 kHz offset frequency introduces the small offset frequency relative to the integrator reference clock and the low frequency (5 kHz) sinusoidal output, which is the integrated voltage, is monitored in the oscilloscope as shown in Fig. 12. Even though the measurement is performed with CW input instead of the real UWB impulse, the measured waveform assures that the 3 GHz RF signal is properly sampled and integrated in accordance with the clock

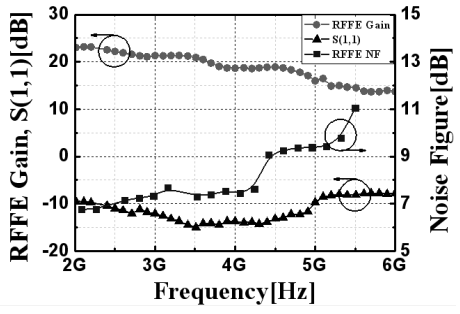


Fig. 11. Receiver measured result.

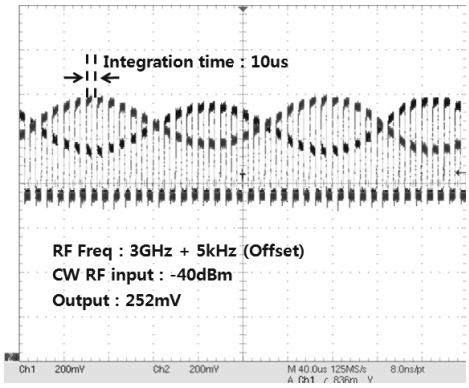


Fig. 12. Measured output of one ASP channel.

Fig. 13. Measured spectrum of UWB Transmitter.

generated by DLL and externally provided clock for the integrator.

Fig. 13 presents the measured spectrum of the transmitter and the UWB impulse has -41.4 dBm/Hz power density at 4.2 GHz and satisfies FCC EIRP regulation. The overall power consumptions of UWB radar receiver and transmitter are 71 mA and 38 mA at 1.5 V supply, respectively. Table I summaries the measured UWB radar chip performance. Fig. 14 shows

Table 1. The Measurement summary of the UWB radar chip

Technology Total Chip area	Chartered 0.13 um CMOS 14.86 mm^2
RFFE Gain (from LNA to splitter)	17 dB
Rx frequency range	3~5 GHz
Noise figure	< 9.5 dB
Rx current consumption	71 mA @1.5 V
DLL lock time	< 1 μs
DLL fine bin timing delay(simulation)	50 ps
Pulse repetition frequency	10 MHz
Tx operating frequency	3~5 GHz
Tx current consumption	38 mA @1.5 V
Fine range bin resolution(expected)	7.3 mm
Radar range(expected)	< 15 m
Max integration time	450 μs
PSD(Power Spectral Density)	-41.4 dBm/MHz

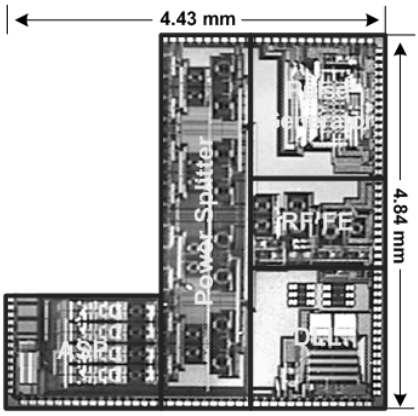


Fig. 14. Fabricated Chip Photo.

the die photograph of the fabricated UWB radar chip. The chip size including pads is 4.4×4.8 mm^2.

V. CONCLUSIONS

In this paper, a 0.13 μm CMOS UWB radar chip adopting equivalent time sampling architecture is presented. In order to reduce the required scan time for 15 m range, the time interleaved sampling is also employed and is realized using multi-channels ASP. Although the digital signal processing part is missing and the full measurement is not achieved, the measured RF and analog performance provided in this paper shows the feasibility of the UWB radar with sub-cm resolution for the various applications such as the surveillance and biometric sensors.

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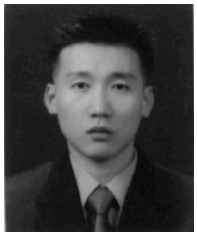
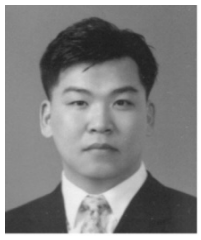
Seung Jun Lee was born in Seoul, Korea, in April 1980. He received B.S. and M.S. degrees in electronics engineering from Kwangwoon University in 2006, 2009, respectively. Since 2009, he has been working toward the Ph.D. degree at the same university. His research interests are on Ultra Wide Band transceiver systems design and RF/Analog integrated circuit and systems design in CMOS technology.

Jong Ok Ha received the B.S. and M.S. degrees in electronics engineering from Kwangwoon University, Seoul, Korea, in 2008 and 2010, respectively, and is currently working toward the Ph.D. degree at Kwangwoon University. His research is focused on CMOS analog integrated circuits and high-speed analog-to-digital converters for wireless applications.



Seung Hwan Jung received B.S. and M.S. degrees in electronics engineering from Kwangwoon University in 2006 and 2008, respectively. Since 2008, he has been working toward the Ph.D. degree at the same university. His research interests are on Ultra Wide Band transceivers and RF/Analog integrated circuits in CMOS technology.

Hyun Jin Yoo received the B.S. and M.S. degrees in Dep. of electronics engineering from Kwangwoon University, Seoul, Korea, in 2006 and 2009, respectively, and is currently working toward the Ph.D. degree at Kwangwoon University. His research is focused on CMOS power amplifier and transmitter design for ZigBee, Wireless LAN and Ultra Wide Band applications.



Young-Hoon Chun (IEEE Member since 2000) received the B.Sc, M.S. and Ph.D. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1993, 1995 and 2000, respectively.

From 2000 to 2005, he was a research staff of the Millimeter-Wave Innovation Technology (MINT) Research Center, Dongguk University, Seoul, Korea. During 2004, he was a Visiting Scholar with Heriot-Watt University, Edinburgh, U.K. From 2005 to 2008, he was with the Department of Electronic Engineering, Heriot-Watt University, as a Research Associate. Before joining LIG Nex1, Rep. of Korea in December 2009, he was with the Department of Electronic Engineering, University of Birmingham, UK, as a Research Fellow. He is currently developing Radar systems as a Principal Research Engineer since he joined. His research area includes Radar systems, sub-systems, Microwave front-end systems and circuits

Wan-Sik Kim received his B.S., M.S. and Ph.D. degrees in Electronic Engineering from Konkuk University, Seoul, Korea in 1991, 1993 and 2005, respectively. He is currently research engineer at LIG Nex1 Co., Ltd. His main research interests are currently MMIC, Millimeter-Wave and Radar systems.

Noh Bok Lee received the B.S. and M.S. degree in Computer Science from Chung-Ang University, Korea, respectively in 1986 and 1990, and Ph.D. in Software Engineering from KAIST in 2005. He is currently a principal research engineer at Agency for Defense Development, Korea and the project manager of the Wireless Sensor Network Systems for Surveillance and Reconnaissance. His interests are in Wireless Sensor Networks and μ- UWB fields.

Yun Seong Eo (M'05) received the B.S., M.S., and Ph.D. degrees all from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993, 1995, and 2001, respectively.

From 2000 to 2002, he was with the LG Electronics Institute of Technology, Seoul, Korea, where he was involved in designing RF integrated circuits (RFICs) such as VCOs, LNAs, and power amplifiers (PAs) using InGaP HBT devices. In September 2002, he joined the Samsung Advanced Institute of Technology, Yongin, Korea, where he developed 5-GHz CMOS PAs and RF transceivers, and was also involved in the development of 900-MHz RF identification (RFID) and 2.4-GHz ZigBee RF transceivers. In September 2005, he joined Kwangwoon University, Seoul, Korea, where he is currently an Associate Professor with the Electronics Engineering Department. During the recent 6 years in Kwangwoon University, he developed so many CMOS RF transceiver ICs for the various applications such as WPAN UWB/ZigBee, T-DMB, DVB-H, WiFi, and Cognitive Radio. In 2009, he founded Silicon R&D inc., where he has developed a CMOS-based UWB RF transceivers and radar chips. His current interest includes UWB RF transceivers for location-based systems, UWB radar chips for surveillance applications and sensors, and low power ZigBee RF transceivers.