A Programmable Compensation Circuit for System-on-Chip Application

Woo-Chang Choi* and Jee-Youl Ryu**

***Abstract*—This paper presents a new programmable compensation circuit (PCC) for a System-on-Chip (SoC). The PCC is integrated with 0.18-μm BiCMOS SiGe technology. It consists of RF Design-for-Testability (DFT) circuit, Resistor Array Bank (RAB) and digital signal processor (DSP). To verify performance of the PCC we built a 5-GHz low noise amplifier (LNA) with an on-chip RAB using the same technology. Proposed circuit helps it to provide DC output voltages, hence, making the RF system chain automatic. It automatically adjusts performance of an LNA with the processor in the SoC when it goes out of the normal range of operation. The PCC also compensates abnormal operation due to the unusual PVT (Process, Voltage and Thermal) variations in RF circuits.**

***Index Terms*—System-on-Chip (SoC), programmable compensation circuit (PCC), low noise amplifier**

I. INTRODUCTION

A recent trend in advanced wireless communication system is to integrate all of the radio frequency (RF) and mixed-signal devices on a single chip. This trend contributes to high density system-on-chip (SoC) with higher performance and reliability. RF and mixed-signal test engineers and designers in SoC field are mainly concerned with unusual process, voltage and thermal (PVT) variations in RF circuits since these variations are hard to distinguish from acceptable variations and lead to a significant performance loss that violates the circuit's specification [1-2]. Therefore, once chips are fabricated and packaged, some sophisticated compensation techniques need to be applied to adjust performance from chips with the PVT variations. In spite of the considerable research underway to solve these problems [2-11], the IC industry is still seeking more suitable technique.

This paper presents a novel low-cost alternative for RF SoC testing to adjust PVT variations. The alternative approach utilizes programmable compensation circuit (PCC). The main part in proposed system involves RF Design-for-Testability (DFT) circuit and Resistor Array Bank (RAB). The RF DFT circuit helps it to provide DC output voltages, hence, making the compensation system automatic. Proposed circuit is very useful for concurrent RF ICs in a complete RF system environment.

II. PROGRAMMABLE COMPENSATION CIRCUIT

1. Compensation Circuit Configuration

Fig. 1 indicates the SoC transceiver configuration with a programmable compensation circuit (PCC) for an RF front-end. The PCC contains RF DFT circuit, RAB and digital signal processor (DSP). The proposed circuit automatically adjusts and compensates performance of the LNA and power amplifier (PA) by the processor when the LNA and PA go out of the normal range of

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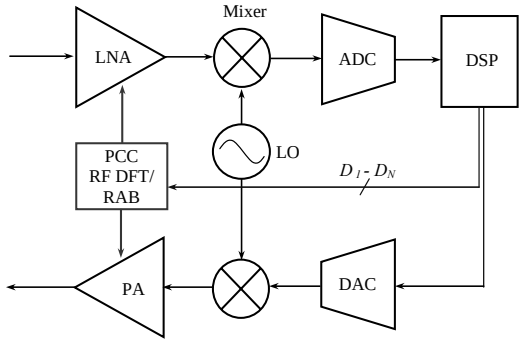


Fig. 1. SoC transceiver configuration with a PCC.

operation due to the unusual PVTs. The RF DFT circuit helps it to provide DC output voltages, thus, making the network automatic.

Fig. 2 shows test set-up to realize our idea shown in Fig. 1. Our proposed PCC provides DC outputs so that all of the measurements can be done by on-chip data converter within the SoC, hence making the measurement automatic. It contains RF circuits with RAB and RF DFT circuit all on a single chip. The test structure can be automatically configured by the external data acquisition hardware. The complete test-bed contains RF source (v_{in}) with source resistance (R_s), RF relays (*S1, S2* and *S3*), load impedance (Z_L), and a data converter board. The measurement set-up contains very low-loss RF relays and input transmission matching to the RF and DFT circuits. The positions of the relays were controlled to measure the output DC voltages and phase, V_{T1}, V_{T2}, and $\Delta\theta_T$ through the DFT circuit, respectively. These relays were controlled by DeMux chip on external board.

The RF DFT circuit contains a test amplifier (TA), a band-gap reference circuit, two RF peak detectors (PD1 and PD2) and a RF phase detector (PHD) as shown in Fig. 3. This additional circuit occupies a very small area

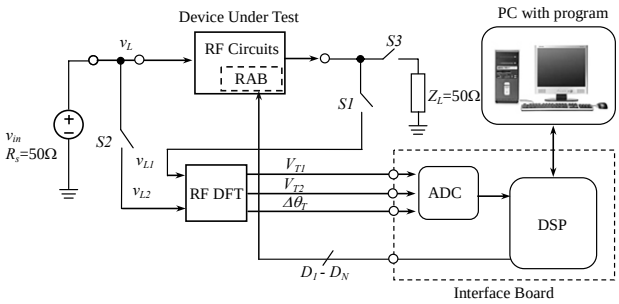


Fig. 2. Measurement set-up of the PCC for an RF circuits.

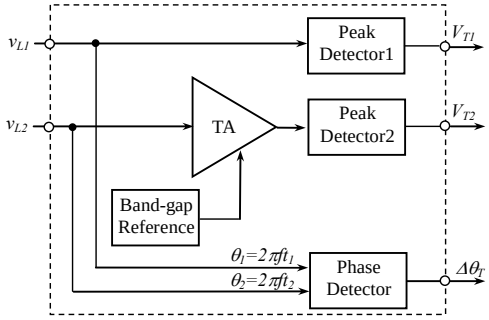


Fig. 3. RF DFT circuit.

less than 5% on the SoC, and it helps to measure LNA performance without expensive external equipment. Two RF peak detectors and a RF phase detector are used to provide DC output voltages (V_{T1} and V_{T2}) and phase difference ($\Delta\theta_T$), respectively.

2. Case Study

In this paper, we studied the testing of RF amplifiers. Our RF test strategy involves the derivation of mathematical equations for many RF device specifications. These mathematical equations contain DC parameters and thus provide values that are comparable to actual measured values using expensive RF equipment. The following sections describe mathematical descriptions of these parameters using DC output voltages. We present the equations for both defective and defect-free cases.

A. Input Impedance

The input impedance measurement is performed with the switch *S2* in closed position and the switch *S1* in open position from Fig. 2. The overall test technique is to find any deviations between the source impedance (R_s) and the input impedances of the RF amplifier and test amplifier. For example, the test amplifier is designed to find changes in input impedance of the RF amplifier for any mismatch with the source resistance. Due to the PVT variations, DC voltage and phase at the output of RF DFT may be changed.

1) Case Study I: Defect-free RF Amplifier

Consider a defect-free RF amplifier with perfectly matched input impedance, i.e., 50 Ω. The theoretical value of the voltage across the input impedances of the

LNA (Z_1) and test amplifier (Z_2) is expressed by $V_t = \frac{Z_1}{2Z_1 + R_s} V_{in}$. The gain of the test amplifier (G_2) is designed to be three to sufficiently increase the output voltage swing. The DFT circuit monitors the DC voltage V_{T2} and phase difference $\Delta\theta_T$ as shown in Fig. 2. Using the measured these values, we can use Eq. (1) to calculate the defect-free RF amplifier impedance, Z_1,

$$Z_1 = \frac{K_1(R_s Z_2)}{K_1(R_s - Z_2) + Z_2} [\Omega] \quad (1)$$

where K_1 is the multiplying constant obtained from the voltage gain.

2) Case Study II: Defective RF Amplifier

We now consider PVT variations in RF circuits [1]. In this case, there is a certain variation in input impedance of RF amplifier due to changes in its input matching condition. This condition provides a new value in V_{T2} and $\Delta\theta_T$. The input impedance of the RF amplifier in defective conditions can be expressed as

$$Z_1^{'} = \frac{K_1^{'}(R_s Z_2)}{K_1^{'}(R_s - Z_2) + Z_2} [\Omega] \quad (2)$$

where $K_1^{'}$ is the multiplying constant obtained under defective conditions.

B. Other Expressions

We have derived two additional mathematical equations for possible RF specifications for the RF amplifier by considering defective and defect-free conditions [12]. These mathematical equations are summarized in Table 1.

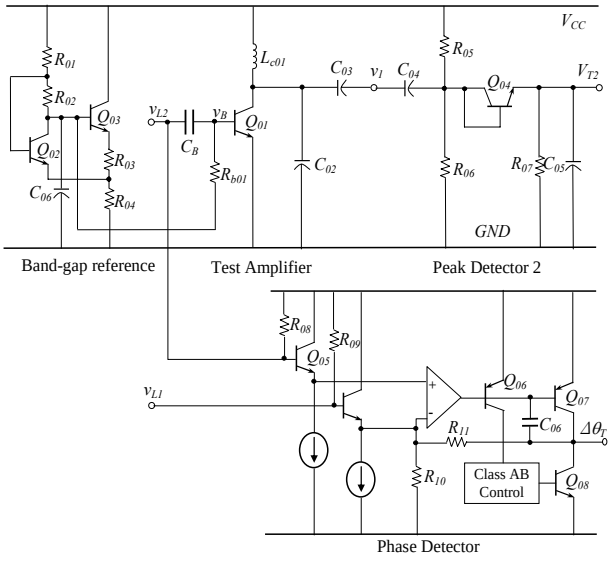
Table 1. Mathematical expressions for RF DFT circuit

Parameters	Defect-free	Variations
Input Impedance	$Z_1 = \frac{K_1(R_s Z_2)}{K_1(R_s - Z_2) + Z_2} [\Omega]$	$Z_1^{'} = \frac{K_1^{'}(R_s Z_2)}{K_1^{'}(R_s - Z_2) + Z_2} [\Omega]$
Voltage Gain	$G_1 = G_{01}\left(1 + \frac{R_s}{Z_1}\right)$	$G_1^{'} = G_{01}^{'}\left(1 + \frac{R_s}{Z_1}\right)$
Noise Figure	$NF = 1 + \left(\frac{Z_1}{R_s + Z_1}\right)^2 \cdot \alpha$	$NF^{'} = 1 + \left(\frac{Z_1}{R_s + Z_1}\right)^2 \cdot \alpha^{'}$

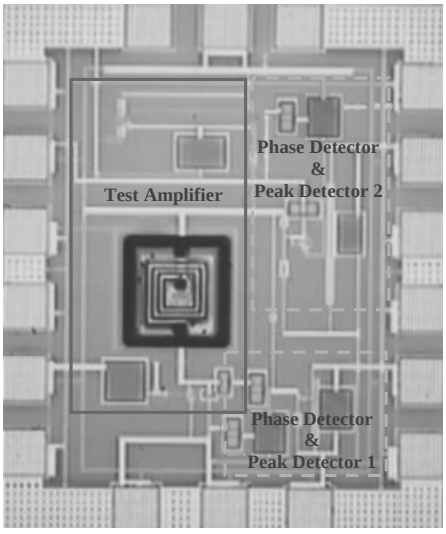
3. PCC Design

The proposed RF DFT circuit is shown in Fig. 4, and it is designed using 0.18 μm SiGe technology. It consists of TA, PD1, PD2 and PHD circuits. The PD1 circuit is also a part of the DFT circuit and it has the same topology as the PD2 circuit shown in Fig. 4(a). The test amplifier is designed with the input and output impedances of 50 ohms, respectively. The gain of the test amplifier is designed to be 3 to increase the output voltage level. The RF peak detectors are used to convert RF signal to DC voltage. To detect phase difference ($\Delta\theta_T$) an RF phase detector are used. The output minimum voltage of phase detector provides 30 mV for phase difference of 180 °. The output maximum voltage of phase detector provides 1.8 V for phase difference of 0 °. When $\theta_2 = \theta_1 \pm 90$ °, phase center point is 900 mV. The output current drive for source/sink condition is 6 mA, and slew rate is 50 V/μs. The small signal envelope bandwidth is 30 MHz, and the response time for 15 ° change condition (10%~90%) is 20 ns. The bias stage utilizes a band-gap reference circuit for a low-supply voltage and a low-power dissipation. The inductor (L_{c01}) is used for matching input and output impedances. The bias resistors (R_{05} and R_{06}) shown in Fig. 4 are used to keep transistor Q_{04} in the active region so that the transistor acts as a rectifier. The diode connections have the advantage of keeping the base-collector junction at zero bias [11-12]. To reduce the output-ripple voltage, large values were chosen for R_{07} and C_{05}.

Fig. 5 shows details of the proposed RAB. It has N-bit resistor banks to accurately compensate an RF amplifier performance. In this approach, we have designed an 8-bit RAB considering a chip area overhead. The resistor bank is controlled by using digital signals ($D_8 \ldots D_2 D_1$) from the digital signal processor (DSP). The input data streams of ($D_8 \ldots D_2 D_1$) = (0…01) for $8R_b$ and (1…11) for R_b have been used to compensate RF amplifier performance, respectively. The R_b is under defect-free value. It was designed with LNA on a single chip using 0.18 μm SiGe technology to demonstrate this idea. It is powered by 1.8-V supply voltage. It was designed to have separate supplies for RF and digital sections of the chip to isolate the RF circuitry from the switching noise introduced by the digital supplies. The chip divided into



(a) Schematic diagram



(b) Chip micrograph

Fig. 4. Schematic diagram of an RF DFT.

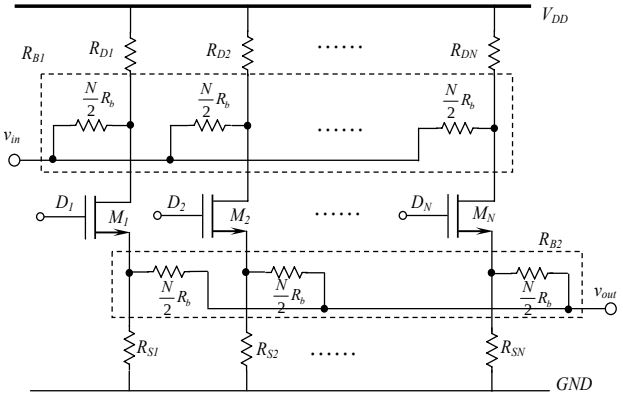
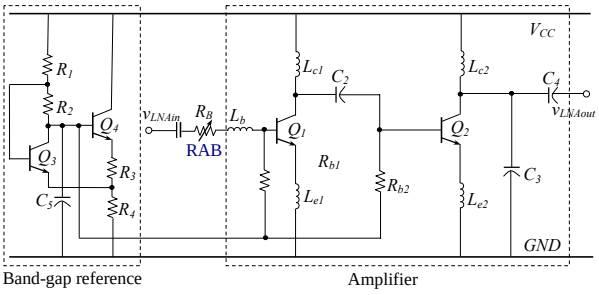


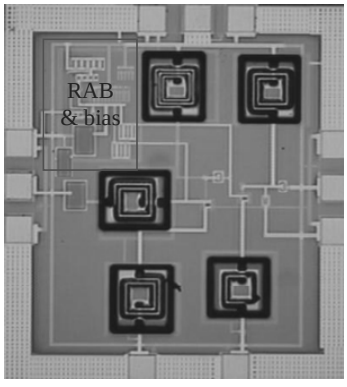
Fig. 5. N-bit RAB circuit.

RF and digital sections with different substrate grounds is divided to attenuate noise coupling from one area of a chip to another. The distributed gate resistance of the MOS devices contributes to the thermal noise [11]. To minimize this resistance, the transistors M_1~M_8 were laid out as a parallel combination of many narrower devices. The transconductances of the transistors were minimized to reduce the input-referred noise voltage related to the thermal noise. These transistors in MOS switches, are designed for operating in the deep triode region so that they exhibit no dc shift between the input and output voltages. The resistors, R_{D1}~R_{S8} were used to control a dc bias voltage of MOS switches.

To verify the performance of our proposed PCC, the two-stage LNA was designed. It is designed for a 5-GHz IEEE802.11a wireless LAN application. Fig. 6(a) and (b) show the schematic and chip micrograph of the 5-GHz LNA, respectively. It is powered by a 1-V supply. The bias stage utilizes band-gap reference circuit. It controls base currents for the first and second stages. The complete design consists of four HBTs, five inductors, five capacitors and six resistors, all on a



(a) Schematic diagram



(b) Chip micrograph

Fig. 6. Schematic diagram of RF amplifier with RAB.

single chip. The physical chip area is approximately 1.5 mm × 1.5 mm.

4. Development of Algorithm

Fig. 7 shows the flowchart of the PCC for the LNA performance. Our approach has three-step process to compensate LNA performance. The first step is to measure simple outputs V_{T1}, V_{T2}, and $\Delta\theta_T$ using proposed DFT. The second step is to compare measured outputs V_{T1}, V_{T2}, and $\Delta\theta_T$ with reference values, $V_{T1(ref)}$, $V_{T2(ref)}$, and $\Delta\theta_{T(ref)}$ in look-up table (LUT), respectively. Finally, the programmable compensation step is applied to adjust LNA performance when the LNA has PVT variations. If measured V_{T1}, V_{T2}, and $\Delta\theta_T$ have more than ±2% of the reference values, $V_{T1(ref)}$, $V_{T2(ref)}$, and $\Delta\theta_{T(ref)}$, they are automatically compensated. It compensates specific LNA specifications such as input impedance, gain and noise figure as listed in Table 1.

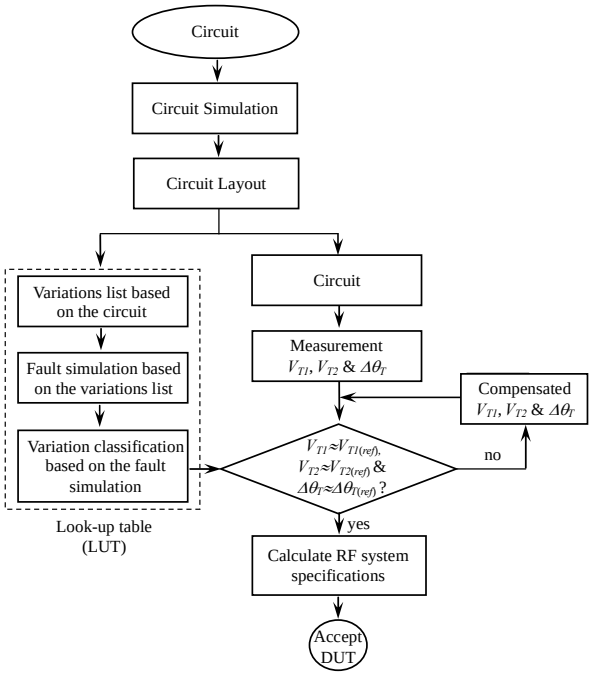


Fig. 7. The flowchart for the PCC.

III. Measurement Results

The PVT defect testing of RF amplifier involves expensive measurement equipment. Our RF DFT circuit provides DC voltages (V_{T1} and V_{T2}), which can be used to find LNA specifications through the mathematical expressions shown in previous section. We were able to adjust RAB with the LNA circuits by providing a combination of digital codes to the resistor array banks.

As process variations, we identified the most sensitive inductor component L_{c1} shown in Fig. 6(a) that contributed to varying LNA voltage gains. We also considered temperature variations of -20 °C to 70 °C that contributed to varying LNA noise figures. As the worst case, we investigated coupled variations with all PVT variations. For these four cases, our results verify that the proposed PCC automatically adjusts and compensates LNA performance such as gains and noise figures.

The $V_{T1(ref)}$, $V_{T2(ref)}$, and $\Delta\theta_{T(ref)}$ measured at output of the DFT circuit are shown in Table 2. The results show average values from 10 times experiments, and PVT variations of within less than ±2% for defect-free values are accepted. These values are measured after 40 nanoseconds settling time of the PD1, PD2, and PHD to ensure steady-state value. These results are used to obtain input impedances, voltage gains and noise figures of the LNA as shown in Table 1. As can be expected from simulation results, since the $V_{T1(ref)}$ is proportional to LNA gain, the $V_{T1(ref)}$ has the highest value at the operating frequency of 5 GHz. The $\Delta\theta_{T(ref)}$ showed small difference at 5.25 GHz. This value means perfect matching status at this frequency. When the frequency is increased, the $V_{T2(ref)}$ is also increased. As shown in Table 2, the measurement showed similar difference compared to the simulation. However, the measurement result showed the maximum values at a lower frequency than the simulation. This frequency shift may be a result of parasitic effects at high frequency [10-12].

Table 2. $V_{T1(ref)}$, $V_{T2(ref)}$ and $\Delta\theta_{T(ref)}$ measured by the RF DFT circuit

Frequency [GHz]	$V_{T1(ref)}$ [mV]		$V_{T2(ref)}$ [mV]		$\Delta\theta_{T(ref)}$[°]	
	Simulation	Measurement	Simulation	Measurement	Simulation	Measurement
4.50	400	343.8	166.20	205.3	-24	-20
4.75	421	335.7	160.30	218.2	-16	-11
5.00	448	304.8	171.40	213.4	-8	-2
5.25	445	274.9	180.00	205.4	0	2
5.50	432	253.0	189.00	182.3	8	4
5.75	418	232.0	191.05	168.1	16	10
6.00	406	219.1	192.02	160.2	24	16

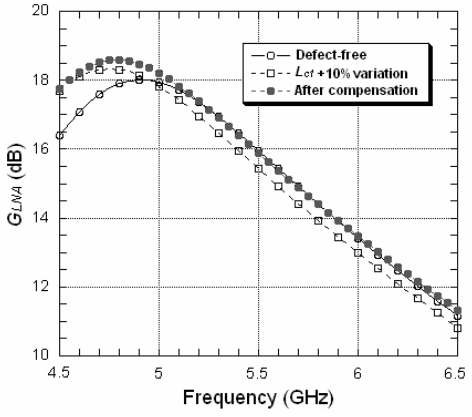
1. Process Variations and Compensations

Fig. 8 shows the compensation results for a +10% process variation of the most sensitive component (L_{c1}) in LNA shown in Fig. 6(a). Defect-free values are obtained using the results of Table 2. The gain compensation shown in this figure was done at the operation frequency of 5.25 GHz. We identified a variation of 0.43 dB in the LNA gain from the +10% process variation. To compensate a 0.43 dB LNA gain, the input data stream of (D_8…$D_4D_3D_2D_1$) = (0…0111) providing R_B = (8/3)(R_b) was applied. The R_b is under defect-free value. The noise figure compensation was also done at 5.25 GHz providing R_B = (8/3)(R_b). The L_{c1}+10% process variation showed a small variation in the LNA noise figure as shown in Fig. 8. We identified a variation of 0.01 dB in the LNA noise figure from the +10% process variation.

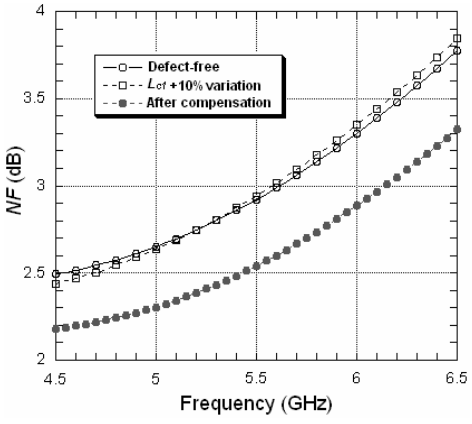
As shown in Fig. 8, the proposed PCC can compensate the gain and noise figure of LNA due to the process variation at 5.25 GHz. The impedance matching network at the LNA input has a significant effect on the noise figure [1]. This significant improvement reveals that the input impedance matching from the adjustment of R_b after compensation is optimized. The noise figure can be minimized by choosing the optimum base resistor, R_b.

2. Voltage Variations and Compensations

The compensation results for a -0.2 V (V_{cc}=1.8 V) voltage variation in LNA is shown in Fig. 9. The gain compensation shown in this figure was also performed at 5.25 GHz. We identified a variation of 0.08 dB in the LNA gain from the -0.2 V voltage variation. To compensate a 0.08 dB gain variation, the input data stream of (D_8…$D_4D_3D_2D_1$) = (1…1111) providing R_B = R_b was applied. The -0.2V voltage variation showed 0.021 dB variation in the noise figure.

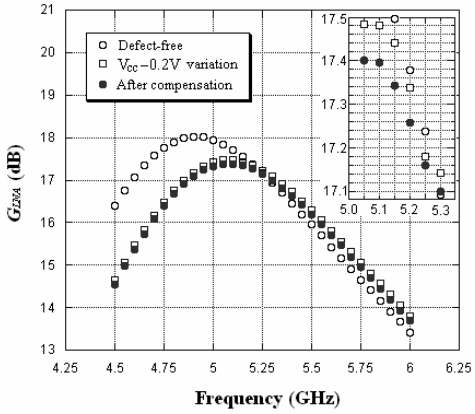


(a) Gain compensation

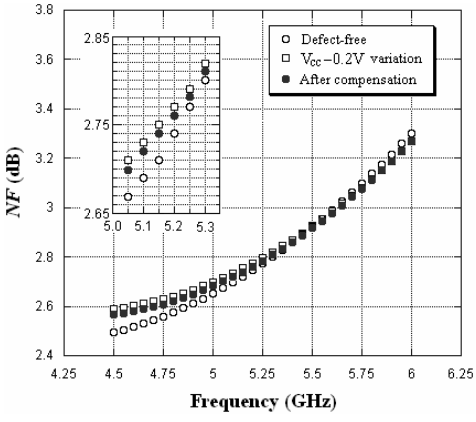


(b) Noise figure compensation

Fig. 8. Compensation for +10% process variation of inductor, L_{c1}.



(a) Gain compensation



(b) Noise figure compensation

Fig. 9. Compensation for -0.2 V variation of supply power, V_{cc}.

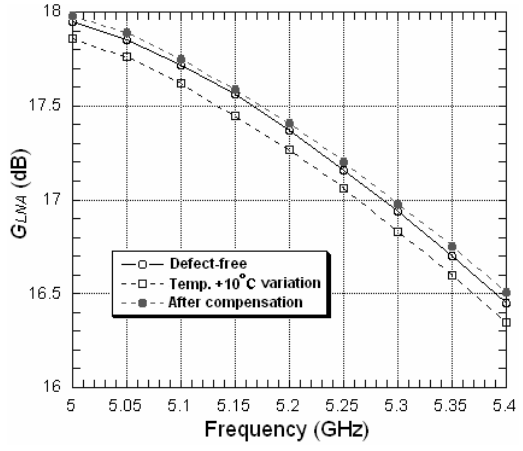
As can be seen from Fig. 9, the proposed PCC can compensate the gain and noise figure of RF amplifier due to the voltage variation.

3. Temperature Variations and Compensations

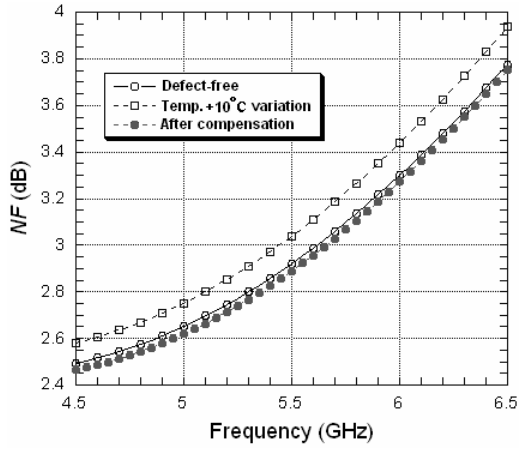
Fig. 10 shows the gain variation and its compensation results for the +10 °C temperature variation. The gain compensation was done at 5.25 GHz. We identified a variation of 0.101 dB in the gain from the +10 °C variation. The input data stream of $(D_8 \ldots D_2 D_1)$ = (0…01) providing R_B = (8/5)(R_b) was applied to compensate a 0.101 dB gain variation. The +10 °C temperature variation showed 0.106 dB variation in the noise figure. As shown in Fig. 10, the proposed PCC can compensate the gain and noise figure of LNA for the temperature variation.

4. Coupled Variations and Compensations

Fig. 11 shows the gain variation and its compensation results for the L_{c1}+10% process, -0.2 V voltage, and +10 °C temperature variations. The gain compensation shown in this figure was also done at 5.25 GHz. We identified a variation of 0.842 dB in the gain from the coupled variations. To compensate a 0.842 dB gain, the input data stream of $(D_8 \ldots D_4 D_3 D_2 D_1)$ = (0…0111) providing R_B = (8/3)(R_b) was applied. The variation of 0.365 dB in the noise figure for these variations was provided. As can be seen from Figure 11, the proposed PCC can compensate the gain and noise figure of LNA due to the coupled variation at 5.25 GHz. This significant improvement in the noise figure reveals that the input impedance matching from the adjustment of R_b after compensation is optimized [1].

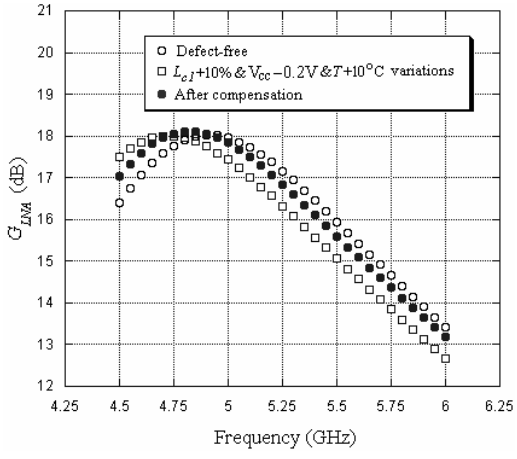


(a) Gain compensation

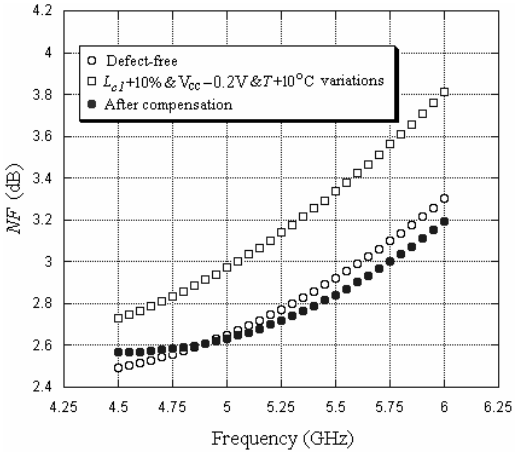


(b) Noise figure compensation

Fig. 10. Compensation for +10 °C variation of temperature.

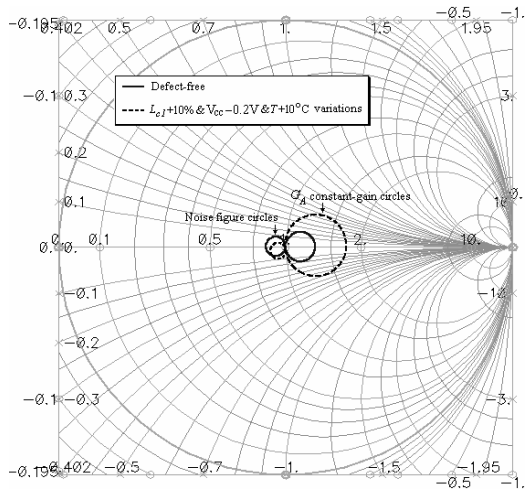


(a) Gain compensation

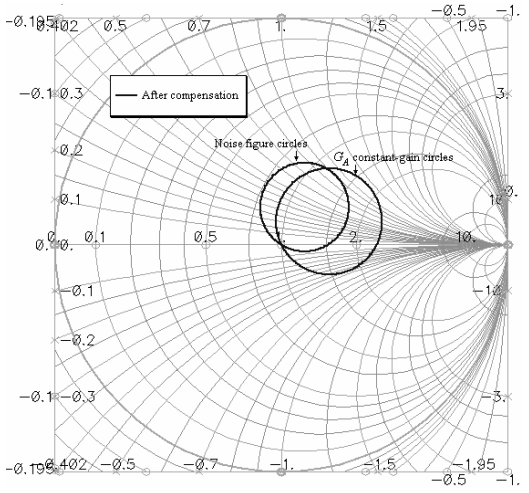


(b) Noise figure compensation

Fig. 11. Compensation for coupled variations.



(a) Coupled variations



(b) Compensation

Fig. 12. G_A and noise figure compensations for parametric variations (Smith Chart).

The constant noise figure circles and constant available power gain (G_A) circles for L_{c1}+10% process, -0.2 V voltage, and +10 °C temperature variations at 5.25 GHz are shown in Fig. 12(a). These circles are drawn in the Γ_s plane. For the process variation, the Smith chart in the Γ_s plane is useful to investigate variations of both gain and noise figure. Maximum gain and minimum noise figure cannot, in general, be obtained simultaneously [2].

As shown in Fig. 12(a), the noise figure circle is decreased and the G_A circle is increased due to the coupled variations. These results support increase of noise figure and decrease of available power gain. Fig. 12(b) shows constant noise figure circle and constant available power gain (G_A) circle after compensation for this coupled variation at 5.25 GHz. These circles are also drawn in the Γ_s plane. After compensation, the noise figure circle moved to clockwise. The phase of Γ_{opt} is approximately 57 °. The available power gain circle moved to counterclockwise. These results reveal decrease of noise figure and increase of available power gain.

Table 3. Comparisons of parametric variations and their compensations

Variations			Compensations			
Components	ΔG_{LNA}(dB)	ΔNF(dB)	Data Codes	R_B	ΔG_{LNA}(dB)	ΔNF(dB)
L_{c1}+10%	-0.431	0.011	(00000111)	$8R_b/3$	0.441	-0.351
L_{c1}+20%	-0.982	0.023	(00000011)	$4R_b$	0.991	-0.382
T+10°C	-0.101	0.106	(00011111)	$8R_b/5$	0.145	-0.140
T+20°C	-0.165	0.189	(00001111)	$2R_b$	0.278	-0.269
T+30°C	-0.277	0.274	(00001111)	$2R_b$	0.278	-0.269
T+40°C	-0.372	0.357	(00000111)	$8R_b/3$	0.441	-0.351
V_{cc}-0.2V	-0.080	0.021	(11111111)	R_b	0.085	-0.015
V_{cc}-0.4V	-0.145	0.085	(00011111)	$8R_b/5$	0.145	-0.040
L_{c1}+10%&T+10°C	-0.545	0.109	(00000111)	$8R_b/3$	0.441	-0.351
L_{c1}+10%&T+20°C	-0.589	0.188	(00000011)	$8R_b/3$	0.441	-0.351
L_{c1}+10%&T+30°C	-0.685	0.223	(00000011)	$4R_b$	0.991	-0.382
L_{c1}+10%&T+40°C	-0.826	0.322	(00000011)	$4R_b$	0.991	-0.382
L_{c1}+20%&T+10°C	-1.025	0.148	(00000001)	$8R_b$	1.121	-0.395
L_{c1}+20%&T+20°C	-1.112	0.285	(00000001)	$8R_b$	1.121	-0.395
L_{c1}+20%&T+30°C	-1.211	0.312	(00000001)	$8R_b$	1.121	-0.395
L_{c1}+20%&T+40°C	-1.312	0.334	(00000001)	$8R_b$	1.121	-0.395
L_{c1}+10%&T+10°C & V_{cc}-0.2V	-0.842	0.365	(00000111)	$8R_b/3$	0.441	-0.351
L_{c1}+20%&T+20°C & V_{cc}-0.4V	-1.214	0.304	(00000001)	$8R_b$	1.121	-0.395

Table 3 summarizes the noise figure and gain variations and their compensation results for the PVT variations. Data codes used for compensation are listed. As can be seen in this table, the proposed PCC showed good compensation results for the various variations of the gains and noise figures.

IV. CONCLUSIONS

This paper proposed a new programmable compensation circuit (PCC) for a System-on-Chip. The PCC was fabricated with 0.18-μm BiCMOS SiGe technology. We successfully proved that our PCC can help to compensate LNA with unusual PVT (Process, Voltage and Thermal) variations. Utilizing our new PCC, we measured gains and noise figures, and it automatically adjusted performance of 5 GHz LNA when it went out

of the normal range of operation. The PCC also provided successful measurement results for LNA chips with Resistor Array Bank (RAB). We believe that this new capability will provide industry with a low-cost technique to test and compensate RFIC chips.

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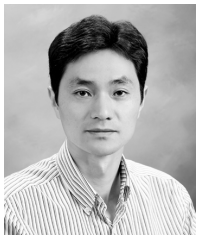

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