Linearity-Distortion Analysis of GME-TRC MOSFET for High Performance and Wireless Applications

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***Abstract*—In this present paper, a comprehensive drain current model incorporating the effects of channel length modulation has been presented for multi-layered gate material engineered trapezoidal recessed channel (MLGME-TRC) MOSFET and the expression for linearity performance metrics, i.e. higher order transconductance coefficients: g_{m1}, g_{m2}, g_{m3}, and figure-of-merit (FOM) metrics; V_{IP2}, V_{IP3}, IIP3 and 1-dB compression point, has been obtained. It is shown that, the incorporation of multi-layered architecture on gate material engineered trapezoidal recessed channel (GME-TRC) MOSFET leads to improved linearity performance in comparison to its conventional counterparts trapezoidal recessed channel (TRC) and rectangular recessed channel (RRC) MOSFETs, proving its efficiency for low-noise applications and future ULSI production. The impact of various structural parameters such as variation of work function, substrate doping and source/drain junction depth (X_j) or negative junction depth (NJD) have been examined for GME-TRC MOSFET and compared its effectiveness with MLGME-TRC MOSFET. The results obtained from proposed model are verified with simulated and experimental results. A good agreement between the results is obtained, thus validating the model.**

Manuscript received May 5, 2011; revised Jul. 22, 2011.
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***Index Terms*—Corner effect, linearity, MLGME, RF, TRC MOSFET**

I. INTRODUCTION

Recent explosion in the demand for mobile telecommunication, computing and multimedia applications has resulted in much interest in system on chip (SOC) applications based on all CMOS technologies due to their inherent low cost and high density. In sub-100 nm regime MOSFETs are the strong contenders for analogue RF applications in lucrative wireless communications market. Linearity assessment [1-3] is an important parameter in all RF systems which need to be tailored in order to ensure that the inter-modulation and high-order harmonics are minimal at the output. Although there are system level techniques to improve linearity, they all require complex circuitry [4]. A transistor-level linearization is more appropriate for power amplifiers in the portable systems, which requires an analysis of linearity behaviour at device level as a function of important design parameters.

The present work concentrates on the extensive study for various recessed channel structures, i.e. RRC, TRC, GME-TRC and MLGME-TRC MOSFETs, for different dielectric configurations to optimize the linearity performance by developing a model and validating it with experimental and simulation results. The Recessed channel (RC) MOSFET [5-7] structures are considered as potential candidates to suppress and overcome short channel effects (SCEs), punch-through and DIBL effects even at gate lengths down to the sub-100 nm regime because negative junctions can be fabricated without any increase in the series resistance and hence, for use in

CMOS ULSI circuits. This is because the recessed channel MOSFETs carries concave device structure in which two potential barriers are formed at the corners due to high density of electric field lines, resulting in improvement of SCEs in terms of reduced punchthrough and drain induced barrier lowering (DIBL) effect. However, these barriers act as hurdle in the path of carriers, because carriers now require more energy to surmount the barriers, which limits its carrier transport efficiency and hence, current driving capabilities of the device. In case of trapezoidal recessed channel (TRC) MOSFET, the height of corner barriers is comparatively low as compared to rectangular recessed channel (RRC) MOSFET, which results in improved device speed and also SCEs suppression [7]. The amalgamation of GME architecture on TRC MOSFET further adds on the enhancement in carrier transport efficiency and reduction in SCEs, owing to the step in potential profile due to the gate electrodes of different metal work functions, i.e. Φ_{M1} for metal M1 and Φ_{M2} for metal M2; thus resulting in screening of channel region, under gate material M1, from drain potential variations [7]. This screening ensures the diminution in DIBL, enhanced carrier transport; reduced hot carrier effect and increased drain current and thus, shows the improved linearity performance as compared to conventional TRC and RRC MOSFETs.

Moreover, for deeply scaled MOS structures, the gate oxide thickness becomes one of the important scaling parameter. Leakage current and tunneling effects will become more prominent as thickness is scaled below 2 nm. The high-*k* films are anticipated to be a viable alternative [8]. However, these films results in high fringing electric field from gate into the source/drain regions thereby degrading the short channel performance [9-12] of the device. This limitation of high-k/SiO_2 system [13-14] can be overcome by using gate stack architecture consisting of a thin passivating layer of SiO_2 between bulk and high-*k* dielectric has been given extensive consideration. Thus, due to the negligible gate oxide leakages and increased carrier transport efficiency, MLGME-TRC MOSFET integrates the potential benefits of GME-TRC MOSFET in terms of high linearity and low distortion behaviour in comparison with conventional MOSFETs in terms of figure-of-merit (FOM) metrics: V_{IP2}, V_{IP3}, IIP3, 1-dB compression point and higher order transconductance coefficients: g_{m1}, g_{m2}, g_{m3}, proving its efficiency for low-noise applications and future ULSI production. Further, to gain an insight into the effectiveness of the proposed design, the characteristics are investigated for different workfunction difference, X_j, dielectric constant (ε_{ox2}), and substrate doping (N_A) in order to study the overall device performance. The results obtained from proposed model are also verified with simulated and experimental results. A good agreement between the results is obtained, thus validating the model.

II. FABRICATION FEASIBILITY OF GME-TRC MOSFET

The MLGME-TRC MOSFET can be fabricated conveniently by using present fabrication technologies and lithographic resolutions. The fabrication of TRC structure is feasible by implementing the fabrication process used by Xiao-Hua et al [16] and Seo et al [17] for grooved gate MOSFET. Further, for GME architecture, many fabrication schemes has been suggested such as inter diffusion process [18, 19] and tilt angle evaporation (TAE) [20, 21] which makes the fabrication possible even in sub-100 nm regime. Moreover, for the viability of advanced multi-layered gate engineered structures, several techniques [22, 23] were reported in the past, using the stack of a thin SiO_2 and a thick high-*k* layer. Thus, with these presented fabrication feasibilities of individual grooved-gate MOSFET, multi-layered and GME architecture, the device fabrication probability of integrated MLGME-TRC MOSFET is enhanced and hence, with advanced lithographic considerations and techniques, its fabrication is possible, so new structure is proposed with its validation.

III. STRUCTURE DESCRIPTION

A schematic cross-sectional view of different recessed channel structures, i.e. MLGME-TRC, GME-TRC, TRC and RRC MOSFETs are shown in Figs. 1(a-d).

The effective channel length L_{eff} corresponds here to the metallurgical channel length, taken along the gate oxide, i.e. $L_{eff}=(2L_s) + L_p$ where, L_p is the planar part and L_s is the angular part of the channel. The substrate doping, N_A, is taken as 1×10^{17} cm^{-3} and source/drain region doping, N_D^+, is 1×10^{20} cm^{-3} and gate length, L_g, is

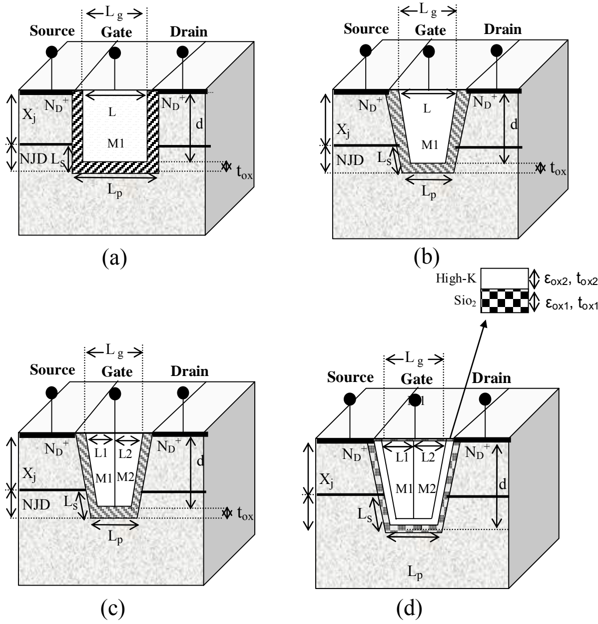


Fig.1. (a), (b), (c) and (d), respectively, shows the schematic structure of RRC, TRC, GME-TRC and MLGME-TRC MOSFETs, where channel length $L_g = L_1 + L_2$=68 nm, with work function difference Φ_{M1}=4.7 V and Φ_{M2}=4.10 V for MLGME-TRC and GME-TRC MOSFET and gate consists of multi-layered-gate dielectrics having a thickness t_{ox1}=2 nm and t_{ox2}=2 nm of the lower and the upper gate dielectrics with the corresponding permittivites, ε_{ox1}=3.9 and ε_{ox2}=20, respectively and for GME-TRC, TRC and RRC MOSFETs t_{ox}=4 nm and $\varepsilon_{ox}=\varepsilon_{ox1}$=3.9. For TRC and RRC MOSFET, channel length L_g=L=68 nm and work function Φ_{M1}=4.7 V having Source/ Drain junction depth (X_j)=10 nm, groove depth d=20 nm, permittivity ε_{ox1}=3.9, $N_A = 1 \times 10^{17}$ cm^{-3}, $N_D = 1 \times 10^{20}$ cm^{-3}. Effective channel length is, $L_{eff}=(2L_s) + L_p$, where, L_p=28 nm and L_s=14 nm for MLGME-TRC, GME-TRC, TRC MOSFETs and L_p=68 nm and L_s=10 nm for RRC MOSFET, unless stated otherwise.

taken as 68 nm for all the devices for fair comparison. The work functions of gate metals M1 and M2 are chosen as 4.77 eV and 4.1 eV, respectively. The study is carried out using ATLAS and DEVEDIT device simulators in order to verify the results of proposed model and a good agreement between their results is obtained. All the device parameters of considered device structures are equivalent, unless otherwise stated.

IV. MODEL FORMULATION

1. Linearity-Distortion Analysis

Low distortion is one of the biggest concerns for current and next-generation wireless communication systems. In order to study the linearity performance, analysis has been carried out in terms of higher order transconductance coefficients and device FOMs: V_{IP2} and V_{IP3} [24], third-order input intercept point (IIP3) [25] and 1-dB compression point, which has been obtained using drain current (I_{ds}-V_{gs}) characteristics with channel length modulation (CLM) effect from sub-threshold to saturation region [26], and is defined as:

$$I_{ds} = \frac{W.\mu_s.C_{oxc}}{\left(L_{eff}-l_d\right).\left(1+\frac{\delta_o.\mu_s.V_{dsx}}{\left(L_{eff}-l_d\right).\nu_{sat}}\right)}.(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).V_{dsx} \quad (1)$$

where, W is the device width, μ_s is the inversion layer mobility of carriers, δ_o is the fitting parameter, α is the Bulk body term, ν_{sat} is the carrier saturation velocity, V_{gs} and V_{ds} are the gate to source voltage and drain to source voltage, respectively and C_{oxc} is the gate oxide capacitance, which can be defined as: $C_{oxc} = \frac{\varepsilon_o \varepsilon_{ox}}{r_o \ln(1+EOT/r_o)}$, where ε_o and ε_{ox} are the dielectric permittivity of air and SiO_2, respectively, r_o is the radius of the convex groove [27] and EOT is the effective oxide thickness, i.e., $EOT = t_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} t_{ox2}$, where, ε_{ox1} and ε_{ox2} are the Dielectric permittivity of lower and upper gate and $t_{ox1}$and t_{ox2} are the thickness of the lower and upper dielectric, respectively.

Also, L_{eff} is the effective channel length and; V_{dsx} is the effective drain-source voltage and V_{gsx} gives the smooth transition from strong to weak inversion, which is given as:

$$V_{dsx} = V_{dsat}\cdot\left[1-\frac{\ln\left[1+\exp\left[A.\left(1-\frac{V_{ds}}{V_{dsat}}\right)\right]\right]}{\ln\left(1+\exp(A)\right)}\right] \quad \text{and}$$

$$V_{gsx} = 2.\eta.V_t.\ln\left[1+\exp\left[\frac{V_{gs}-V_{th}}{2.\eta.V_t}\right]\right]+V_{th}$$

where, V_{dsat} is drain saturation voltage, η is the capacitive coupling factor between gate and silicon surface, $V_t = \frac{k.T}{q}$, where, k and T are the Boltzmann constant and temperature in Kelvin, respectively and A is constant, whose value is taken as 8.

The effective channel length is decreased by l_d, due to CLM effect, i.e. $l_d = l.\ln\left(1+\frac{V_{dsx}-V_{dsat}}{V_{pp}}\right)$ where, $l=\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}.t_{ox}.X_j}$, where, ε_{si} is the dielectric permittivity of Silicon and X_j is the Source/Drain junction depth and V_{pp} [26] is treated as fitting parameter and its value can be calculated as: $V_{pp}=\frac{l.\varepsilon_c}{\delta^{/}}$, where $\varepsilon_c=2.\frac{\nu_{sat}}{\mu_s}$.

The, threshold voltage, V_{th}, for GME-TRC MOSFET [27] is defined as:

$$V_{th}=2\phi_F+\frac{1}{M}\frac{(r_o+EOT)y_d}{(y_d-r_o-EOT)}\frac{qN_A}{\varepsilon_{si}}-2\exp\left(\frac{-\theta_{01}}{2\lambda}\right)\sqrt{\delta_{11}\delta_{12}} \quad (2)$$

The depletion layer thickness y_d, is approximately given by $y_d=\sqrt{\frac{2\varepsilon_{Si}}{qN_A}1.5\phi_F}$ where, ϕ_F is the Fermi potential and q is the electronic charge.

Further, assuming the concave corner to be part of a cylinder, having corner radius of the convex groove is r_o, and the corner angle under region M1 is θ_{o1}.

Also, λ, M, δ_{11} and δ_{12} are the variables whose values have been calculated in [27].

Moreover, Non-linearity in a device is manifested by the presence of high-order 'harmonics' at the output signal. To model the non-linearity, a MOSFET modulated with an AC gate voltage, V_{gs}, producing a drain current, I_{ds}, can be viewed as a time variant non-linear system

$$I_{ds}=I_o+g_{m1}.V_{gs}+g_{m2}.V_{gs}^2+g_{m3}.V_{gs}^3+.............. \quad (3)$$

where, I_o is the current at DC operation point and Taylor expansion coefficients are $g_{mn}=\frac{1}{n!}\frac{\partial^n I_{ds}}{\partial V^n_{gs}}\Big|_{V_{ds}=const}$ which can be represented as:

A. First Order Transconductance

$$g_{m1}=\frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=const}=\left\{\begin{array}{l} -\frac{A^{/}B}{C}.\left(-\frac{dl_d}{dV_{gs}}.\nu_{sat}+\delta_o.\mu_s.\frac{dV_{dsx}}{dV_{gs}}\right)+ \\ A^{/}\left(\frac{dV_{gsx}}{dV_{gs}}-\frac{0.5\alpha dV_{dsx}}{dV_{gs}}\right).V_{dsx} \\ +A^{/}.(V_{gs}-V_{th}-0.5.\alpha.V_{dsx}).\frac{dV_{dsx}}{dV_{gs}} \end{array}\right\}$$

where, $A^{/}=\frac{\mu_s.C_{oxc}.W.\nu_{sat}}{\left((L_{eff}-l_d).\nu_{sat}+\delta_o.\mu_s.V_{dsx}\right)}$,

$B=(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).V_{dsx}$

$C=\left((L_{eff}-l_d).\nu_{sat}+\delta_o.\mu_s.V_{dsx}\right)$ and $E=1+\exp\left[\frac{V_{gs}-V_{th}}{2.\eta.V_t}\right]$

B. Second Order Transconductance

$$g_{m2}=\frac{\partial^2 I_{ds}}{\partial V_{gs}^2}\Big|_{V_{ds}=const}=\left[\begin{array}{l} \frac{2A^{/}B}{C^2}.\left(-\frac{dl_d}{dV_{gs}}.\nu_{sat}+\delta_o.\mu_s.\frac{dV_{dsx}}{dV_{gs}}\right)^2- \\ \frac{2A^{/}B}{C}.\left(\frac{dV_{gsx}}{dV_{gs}}-\frac{0.5\alpha dV_{dsx}}{dV_{gs}}\right). \\ V_{dsx}.\left(-\frac{dl_d}{dV_{gs}}.\nu_{sat}+\delta_o.\mu_s.\frac{dV_{dsx}}{dV_{gs}}\right)- \\ \frac{2A^{/}}{C^2}.\left(-\frac{dl_d}{dV_{gs}}.\nu_{sat}+\delta_o.\mu_s.\frac{dV_{dsx}}{dV_{gs}}\right). \\ (V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).\frac{dV_{dsx}}{dV_{gs}}- \\ \frac{A^{/}B}{C}.\left(-\frac{d^2l_d}{dV_{gs}^2}.\nu_{sat}+\delta_o.\mu_s.\frac{d^2V_{dsx}}{dV_{gs}^2}\right)+ \\ \frac{A^{/}}{C}.\left(\frac{d^2V_{gsx}}{dV_{gs}^2}-0.5\alpha.\frac{d^2V_{dsx}}{dV_{gs}^2}\right).V_{dsx}+ \\ \frac{2A^{/}}{C}.\left(\frac{dV_{gsx}}{dV_{gs}}-\frac{0.5\alpha dV_{dsx}}{dV_{gs}}\right).\frac{dV_{dsx}}{dV_{gs}}+ \\ \frac{A^{/}}{C}.(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).\frac{d^2V_{dsx}}{dV_{gs}^2} \end{array}\right] \quad (4)$$

where, $V_{dsat}=\frac{V_{gsx}-V_{th}}{\alpha}$, $\frac{dV_{dsat}}{dV_{gs}}=\frac{E-1}{\alpha.E}$ and

$$\frac{dl_d}{dV_{gs}}=\frac{l}{V_{pp}}.\frac{\left(\frac{dV_{dsx}}{dV_{gs}}-\frac{dV_{dsat}}{dV_{gs}}\right)}{\left(1+\frac{V_{dsx}-V_{dsat}}{V_{pp}}\right)} \quad (5)$$

$$\frac{dV_{dsx}}{dV_{gs}}=\frac{dV_{dsat}}{dV_{gs}}.\left[\begin{array}{l} 1-\frac{\ln\left[1+\exp\left[A.\left(1-\frac{V_{ds}}{V_{dsat}}\right)\right]\right]}{\ln(1+\exp(A))}- \\ \frac{A.V_{ds}}{V_{dsat}}.\frac{\exp\left[A.\left(1-\frac{V_{ds}}{V_{dsat}}\right)\right]}{1+\exp\left[A.\left(1-\frac{V_{ds}}{V_{dsat}}\right)\right].\ln(1+\exp(A))} \end{array}\right] \quad (6)$$

Also, $\frac{d^2l_d}{dV_{gs}^2}$ and $\frac{d^2V_{dsx}}{dV_{gs}^2}$ can be obtained by differentiating Eqs. (5-6) w.r.t. V_{gs}.

Similarly, by differentiating again Eq. (4) w.r.t. V_{gs} we obtained g_{m3}, i.e.

$$g_{m3}=\frac{\partial^3 I_{ds}}{\partial V_{gs}^{\ 3}}\Big|_{V_{ds}=const}=NQ.\begin{bmatrix}\frac{4A^{/}B}{QC^2}.\frac{dN}{dV_{gs}}-\frac{2A^{/}V_{dsx}}{QC}.\frac{dQ}{dV_{gs}}+\frac{4A^{/}B}{C^2}. \\ \frac{dN}{dV_{gs}}-\frac{2QA^{/}}{C}.\frac{dV_{dsx}}{dV_{gs}}-\frac{2QA^{/}}{C}.\frac{d^2V_{dsx}}{dV_{gs}^{\ 2}}-\frac{2QA^{/}}{C} \\ .\frac{dV_{dsx}}{dV_{gs}}-\frac{2QA^{/}}{C}.\frac{d^2V_{dsx}}{dV_{gs}^{\ 2}}\frac{2A^{/}B}{C^2}.\frac{dN}{dV_{gs}}-\frac{A^{/}V_{dsx}}{QC} \\ .\frac{dQ}{dV_{gs}}+\frac{2A^{/}}{C}.\frac{dV_{dsx}}{dV_{gs}}-(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}). \\ \frac{A^{/}}{C}.\frac{d^2V_{dsx}}{dV_{gs}^{\ 2}}-\frac{2A^{/}}{C}.\frac{dV_{dsx}}{dV_{gs}}\end{bmatrix}$$

$$+N^2\begin{bmatrix}-\frac{6A^{/}BK}{C^3}+\frac{2A^{/}QV_{dsx}}{C^2}+\frac{2A^{/}B}{C^2}.\frac{dV_{dsx}}{dV_{gs}}+ \\ \frac{4A^{/}QV_{dsx}}{C^2}+\frac{4A^{/}}{C^2}.(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).\frac{dV_{dsx}}{dV_{gs}}\end{bmatrix}+\frac{2A^{/}QV_{dsx}}{C}. \qquad (7)$$

$$\frac{dN}{dV_{gs}}+\frac{2A^{/}}{C}.\frac{dN}{dV_{gs}}.\frac{dV_{dsx}}{dV_{gs}}.(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx})-\frac{A^{/}QV_{dsx}}{C}.\frac{dN}{dV_{gs}}-\frac{A^{/}}{C}$$

$$.\frac{dN}{dV_{gs}}(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).\frac{dV_{dsx}}{dV_{gs}}-\frac{A^{/}B}{C}.\frac{d^2N}{dV_{gs}^{\ 2}}+A^{/}\frac{dV_{dsx}}{dV_{gs}}.\frac{dQ}{dV_{gs}}$$

$$+A^{/}V_{dsx}.\frac{d^2Q}{dV_{gs}^{\ 2}}+2A^{/}\frac{dV_{dsx}}{dV_{gs}}.\frac{dQ}{dV_{gs}}+2A^{/}Q\frac{d^2V_{dsx}}{dV_{gs}^{\ 2}}+A^{/}Q\frac{d^2V_{dsx}}{dV_{gs}^{\ 2}}+A^{/}.$$

$$(V_{gsx}-V_{th}-0.5.\alpha.V_{dsx}).\frac{d^3V_{dsx}}{dV_{gs}^{\ 3}}$$

where, $N=\left(-\frac{dl_d}{dV_{gs}}.\nu_{sat}+\delta_o.\mu_s.\frac{dV_{dsx}}{dV_{gs}}\right)$, $Q=\left(\frac{dV_{gsx}}{dV_{gs}}-0.5\alpha.\frac{dV_{dsx}}{dV_{gs}}\right)$

Further, the linearity FOMs can be obtained by using above equations as:

$V_{IP2}=4.\left(\frac{g_{m1}}{g_{m2}}\right)$ and $V_{IP3}=\sqrt{24.\frac{g_{m1}}{g_{m3}}}$ [28] $IIP3=\frac{2}{3}.\left(\frac{g_{m1}}{g_{m3}.Rs}\right)$

and [29] 1-dB compression point $=0.22\sqrt{\frac{g_{m1}}{g_{m3}}}$

where, Rs=50 Ω for most RF applications.

For improved linearity performance and low distortion operations, these FOMs should be as high as possible. Where, V_{IP2} represents the extrapolated input voltage at which first and second-order harmonic voltages are equal; V_{IP3} represents the extrapolated input voltage at which first and third-order harmonic voltages are equal; and IIP3 represents the extrapolated input power at which first and third-order harmonic powers are equal.

V. Results and Discussion

1. Electron Temperature Assessment for Different Recessed Channel Structure

Fig. 2 shows the impact of electron temperature for various recessed structures along the channel position. In scaled devices, electric field peak near the drain end causes carrier heating that results in the hot electron effect thereby degrading the hot carrier reliability of the

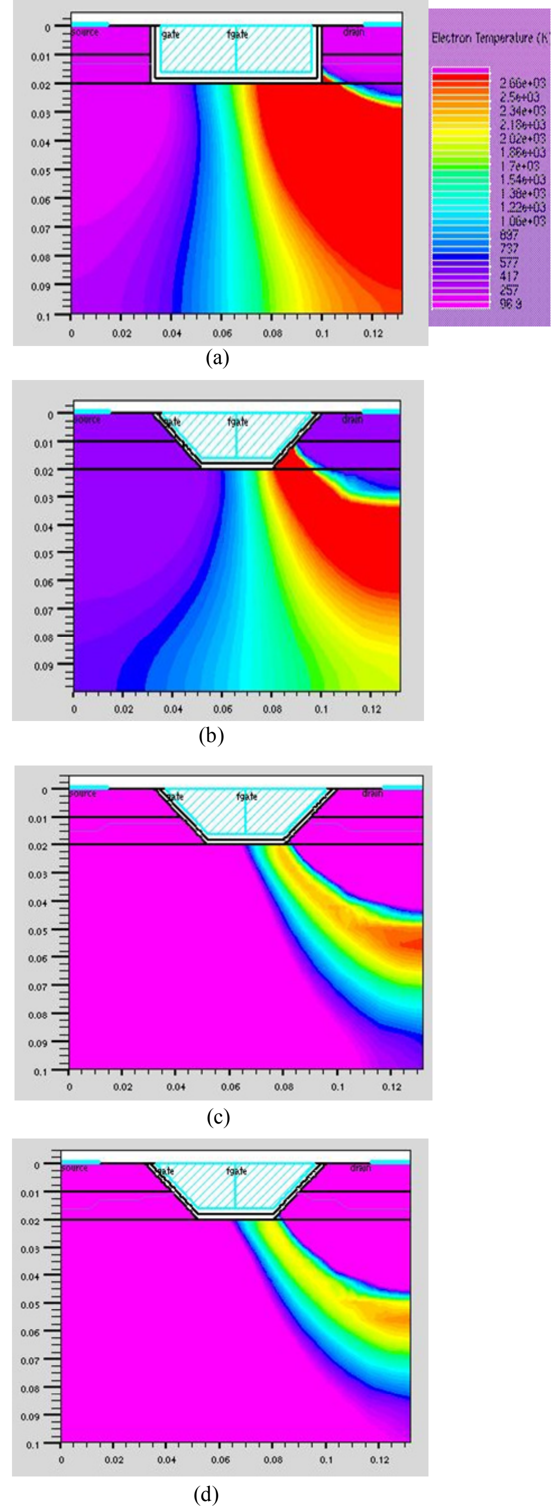


Fig. 2. (a), (b), (c) and (d), respectively, show the variation of electron temperature along the channel position for RRC, TRC, GME-TRC and MLGME-TRC MOSFETs.

device. From Fig. 2(a) and (b), it can be seen that the TRC MOSFET results in improved hot carrier reliability as compared to RRC MOSFET by possessing lower electron temperature at the drain end. This is because in RRC MOSFET the corners are comparatively sharper as compared to TRC MOSFET which results in high peak electric field at the corners, leading to high carrier heating near the drain end, resulting in degradation of hot carrier immunity in RRC MOSFET. In GME-TRC MOSFET high electric field originates in between the channel and reduces at the drain end, because of the work function difference between the two metal gates. This result in screening of channel regime from potential variations at the drain, leading to reduced carrier heating, thereby enhances the hot carrier reliability in terms of reduced electron temperature at the drain, as shown in Fig. 2(c). The incorporation of multi-layered high-κ dielectric system facilitates physically thicker gates, thereby permitting the scaling of gate oxide thickness and thus, increasing gate control over the channel. Also, it is seen from Fig. 2(d) that, MLGME-TRC MOSFET exhibits lowest electron temperature near the drain as compared to its conventional counterparts, owing to the use of high-κ upper dielectric, resulting in improved screening across the channel from drain potential variation, tending to reduced electric field at the drain end which in turn reduces the gate leakage current and hence, also provides the hot carrier immunity in the device.

2. Linearity Performance Evaluation

A. Higher Order Transconductance Parameterization

Fig. 3(a) shows the drain current characteristics for grooved gate MOSFET [30], having L_g=140 nm. It is reflected from the figure that there is a good agreement between experimental, simulation and proposed model. Figs. 3(b-d) shows the higher order transconductance parameters, i.e. g_{m1}, g_{m2}, and g_{m3} with respect to gate overdrive voltage (V_{gs}-V_t), for MLGME-TRC, GME-TRC, TRC and RRC MOSFETs having threshold voltage, i.e. V_t, equals to 0.191 V, 0.217 V, 0.30 V and 0.49 V, respectively.

Fig. 3(b) indicates that, MLGME-TRC MOSFET shows the higher performance as compared to RRC and GME-TRC MOSFET. This is due to the gate material

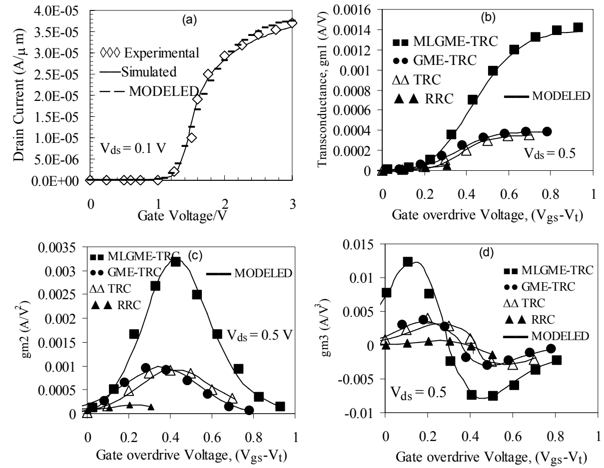


Fig. 3. (a) Experimental, Simulation and modeled result comparison of I_{ds}-V_{gs} characteristics of grooved gate MOSFET, having L_g=140 nm.(b), (c) and (d) shows the variation of g_{m1}, g_{m2} and g_{m3} respectively.

engineering architecture and multi-layered high-κ dielectric system, which provides the significantly enhanced screening effect and facilitates the physically thicker gates, thereby permitting the scaling of gate oxide thickness, resulting in increasing the gate control over the channel and hence, the transconductance parameters. The zero-crossover point of g_{m3} determines the DC bias point for optimum device operation.

Thus, the non-linear behaviour of g_{m3} can be minimized by setting DC bias close to g_{m3} zero-crossover point. Since g_{m3} has approximately a balanced magnitude around the zero-crossover point as is clear from Fig. 3(d), the harmonic distortion it generates can be cancelled for a small signal [19]. Fig. 3(d) clearly indicates that, as we move from RRC structure to more prominent device structures, i.e. TRC, GME-TRC and then to MLGME-TRC, it results in shifting of bias point towards the lower V_{gs}, as a consequence of improvement in gate control, and hence causing reduction in harmonic distortion and non-linear behaviour. Moreover, to gain the effectiveness of the proposed design, impact of various technology parameter variations has been considered for higher transconductance parameters with respect to gate overdrive voltage, having threshold voltage 0.217 for Φ_{M1}=4.7 V, Φ_{M2}=4.1 V, 0.288 for Φ_{M1}=4.7 V, Φ_{M2}=4.4 V, 0.06 V for., $N_A=1\times10^{17}$ cm^{-3}, 0.19 V for, ε_{ox1}=3.9 and ε_{ox2}=20 and 0.18 V for X_j=13 nm, as shown in Figs. 4(a-f). It is seen from Figs. 4(a), (c) and (e) that, the increase in

work function difference of two gate metals, i.e. Φ_{M1} and

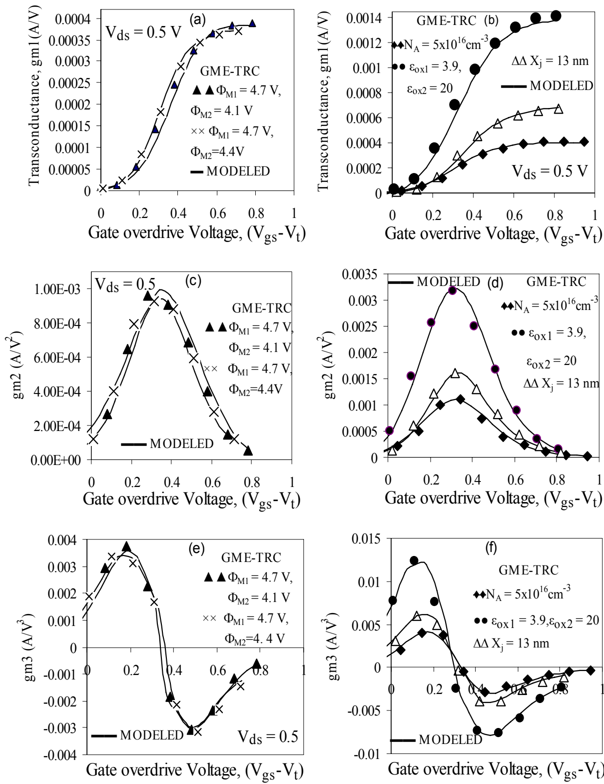


Fig .4. (a), (c) and (e) Variation of g_{m1}, g_{m2} and g_{m3}, respectively, with gate overdrive voltage (V_{gs}-V_t) for workfunction difference variation of GME-TRC MOSFET. (b), (d) and (f) Variation of g_{m1}, g_{m2} and g_{m3}, respectively, with gate overdrive voltage (V_{gs}-V_t) of GME-TRC MOSFET for different structural parameters.

Φ_{M2}, results in enhancement of potential step at the metal gate interface, leading to the improvement in screening effect due to metal gate M2.

Thus, increasing workfunction difference can further suppress the harmonic distortion and non linear behaviour in terms of shifting of DC bias point of g_{m3} towards the lower V_{gs}, as shown in Fig. 4(e).

Results also indicate that, higher order transconductance parameters can be improved further by using lightly doped substrate, due to carrier mobility enhancement, which in turn implies better carrier transport efficiency and reduced non linear behaviour in terms of shifting of DC bias point of g_{m3} towards the lower V_{gs}, as shown in Fig. 4(f). It is seen from the figure that, the increase of dielectric constant ε_{ox2}, also improves the linearity behaviour due to reduced gate oxide leakages and hot carrier effects (HCEs), leading to suppress harmonic distortion and non-linear behaviour exhibited by g_{m3}. Moreover, as X_j increases, i.e. NJD decreases, the bias point moves towards the lower V_{gs}, this is mainly attributed because of the decrease in height of the barriers formed at the corners with the decrease in NJD, resulting in increased carrier mobility due to improved gate control over the channel thereby, enhancing the linear characteristics, as illustrated by Fig. 4(b), (d) and (f). Close proximity of modeled and simulated results proves the validity of the proposed model.

B. V_{IP2} and V_{IP3} Linearity FOMs

V_{IP2} and V_{IP3}, represents the extrapolated gate-voltage amplitudes at which the second and third order harmonics, respectively, becomes equal to the fundamental tone in the device drain current (I_{ds}). These are the suitable FOMs, which can properly determine the distortion characteristics from DC parameters; to achieve high linearity and low distortion operations, these should be as high as possible. It is seen from Fig. 5(a) and (b) that V_{IP2} and peak point or singularity in V_{IP3} increases significantly in MLGME-TRC MOSFET and occurs at the lower gate bias, implies that lower gate voltage is needed to preserve the linearity, as compared to conventional GME-TRC, TRC and RRC MOSFETs. This is due to the reduced harmonic distrotion, owing to the improvement in gate leakages, carrier transport efficiency and hence the device gain. The peak of V_{IP3} mainly signifies the second order interaction effect and depicts the cancellation of the third-order non-linearity by device internal feedback around a second order non-linearity. This peak is highest in MLGME-TRC MOSFET, as shown in Fig. 5(b), thus, it is more linear than its conventional counterparts. Moreover, in order to improve the RF performance of the device, the structural design parameter needs to be tailored; hence influence of various technology variations have also been studied.

Figs. 5(c-f), respectively, shows the V_{IP2} and V_{IP3} profile for different structural parameter variations. It is seen that, as the metal gate work function difference for GME-TRC MOSFET is increased, substrate doping is decreased and X_j is increased, i.e. NJD is decreased, V_{IP2} and the peak in V_{IP3} significantly increases and singularity in V_{IP3} shifts more towards the lower gate bias, owing to improved gate control and drive current due to the increased screening of metal gate M1, improved mobility and enhanced carrier effeciency

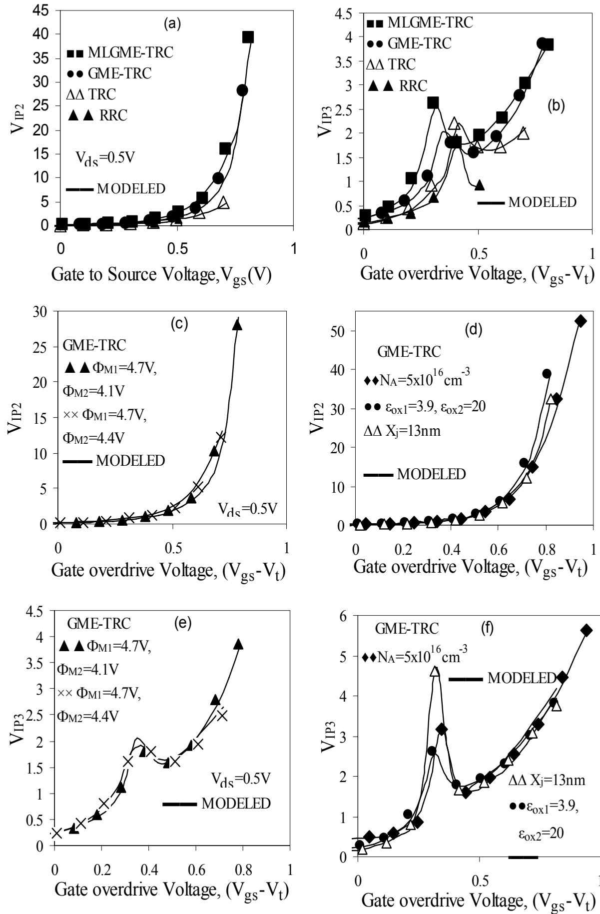
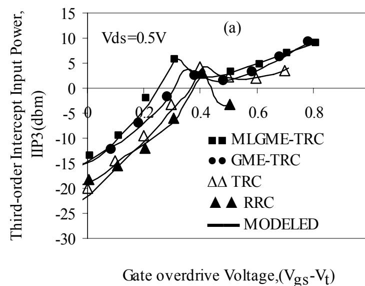


Fig.5. (a), (b) Variation of V_{IP2} and V_{IP3}, respectively, with overdrive voltage (V_{gs}-V_t) for MLGME-TRC, GME-TRC, TRC and RRC MOSFETs. (c), (e) Variation of V_{IP2} and V_{IP3}, respectively, with gate overdrive voltage (V_{gs}-V_t) for workfunction difference variation of GME-TRC MOSFET. (d), (f) Variation of V_{IP2} and V_{IP3}, respectively, with gate overdrive voltage (V_{gs}-V_t) of GME-TRC MOSFET for different structural parameters

across the channel, respectively. It is also indicated from the Fig. 5(d) and (f) that, linearity-distortion performance is improved with the increase in dielectric constant, i.e. ε_{ox2}, of MLGME-TRC MOSFET due to enhanced gate control over inversion charge density leading to improvement in g_{m1} and hence, V_{IP2} and V_{IP3}.



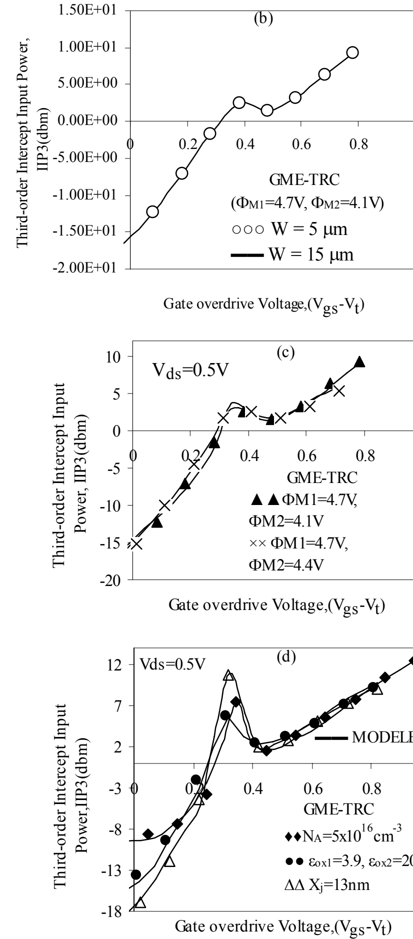


Fig.6. (a) Variation of IIP3 with overdrive voltage (V_{gs}-V_t) for MLGME-TRC, GME-TRC, TRC and RRC MOSFETs, (b) Variation of IIP3 with overdrive voltage (V_{gs}-V_t) for workfunction difference variation of GME-TRC MOSFET, (c) Variation of IIP3 with overdrive voltage (V_{gs}-V_t) of GME-TRC MOSFET for device width W=1 μm and 15 μm, (d) Variation of IIP3 with overdrive voltage (V_{gs}-V_t) of GME-TRC MOSFET for different structural parameters.

C. IIP3 and 1-dB compression point

IIP3 and 1-dB compression point are yet another important FOMs that evaluates the linearity performance. Further, the third-order nonlinearity term, g_{m3}, is mainly caused the trouble in RF applications, since it leads to inter-modulation, i.e. distortion of the fundamental amplitude via signals in the adjacent bands. In signal power, IIP3, where this spurious term is equal to the fundamental one is called the third-order inter-modulation intercept point. Fig. 6(a) represents the variation of IIP3 with gate overdrive voltage for various recessed channel structures. There is a considerable enhacement in IIP3 for MLGME-TRC MOSFET in comparison to conventional GME-TRC, TRC and RRC

MOSFETs. This is attributed to the step potential profile and improved gate controlability exhibited by GME and multilayered architecture. Thus, this significantly increases the carrier transport efficiency and gate control over the channel, thereby enhancing the gain (i.e. transconductance, g_{m1}). Further, in order to preserve linearity, the device should be biased in pre-kink position. Fig. 6(a) clearly shows the shifting of kink position towards higher gate bias for conventional MOSFETs in comparison to MLGME-TRC MOSFET which implicates that conventional MOSFETs need larger currents to preserve linearity. Moreover, it is seen from Fig. 6(b) and (c) that the variation of IIP3 for device width W = 5 μm and W = 15 μm is same as that for W=1 μm. This is due to the fact that, the transconductance mainly depends on the carrier following across the channel and the width of the device hardly affects its performance. Due to this reason authors have taken the constant device width (W), i.e. 1 μm, through out its consideration.

Further, the input power value, in dB, at which the gain of the low noise amplifier (LNA) drops by 1 dB, is referred to as the 1 dB gain compression point or the P1dB. This parameter is important for an amplifier circuit as it gives an idea about the maximum input power that the circuit can handle by providing a fixed amount of gain. Once the input power exceeds the P1dB of the amplifier, the gain starts decreasing. Thus, it is desirable that a LNA should have as high a P1dB value as feasible without significant tradeoff in the other parameters.

Fig. 7(a) clearly demonstrates that MLGME-TRC MOSFET exhibits a higher 1-dB compression point in contrast to conventional MOSFETs due to reduced signal distortion, and transconductance. Further, the effect of variation of device width (W) on P1dB is negligible and gives the same value, i.e. -26 for W=1 μm, 5 μm and 15 μm. This is because P1 dB is depends on transconductance and its derivative which is related to the carrier transport efficiency across the channel and the device width hardly has any impact on the channel formed.

Moreover, tuning of the GME-TRC MOSFET design in terms of increased workfunction difference, increased X_j, i.e. decreased NJD, dielectric constant, ε_{ox2}, and reduced substrate doping further improves IIP3 and 1-dB compression point and hence, enhances the linearity performance of the proposed design, as shown in Figs. 6(c, d) and Fig. 7(b).

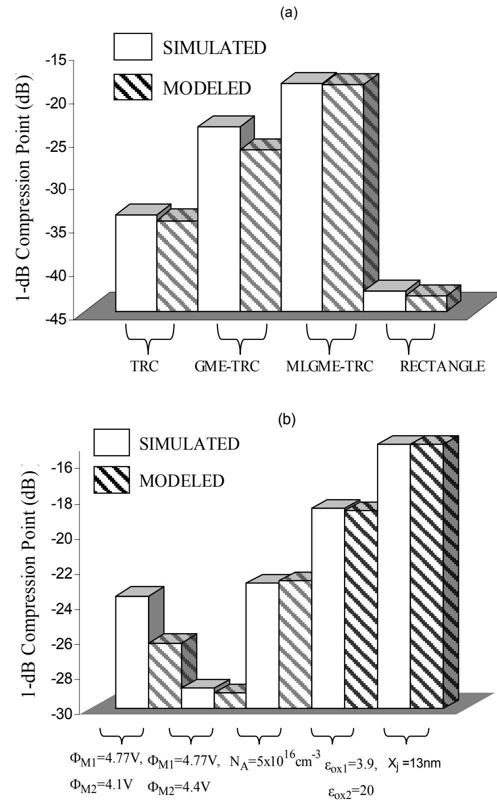


Fig.7. (a) 1-dB compression point (dB) at gate bias, V_{gs}=0.5 V for MLGME-TRC, GME-TRC, TRC and RRC MOSFETs, (b) 1-dB compression point (dB) at gate bias, V_{gs}=0.5 V for different structural parameter variations of GME-TRC MOSFET.

Hence, MLGME-TRC MOSFET exhibits superior linearity performance and high device efficiency as compared to conventional MOSFETs in terms of transconductance coefficients g_{m1}, g_{m2} and g_{m3}; and linearity metrics evaluation parameters: V_{IP2}, V_{IP3} and IIP3. Results, thus, imply that the RF harmonic distortion and linearity improves tremendously in scaled MOS devices. Although the amplifier's IIP3 and IMD3 are more complex in a single MOSFET, the optimization of the MOSFETs characteristics is a requisite to achieve the best LNA performance.

VI. CONCLUSIONS

The present work concentrates on the extensive study for various recessed channel structures, i.e. RRC, TRC, GME-TRC and MLGME-TRC MOSFETs, for different dielectric configurations to optimize the linearity performance by developing a model and validating it with experimental and simulated results. The key

factors affecting the device performance and the physics behind it are also scrutinized. Results reveal that MLGME-TRC design is superior to its conventional counterpart in all aspects, proving its consistently enhanced linearity performance in terms of improved higher order transconductance coefficients: g_{m1}, g_{m2}, g_{m3} and intermodulation distortion performance in terms of FOMs: V_{IP2}, V_{IP3}, IIP3 and 1-dB compression point. Hence, MLGME-TRC MOSFET design presents its effectiveness in the high-scale integration, design and modeling of power amplifiers and RFIC design.

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