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Continuous and Accurate PCRAM Current-voltage Model

Chul-Moon Jung, Eun-Sub Lee, and Kyeong-Sik Min

***Abstract*—In this paper, we propose a new Verilog-A current-voltage model for multi-level-cell PCRAMs. This model can describe the PCRAM operation not only in full SET and RESET states but also in the partial resistance states. And, 3 PCRAM operating regions of SET-RESET, Negative Differential Resistance, and strong-ON are unified into one equation in this model thereby any discontinuity that may introduce a convergence problem cannot be found in the new PCRAM model. The percentage error between the measured data and this model is as small as 7.4% on average compared to 60.1% of the previous piecewise model. The parameter extraction which is embedded in the Verilog-A code can be done automatically.**

***Index Terms*—Phase-change RAMs, Verilog-A model, unified model, multi-level-cell memories, PRAMs, PCRAMs**

I. INTRODUCTION

Phase-Change RAM (PCRAM) has been studied for many years due to better scalability than DRAM and FLASH memory thus being considered now as a strong candidate for future memories [1, 2]. Moreover, PCRAM can be used as Multi-Level-Cell (MLC) applications, where we can store more than two bits at one PCRAM cell because their resistance is able to be controlled as a function of the pulse width and amplitude of programming current [2]. To design read and write circuits of MLC PCRAM, an accurate and reliable current-voltage model is needed.

In this paper, we propose a new accurate current-voltage model which can fit well to the measured data not only in full SET and RESET states but also in partial SET and RESET, where the crystal fraction ratio, C_X is in between the full SET (C_X=1) and RESET (C_X=0). And, this model is reliable because one unified equation describes all the operation regions of PCRAM to prevent any numerical discontinuity point that may introduce the convergence problem in the circuit simulation. Comparing this new model to the previous ones, the models in [3-7] have discontinuity points in their current-voltage relationships which happen at the boundaries between different operating regions of PCRAM. This is caused from that the previous models have described the PCRAM operation using 3 different piecewise-linear models that are representing SET-RESET, Negative Differential Resistance (NDR), and ON region, respectively [7]. These piecewise-linear models could make some discontinuity points at their boundaries between different regions. Though a one-piece model without discontinuity was proposed in [8], it could not describe the partial resistance state well particularly when PCRAM changes from SET to RESET unlike our proposed model. And also, it was based on the SPICE macromodel and the step-like smooth blending function [8] which made the model complicated and its parameter extraction difficult. Comparing the SPICE macromodel with the Verilog-A, the Verilog-A model used in this paper is simpler, more portable, and flexible [7, 9], because the SPICE macromodel is based on circuit elements that have many limitations in describing the

Manuscript received Apr. 29, 2011; revised Jul. 8, 2011.
School of EE., Kookmin Univ., Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Korea
E-mail : mks@kookmin.ac.kr

complicated non-linear behavior of PCRAMs. For parameter extraction, the automatic and embedded parameter extraction step that cannot be provided in the SPICE macromodels of PCRAMs such as [8] makes the proposed Verilog-A model very useful in practical applications.

II. Unified and Continuous Current-voltage Model for Multi-Level-Cell PCRAM

In Fig. 1(a), at the SET-RESET region, PCRAM resistance is changed between the SET and RESET state according to the calculated crystal fraction ratio. The NDR region shows negative differential resistance between the SET-RESET and ON regions. The I_{TH} and V_{TH} mean a threshold current and voltage at which the NDR region starts, respectively. At the (I_X, V_X), a PCRAM enters into the ON region.

A new model equation that can describe PCRAM transient behavior of the partial state can be started from the previous model Eq. (1) in [10], where 3 regional equations of SET-RESET, NDR, and ON regions were merged mathematically using the parallel combination equation. However, the previous model Eq. (1) in [10] could not describe well the NDR region, especially for the partial state that is close to the full SET, as shown in Fig. 1(b). This is because the negative differential resistance is shown very little when the partial state is close to the full SET state. On the contrary, if the partial state is close to the full RESET, the negative differential resistance seems very obvious. Hence, to consider both the partial states that are close to the full SET and full RESET, we use the following merging function [11] in this paper.

$$f = f_1 \times \exp\left(w \cdot Ln(f_2 / f_1)\right) \tag{1}$$

Here, f_1 and f_2 are two regional equations and f is a merged equation. w is the weighting variable. If w=0, f becomes f_1 and as w becomes 1, f becomes more and more dominated by f_2. Assume that f_1 and f_2 represent the SET-RESET and ON regional equations, respectively. For the partial state that is close to the full SET, f_1 can move to f_2 very smoothly with showing very little negative differential resistance, using Eq. (1). For the partial state that is close to the full RESET, f_1 is abruptly changed to f_2, showing the large negative resistance. Hence, using Eq. (1), we can describe the partial state more accurately than the previous Eq. (1) in [10].

Using Eq. (1), the exact model equation of PCRAM current versus voltage relationship can be written by Eq. (2).

$$V_P = \frac{Ln(k_1 R_X I_P + 1)}{k_1} \times \exp\left[w \cdot Ln\left(\left(R_{ON} I_P + V_H\right) \Big/ \frac{Ln(k_1 R_X I_P + 1)}{k_1} \right) \right], \tag{2}$$

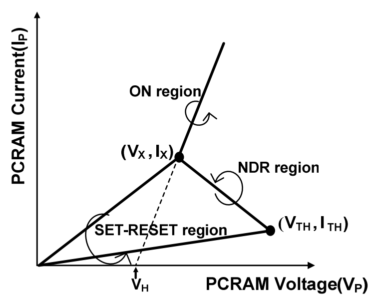
$$where\ w = 1 \Big/ \sqrt[n]{1 \Big/ \left(\frac{I_P - I_{TH}}{I_X - I_{TH}} \right)^n + 1} \quad (0 \le w \le 1)$$

Eq. (2) combines the SET-RESET regional equation and the ON regional equation into one unified equation using an exponential and a logarithmic function as indicated in Eq. (1). Here a transition phenomenon between the SET-RESET and ON region is modeled using a weighting variable that controls a relative portion of each region. Here V_P and I_P are a PCRAM voltage and current, respectively. R_X, R_{ON}, and V_H are SET-RESET resistance, ON resistance, and a holding voltage, respectively. k_1 is a coefficient of the SET-RESET region and w means a weighting variable which is calculated between 0 and 1. The value of n used in this simulation is 9. As n becomes larger, we can have a sharper transition from the NDR to the ON region. More specifically, the weighting variable, w is 0 for the SET-RESET, gets closer to 1 for the ON, and in between 0 and 1 for the NDR. If w is 0, Eq. (2) can be calculated with $V_P = Ln(k_1 R_X I_P + 1)/k_1$. This term can lead to $I_P \approx V_P / R_X$ when $k_1 \cdot V_P$ is very small and becomes exponential when $k_1 \cdot V_P$ is large. When w=1, Eq. (2) becomes $V_P = R_{ON} \cdot I_P + V_H$ which represents the current-voltage relationship at the ON region. Here n is 9 and I_{TH} varies according to the R_X. When R_X is full SET state I_{TH} is 0. When R_X is larger than full SET state I_{TH} becomes 40 μA.

R_X in Eq. (2) is calculated with the crystal fraction ratio, C_X. C_X varies in between a full crystal state (C_X=1) and a full amorphous state (C_X=0), as shown in Eq. (3), according to a calculated state variable, X [8]. The PCRAM resistance changes according to the cell temperature. The state variable, X means the thermal energy that is applied to the PCRAM and has the same dimension as temperature.

$$R_X = R_{SET} + (R_{RESET} - R_{SET}) \cdot (1 - C_X) \qquad (3)$$

where $C_X = 1 - e^{-X/A(X)}, A(X) = B \cdot e^{C/X}, and\ X = \int I_P^2 \cdot R_{ON} dt$



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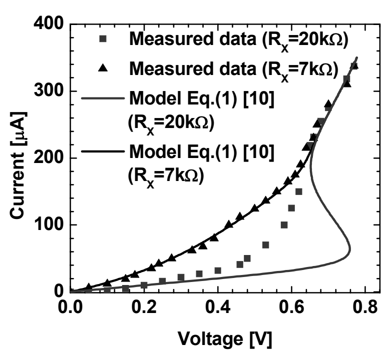

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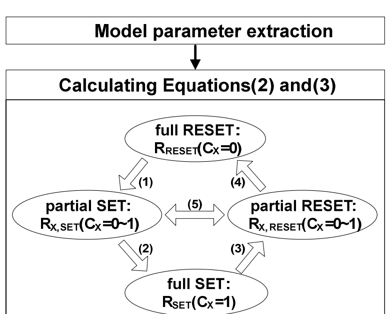


(c)

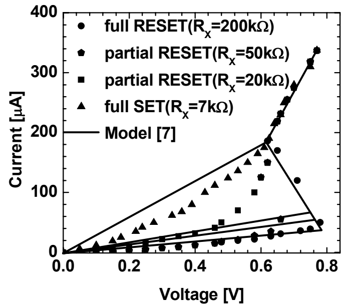
Fig. 1. (a) Current-voltage characteristic of PCRAM with 3 operation regions of SET-RESET, Negative Differential Resistance (NDR), and ON, (b) Comparison between the measured data [1] and the previous PCRAM model Eq. (1) in [10]. The partial state (R_X=20 kΩ) that is close to the full SET state (R_X=7 kΩ) shows a very large discrepancy between the measurement and the model Eq. (1) in [10], (c) Flow chart of the proposed PCRAM Verilog-A model where (1) means that the full RESET state changes to the partial SET and (2) means that the partial SET changes to the full SET. Similarly, the full SET changes to the partial RESET via (3) and the partial RESET changes to the full RESET via (4). (5) means the partial SET changes to the partial RESET and vice versus.

Here R_{SET}, R_{RESET}, and R_{ON} are PCRAM resistance in the full SET state, the full RESET state, and the ON region, respectively. A(X) has the parameters of B and C which are extracted using a simple linear fitting method.

Fig. 1(c) shows a flowchart of the new PCRAM Verilog-A model. First, it extracts the parameters used in Eqs. (2-3) automatically from the measured current-voltage data. And, k1 is calculated with the relationship between R_X and V_{TH}. Secondly, PCRAM voltage and current are calculated with Eqs. (2-3). The R_X in Eq. (2) is calculated with Eq. (3) using the state variable, X which represents thermal energy given to PCRAM cell. A state transition diagram for calculating the R_X is shown in Fig. 1(c). The full RESET and SET state have their resistance as large as the R_{RESET} and as small as the R_{SET}, respectively. According to the thermal energy given to PCRAM cell, the R_X can change in between the R_{SET} and R_{RESET}. If an amount of thermal energy is not enough to change its state fully from a crystal state (C_X=1) to an amorphous (C_X=0) or vice versa, the PCRAM goes into the partial RESET or SET state in Fig. 1(b). One thing to note is that this new model can support that PCRAM resistance can move directly from the partial SET to the partial RESET or in the reverse way not passing through the full RESET or full SET.

III. Comparison between the Conventional and the Newly Proposed Model

Fig. 2(a) shows comparison between the measured PCRAM data and the conventional piecewise model, where its 3 piecewise linear models describe the 3 operation regions, respectively. Fig. 2(b) shows the proposed unified model which has only one unified equation to prevent any discontinuity point at the boundaries between different regions. If you look at Fig. 2(b), its current-voltage relationship looks continuous through all the regions not showing any discontinuity at the boundaries. Also this Figure shows how the proposed model fits well to the measured data not only at the full SET-RESET states but also the partial states. To see the discontinuity more in detail, the dv/di is plotted with respect to the PCRAM current in Fig. 3(a), where we can see a discontinuity point happens in the conventional model that is not found in the proposed model. In Fig. 3(b),



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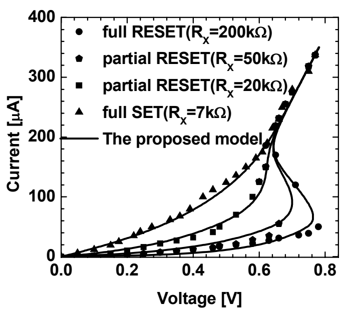
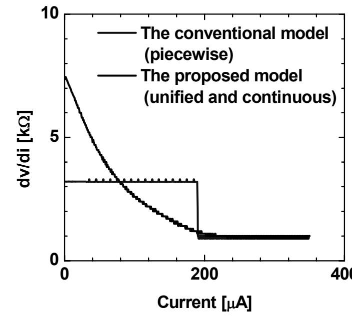


(b)

Fig. 2. (a) Comparison between the measured data [1] and the conventional piecewise model [7], (b) Comparison between the measured data [1] and the proposed model. Here I_{TH} is 40 μA and I_X and V_X are 180 μA and 0.62 V, respectively. k_1 in Eq. (2) is $10.4 \times 10^{-6}R_X + 2.93$ [1/V].

percentage errors between the measured data and the model are shown. Here the error of the conventional model reaches 60.1% on average, whereas that of the proposed is just as small as 7.4% in the entire PCRAM operation region, where the percentage error is calculated with $\frac{|I_{measured} - I_{simulated}|}{I_{measured}} \times 100$.

The crystal fraction ratio, C_X is plotted with respect to the pulse amplitude of programming current in Fig. 4(a). The C_X is calculated with Eq. (3) and it can change between 0 and 1 according to the state variable calculated with Eq. (3). The parameters in Eq. (3) are B=3.9621×10^{-12} [J] and C=-3.0574×10^{-14} [J], respectively. The R_{SET}, R_{RESET}, and R_{ON} are 7 kΩ, 200 kΩ, and 0.947 kΩ, respectively. Fig. 4(b) shows PCRAM resistance changes from the RESET to the SET and vice versa according to the crystal fraction ratio. Comparing the PCRAM resistance calculated with this unified model to the measured data, we can see this unified model fits very well to the measured data both in the SET and RESET states in the entire range of pulse amplitude from 0A to 1300 μA. Fig. 5(b) shows that PCRAM resistance



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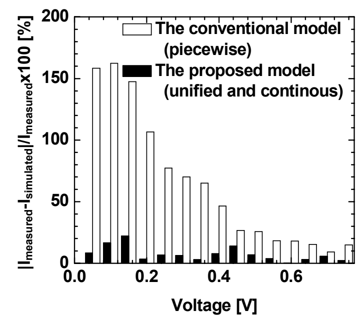
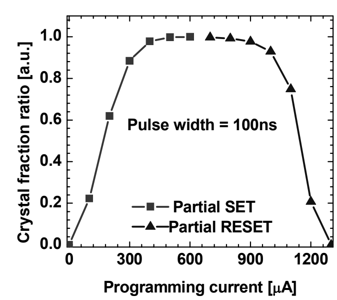


(b)

Fig. 3. (a) Comparison of the dv/di for full SET state between the conventional piecewise model [7] and the proposed unified model, (b) Comparison of percentage errors of the conventional [7] and proposed model for the full SET state i-v curve with the measured data [1].



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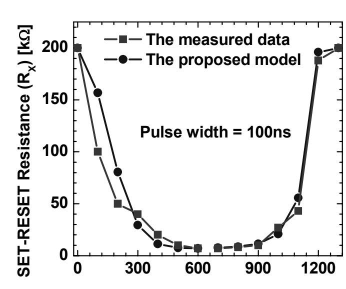

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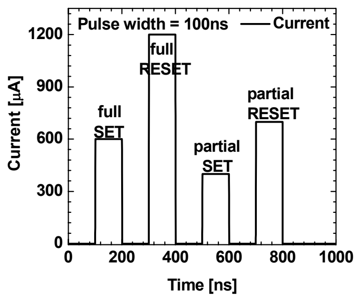
Fig. 4. (a) Crystal fraction ratio vs. programming current plot, (b) Comparison between the measured [1] and simulated resistance in the full SET, full RESET, partial SET, and partial RESET states.



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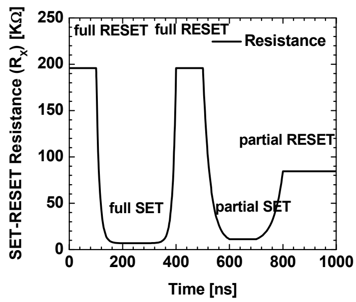
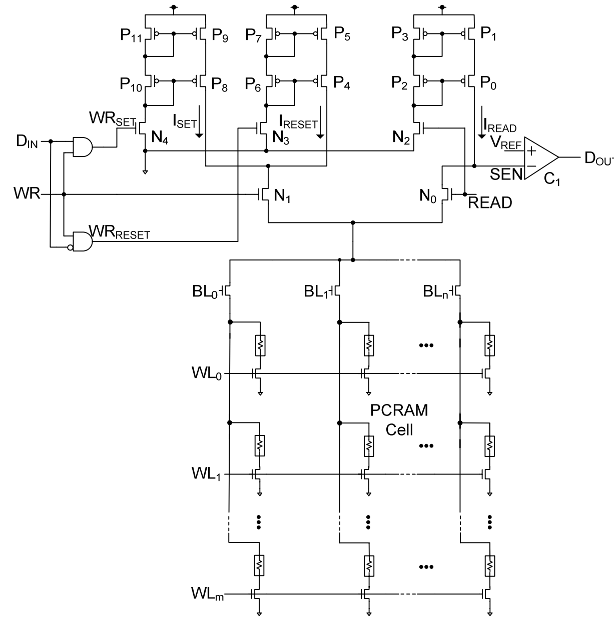


(b)

Fig. 5. (a) Waveforms of the applied programming current with the pulse width of 100ns, (b) Simulated PCRAM resistance changed according to the programming current in between the full RESET and SET state using real read and write circuits with 0.13-μm SPICE parameters from industry.

changes according to the programming current applied as shown in Fig. 5(a). By the first SET pulse, the PCRAM changes to the full SET state. In the second RESET pulse, it goes to the full RESET state. The third and fourth pulses are for the partial SET and partial RESET, respectively. In Fig. 5(a) and (b), the simulation was done using practical PCRAM read and write circuits from industry using real SPICE MOSFET parameters of a commercial 0.13-μm process technology.

Fig. 6(a) shows a schematic of PCRAM write and read circuits. In writing 'SET' to PCRAM, D_{IN} and WR become high to turn on N_1 and N_4. If N_1 and N_4 are on, I_{SET} as large as 550 μA can be applied to PCRAM to decrease PCRAM resistance to R_{SET} by the current mirror circuit. When we write 'RESET' to PCRAM, D_{IN} should be low and WR should be high to turn on N_1 and N_3. At this time, I_{RESET} as large as 1300 μA is applied to PCRAM using the other current mirror thus PCRAM resistance is raised up to R_{RESET}. When I_{RESET} is applied, PCRAM resistance increases dynamically. For reading PCRAM data, first, READ signal should be high and WR signal should be low to turn on N_0 and N_2 and turn off N_1, N_3, and N_4. At this time the small read current, I_{READ} as small as 20 μA is applied to PCRAM.



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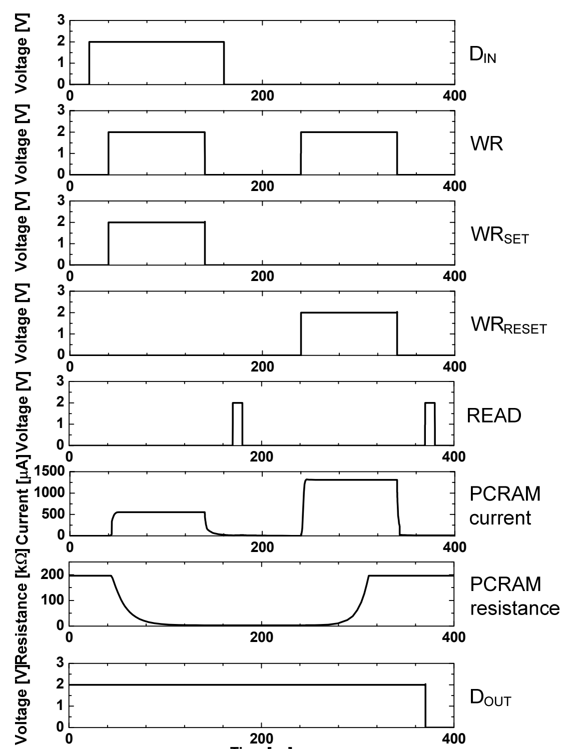

(b)

Fig. 6. (a) Schematic of PCRAM write and read circuit, (b) Voltage waveforms of D_{IN}, WR, WR_{SET}, WR_{RESET}, READ, PCRAM current, PCRAM resistance, and D_{OUT}.

When this small I_{READ} is applied, PCRAM resistance does not change because I_{READ} is too small to change the PCRAM resistance. According to PCRAM resistance, a voltage which is associated with the sensing node 'SEN' can be higher or lower than V_{REF}. The comparator, C_1 can decide whether the voltage is higher or lower. After comparing, the sensed data can be stored at the latch or flip-flop that is connected to the comparator output. Here the simulated array size is 32 × 32. Fig. 6(b) shows the waveforms of the D_{IN}, WR, WR_{SET}, WR_{RESET}, and READ, And, PCRAM current, PCRAM Resistance, and Dout are also shown in Fig. 6(b). For the circuit simulation, SAMSUNG 0.13-μm SPICE parameters were used for the MOSFET devices in Fig. 6(a) and the electrical behaviors of PCRAM was described by the proposed Verilog-A model. The mixed simulation of both CMOS and PCRAM was done by Spectre circuit simulator in Cadence.

IV. CONCLUSIONS

In this paper, we proposed the new Verilog-A current-voltage model for MLC PCRAM. This model fits well to the measured data not only in full SET and RESET states but also in the partial SET and RESET which are in between the full SET and full RESET. Moreover, the percentage error of this model that includes both linear and non-linear current-voltage relationships is lower than 7.4% on average in the entire operation region, compared to 60.1% of the conventional piecewise one. The SET-RESET, NDR, and ON regions of PCRAM are unified into one equation in this model thereby discontinuity being able to be prevented. The parameter extraction is straightforward and this extraction step is embedded in the Verilog-A code thus it can be done automatically.

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Chul-Moon Jung received the B.S degree in Electronic and Computer Engineering from Kookmin University, Seoul, the Republic of Korea, in 2010. He is currently working toward the Master's degree of Electronic and Computer Engineering at Kookmin University, Seoul, Korea. His research interest includes the circuit design and modeling for resistive RAM and phase change RAM.

Eun-Sub Lee received the B.S degree in Electronic and Computer Engineering from Kookmin University, Seoul, the Republic of Korea, in 2010. He is currently working toward the Master's degree of Electronic and Computer Engineering at Kookmin University, Seoul, Korea. His current research interest includes the power management IC design.

Kyeong-Sik Min received the B.S. degree in Electronic and Computer Engineering from Korea University, Seoul, Korea, in 1991, and the M.S.E.E. and Ph. D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993 and 1997, respectively. In 1997, he joined Hynix Semiconductor Inc., where he was engaged in the development of low-power and high-speed DRAM circuits. From 2001 to 2002, he was a research associate at University of Tokyo, Tokyo, Japan, where he designed low-leakage memories and logic circuits. In September 2002, he joined the faculty of Kookmin University, Seoul, Korea, where he is currently an Associate Professor in the School of Electrical Engineering. His research interests include low-power VLSI, memory design, and power IC design. Prof. Min is a technical program committee member of Asian Solid-State Circuits Conference (A-SSCC) and Korean Conference on Semiconductors (KCS). He is a member of IEEE, IEICE, and IEEK.