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Selective Growth of Carbon Nanotubes using Two-step Etch Scheme for Semiconductor Via Interconnects

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Abstract - In the present work, a new approach is proposed for via interconnects of semiconductor devices, where multi-wall carbon nanotubes (MWCNTs) are used instead of conventional metals. In order to implement a selective growth of carbon nanotubes (CNTs) for via interconnect, the buried catalyst method is selected which is the most compatible with semiconductor processes. The cobalt catalyst for CNT growth is pre-deposited before via hole patterning, and to achieve the via etch stop on the thin catalyst layer (ca. 3nm), a novel 2-step etch scheme is designed; the first step is a conventional oxide etch while the second step chemically etches the silicon nitride layer to lower the damage of the catalyst layer. The results show that the 2-step etch scheme is a feasible candidate for the realization of CNT interconnects in conventional semiconductor devices.

Keywords: Carbon nanotubes, Via interconnects, Selective growth, Two-step etch, Physical and chemical reactions

1. Introduction

Carbon nanotubes (CNTs) have been considered good electrical conductors with a one dimensional graphene tubular structure and nano size diameter [1-5]. With such properties it has been investigated as a candidate for vertical interconnects competing with copper in nano-scale feature sizes in semiconductor industry [6-10]. Although the integration of CNT interconnects has been tried by many other groups [8-11], most groups have used e-beam evaporation for the catalyst material or lift-off method for the catalyst pattern which are not compatible with current semiconductor processes. Compatibility with pre-existing technologies would be an important guideline for the introduction of CNT to the semiconductor industry. Among CNT interconnect methods have been reported, the most semiconductor process compatible method would be a buried catalyst method [11-13], in which a catalyst layer is deposited before via patterning. In this method, since the ultra thin catalyst film (~3nm) should be remained on the bottom electrode after via patterning, via etch should be done carefully. Especially, etch stopping on the ultra thin catalyst layer is quite difficult, because plasma damage easily remove the catalyst layer. Thickness of catalyst layer is directly related to the CNT density (number of conduction path), a ultra thin catalyst layer is strongly required to obtain low resistive CNT interconnects.

In the present work, we propose novel 2-step etch scheme including a conventional inter-layer dielectrics (ILD, silicon-dioxide layer in this work) etch step and a stopper layer etch step. First etch step is physical reaction dominant SiO_2 etch and stops on the stopper layer of silicon nitride (Si_3N_4) layer using etch selectivity between SiO_2 and Si_3N_4. Second step is chemical reaction dominant Si_3N_4 etch which has quite slow reactivity and stops on the ultra thin catalyst layer. Finally, we show selective growth of CNTs in the via hole with good uniformity.

2. Experiments

The key processes of vertical CNT via interconnection are the bottom electrode (BE) patterning, the CNT vertical interconnects, and the top electrode (TE) patterning. The most critical process would be the CNT vertical interconnects process among above key processes, since etch stopping on the ultra thin catalyst layer is quite sensitive to the etch process. Fig. 1 shows the schematic diagrams of process flow for the CNT vertical interconnects. The method is the so-called buried catalyst scheme [11-13], in which a Co catalyst layer is deposited before via patterning.

2.1 Bottom electrode patterning

For the BE, the titanium nitride (TiN) layer is deposited on the oxidized silicon wafer by reactive ion beam sputtering. A Ti contact layer (1 nm), a Co catalyst layer (3 nm) and a silicon nitride (Si_3N_4) etch stopper layer (20 nm) are deposited sequentially on the TiN layer. A Ti contact layer forms conducting TiC ohmic layer leading to ohmic contact between CNTs and TiN BE [14]. Photolithography and a plasma etch process were used for BE patterning. BE stack structure with thicknesses and BE patterning result are shown in Fig. 2.

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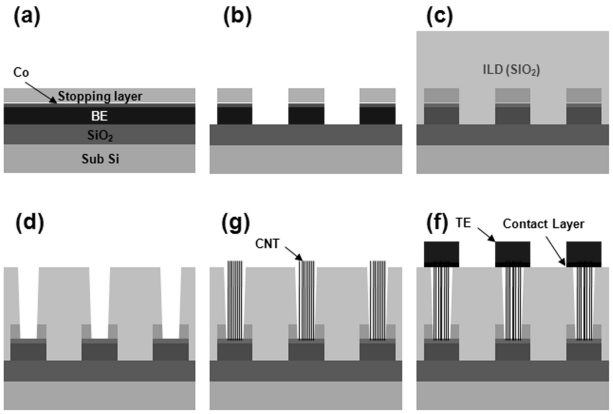

Fig. 1. Process flow and schematic diagram of a buried catalyst scheme for CNT interconnects; (a) BE, Co catalyst, and Stopping layer deposition, (b) BE patterning, (c) ILD deposition, (d) via hole patterning, (e) CNT growth, (f) TE formation (In this work, since we focuse on the etch stopping at ultra thin Co catalyst layer, TE patterning process is not described here.).

2.2 Via hole patterning

Vias are also patterned using conventional photolithography techniques and plasma etch process. At the via etch step, special care should be taken, because the etch process must be stopped at the ultra thin Co catalyst layer.

2.3 CNT growth

Multi-walled CNTs were grown in a plasma CVD system with CH_4 source gas and H_2 carrier gas at 600 °C with a flow rate of 1:4 at 10 Torr. Plasma is formed by microwaves (2.45GHz) with a spherical discharging area. A metal mesh is situated above the substrate and the discharging plasma area is limited by the mesh. In this case, carbon radicals mainly contribute to CNT growth and the damage by positive ions of the CNT structure is negligible. In our CNT growth system, the length and diameter of the CNTs were measured by scanning electron microscopy (SEM) and transmission electron microscopy (TEM, not shown in this paper) images to be about 10 μm and 10 nm, respectively. The CNT density is comparable to that of conventional CNT via hole, 4×10^{11} /cm^2. The results suggest that the location of CNT growth can be controlled by the two-step etch scheme designed in this work.

3. Results and Discussions

In order to define the BE line-and-spaces, plasma etch process was done by consecutive two steps; the first step was chlorine and fluorine based etch for Si_3N_4 stopper layer and Co catalyst layer etch, and the second step was chlorine based etch for TiN etch. Fig. 2(b) and (c) shows a

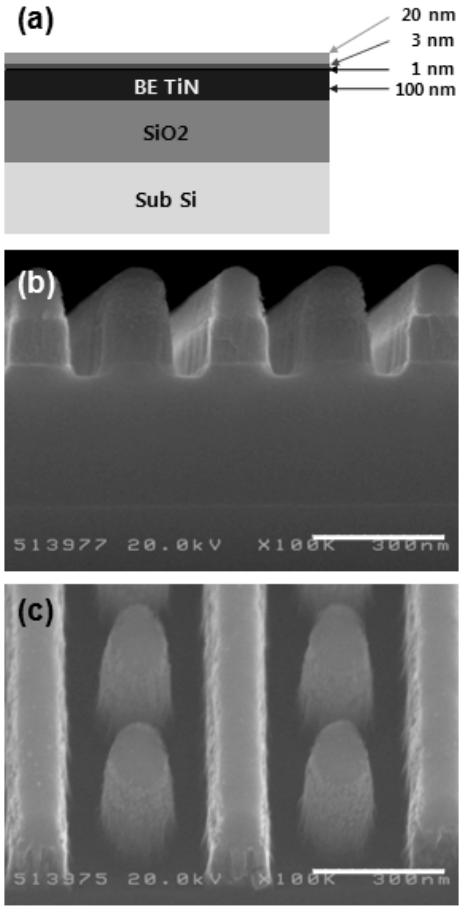

Fig. 2. BE patterning results. (a) BE stack structure with thicknesses (b) a cross-sectional view and (c) a bird view of scanning electron microscopy (SEM) image.

cross-sectional view of SEM image and a bird view of that, respectively. BE isolation was done clearly. In Fig. 2(c), island patterns and straight line patterns show string type BE patterns and dummy patterns for better isolation, respectively. Two via holes will be formed only on the island patterns and not on the line patterns. The BE layer and the Si_3N_4 stopper layer were remained after patterning process. The Co catalyst layer was protected under the Si_3N_4 stopper layer. After the BE patterning process, a inter-layer-dielectric (ILD, 1 μm) is deposited by a high-density plasma silicon dioxide (SiO_2) deposition process and is planarized to be 300 nm in height from the BE TiN layer using chemical mechanical polishing (CMP) process.

When a conventional etch condition is used for via hole patterning, etch stopping at the thin Co catalyst layer is very difficult, since most of the Co layer is etched away from the bottom of the via hole. SEM images of as-etched via hole and CNT growth result of a sample etched by the conventional etch conditions are shown in Fig. 3(a) and (b), respectively.

We could hardly recognize whether the Co catalyst layer

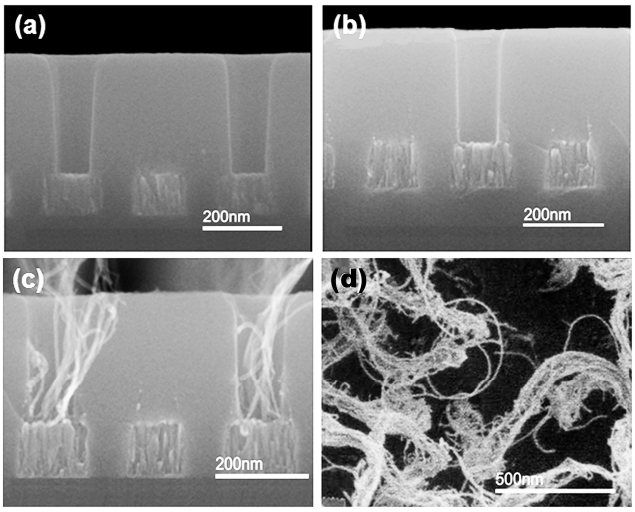

Fig. 3. (a) SEM image of as-etched via hole using a conventional etch condition, (b) and (c) SEM images of CNT growth test on via hole samples etched using conventional etch conditions and 2-step etch scheme designed in this work, respectively, (d) magnified top view SEM image of (c).

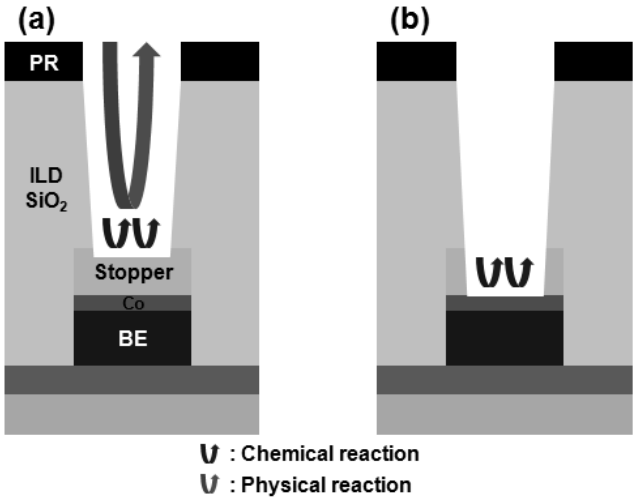

Fig. 4. Schematic illustration of 2-step etch scheme. (a) physical reaction dominant SiO_2 etch step and (b) chemical reaction dominant Si_3N_4 etch step.

Table 1. Specific etch conditions for conventional etch and 2-step etch designed in this work

		Conventional etch	2-step etch	
			1st-step	2nd-step
Power [W]		2000	2000	50
Pressure [mTorr]		40	40	10
Etch gas [sccm]	Ar	1000	1000	0
	Etchant	C4F6 25 O2 25	C4F6 25 O2 25	CF4 50 O2 30
Time [s]		30	30	100

was remained or not from the as-etched SEM images. We judged the success of etch stopping on the Co catalyst layer only in case that CNTs were grown well. As shown in Fig. 3(b), there is no CNT grown in the via hole. Integration of CNT interconnection using the conventional etch condition is extremely difficult for its small process margin and poor process reliability. Co catalyst is hard to be etched for its chemical inertness under the conventional dry etch process. However, we used very thin Co catalyst layer for growth of CNTs in this work, it is easily etched away by the physical reaction of the plasma. In order to utilize the buried catalyst scheme, a novel etch-stopping scheme on the thin catalyst layer should be designed.

In this work, we design a two-step etch scheme as shown in Fig. 4, which includes physical reaction dominant SiO_2 etch step and a chemical reaction dominant Si_3N_4 etch step.

In the first step as shown in Fig. 4(a), a large amount of Ar gas (1000 sccm) with a small amount of fluorine-based etchant gas is used for the physical etch. We adopt high plasma power of 2000 W and large amount of Ar flow rate to obtain a high physical reaction. Under this plasma etch condition (conventional SiO_2 etch condition), we could obtain high etch selectivity (greater than 10:1) which etches SiO_2 layer well and not Si_3N_4 layer. Therefore etch process stops on the Si_3N_4 stopper layer automatically. In the second step as shown in Fig. 4(b), fluorine-based etchant gas without Ar gas is used. Since we used low plasma power of 50 W and no Ar gas, etch rate in the second step was quite low, consequently resulting in extremely low etch damage of the Co catalyst layer. Since Co is chemically inert under this plasma condition, etch selectivity between Si_3N_4 and Co is greater than 100:1 in the second step. Therefore we achieved a fine etch-stop on the ultra thin Co catalyst layer, on which CNTs can be grown. CNT growth results are shown in Fig. 3(c) and (d), respectively. Curved CNTs were grown selectively only in the via holes, as shown in Fig. 3(d). Specific etch conditions proposed in this work are summarized in table 1.

4. Conclusion

We have successfully grown CNTs only in the via holes selectively, resulting in via interconnects with full compatibility with conventional semiconductor process. Via etch is successfully stopped on the ultra thin Co catalyst layer using the two-step etch scheme, resulting in extremely low etch damage of the Co catalyst layer. The density of CNT is calculated about 4×10^{11} /cm^2 in the 80 nm via hole.

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