Verification of New Family for Cascade Multilevel Inverters with Reduction of Components

M. R. Banaei[†] and E. Salary*

Abstract - This paper presents a new group for multilevel converter that operates as symmetric and asymmetric state. The proposed multilevel converter generates DC voltage levels similar to other topologies with less number of semiconductor switches. It results in the reduction of the number of switches, losses, installation area, and converter cost. To verify the voltage injection capabilities of the proposed inverter, the proposed topology is used in dynamic voltage restorer (DVR) to restore load voltage. The operation and performance of the proposed multilevel converters are verified by simulation using SIMULINK/MATLAB and experimental results.

Keywords: Cascaded multilevel converter, New topology, Reduction of components, DVR

1. Introduction

Multilevel power converters can be considered as voltage synthesizers, in which the output voltage is synthesized from many discrete smaller voltage levels. Compared with the traditional two-level voltage inverter, the main advantages of the multilevel inverter are having smaller output voltage step, lower harmonic components, better electromagnetic compatibility, and lower switching losses [1], [2]. Multilevel converters are the most attractive technology for medium to high voltage range, which includes motor drives, power distribution, power quality, and power conditioning applications. It is important that the multilevel inverter is introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors [3]. Conventionally, multilevel inverters are divided into three basic structures: diode-clamped multilevel inverter (DCMLI), flying-capacitor multilevel inverter (FCMLI), and H-bridge inverter [4], [5]. In recent years, many topologies have been suggested to multilevel converter with a low number of switches and gate driver circuits [6], but proposed topology has less switches than that of [6] in symmetric topology due to particular switching algorithm The modulation methods used in multilevel inverters can be classified according to switching frequency. Methods that work with high switching frequencies have many instances of switching at one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal pulse width modulation (SPWM), which uses the phase-shifting technique to reduce the harmonics in the load voltage [7]-[9]. The main disadvantages of multilevel converters are

their use of a larger number of semiconductors and a complex control circuitry and their requirement to equilibrate the voltage at the boundaries of the capacitors. Meanwhile, the cascaded multilevel configuration of the inverter has the advantage of being simple compared to a DCMLI or a FCMLI. Whereas the cascaded topology requires a separate DC-link capacitor for each cell, the configurations of DCMLI or FCMLI require additional diodes or capacitors, requiring a complex control strategy to regulate the voltage across each capacitorModern industrial processes are based on a large number of electronic devices such as programmable logic controllers and adjustable speed drives. The power quality of distribution system can be enhanced using custom power devices such as dynamic voltage restorer (DVR). To restore the load voltage, the DVR, which is installed between the supply and a sensitive load, should inject voltage and active power to the distribution system during voltage disturbance [10]-[12].

This paper presents a novel cascaded topology for multilevel converters. This topology consists of half of the H-bridges and H-bridge output stage. The proposed multilevel converter can be used as symmetrical or asymmetrical. The multi-carrier sub-harmonic pulse width modulation (MCSHPWM) method is applied for switching in the proposed cascaded topology. In order to verify the capabilities of the proposed inverter in the injection of voltage, the proposed topology is used in the DVR to restore load voltage.

2. Cascade Multilevel Inverters

Single-phase topology of a cascade multilevel inverter is shown in Fig. 1. An output phase voltage waveform of a cascade inverter with isolated DC voltage sources is achieved by summing the output voltages of bridges. The output phase voltage of a cascade inverter is obtained by the following:

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† Corresponding Author: Electrical Engineering Department, Faculty of Engineering, Azarbaijan University of Tarbiat Moallem, Tabriz, Iran. (m.banaei@azaruniv.edu)

* Electrical Engineering Department, Faculty of Engineering, Azarbaijan University of Tarbiat Moallem, Tabriz, Iran.

$$V_O = V_{O1} + V_{O2} + ... + V_{On} \qquad (1)$$

The DC voltage sources of all H-bridge cells are the same, with the maximum number of levels of phase voltage given by the following:

$$m = 2n + 1 \qquad (2)$$

Where n and m are the number of DC voltage source and the maximum number of levels of phase voltage, respectively. These multilevel inverters are called symmetrical multilevel inverter. The maximum output voltage (V_{Omax}) of the cascade topology is as follows:

$$V_{O\max} = V_1 + V_2 + ... + V_n \qquad (3)$$

The cascade H-bridge converter consists of power conversion cells, each supplied by an isolated DC source on the DC side and series connected on the AC side. The two main components of the power losses in a switch are conduction losses and switching losses. The $2n$ switches of the basic element shown in Fig. 1 must always be turned on in different modes of converter operation, thus it is enough to change (3) to (4) in order to consider the on-state voltage drop of the switches.

$$V_{O\max} = V_1 + V_2 + ... + V_n - 2nV_D \qquad (4)$$

Where V_D is the on-state voltage drops of one switch. To provide a large number of output steps without increasing the number of DC voltage sources, asymmetric multilevel converters (AMC) can be used. The DC voltage sources are proposed to be chosen according to a geometric progression with a factor of two or three. In an AMC based on a geometric progression with a factor of two (binary), all the partial asymmetry factors are equal to two, and the total asymmetry factors are given by a geometric sequence with a factor of two. Another asymmetrical approach is to choose the total asymmetry factors in a geometric progression with a factor of three (trinary). In this case, the partial asymmetry factors are equal to three. For n-cascaded multilevel inverters, the number of voltage levels is given as follows:

$$m = 2^{n+1} - 1, \ V_i = 2^{i-1}V_{dc} \ , i=1,2,....,n \qquad (5)$$

$$m = 3^n, \ V_i = 3^{i-1}V_{dc} \ , \ i=1,2,....,n \qquad (6)$$

The maximum output voltages of these n-cascaded multilevel inverters are as follows:

$$V_{O\max} = (2^n - 1)V_{dc}, \ V_i = 2^{i-1}V_{dc} ..., i=1,2,....,n \qquad (7)$$

$$V_{O\max} = (\frac{3^n - 1}{2})V_{dc} \ , V_i = 3^{i-1}V_{dc} ..., i=1,2,....,n \qquad (8)$$

Table 1 summarizes the number of levels, switches, gate drives, DC sources, and maximum available output voltages for classical cascaded multilevel converters.
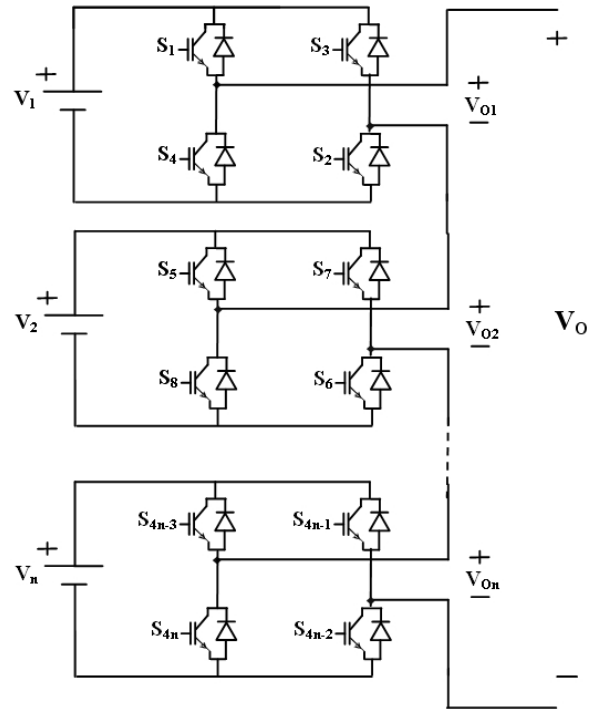

Fig. 1. Configuration of cascade inverter.

Table 1. Comparison of cascade multilevel converters

Type	Symmetric	Asymmetric	
		Binary	Trinary
DC sources	n	n	n
Voltage levels	$2n+1$	$2^{n+1}-1$	3^n
V_{Omax}	nV_{dc}	$(2^n-1)V_{dc}$	$\frac{(3^n-1)}{2}V_{dc}$
Switches number	$4n$	$4n$	$4n$

Comparing (1)-(7) and Table 1, it can be seen that the AMC can generate more voltage levels and higher maximum output voltage with the same number of bridges. Several modulation strategies have been proposed for symmetrical multilevel converters. They are generally derived from the classical modulation techniques used for more traditional converters. Among these methods, the most commonly used is the multi-carrier sub-harmonic pulse width modulation (MCSHPWM), the principle of which is based on a comparison of a sinusoidal reference waveform with shifted carrier triangular waveforms.

Some of the drawbacks of cascaded multilevel converters are their many components, complex control circuitry, and the need for separate DC sources.

3. The Proposed Multilevel Converter Topology

In all well-known multilevel inverter topologies, the required number of power devices depends on the output voltage level. However, increasing the number of power

semiconductor switches also increases the inverter circuit size, cost, and control complexity. To obtain a desired number of output levels without increasing the number of semiconductor switches, a novel topology for multilevel converters is proposed in this paper. Two different methods of determining the magnitudes of DC voltage sources are proposed. The first method is used in the proposed symmetric multilevel converter and second method is used in the proposed asymmetric multilevel converter. Although the novel topology requires multiple DC sources, they may be available in some systems through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries.

Fig. 2 shows a novel topology for multilevel inverter. An output phase voltage waveform of a proposed cascaded inverter with isolated DC voltage sources like cascade inverter is obtained by summing the output voltages of the bridges. This inverter has two rows of switches (arms) and one H-bridge cell. The switches (arms) produce waveform with one polarity in two half periods and the H-bridge cell inverses waveform in half period. Thus, the other polarity of the waveform is obtained and sinusoidal waveform is produced. Zero level is produced with H-bridge cell. The maximum output voltage for this topology is obtained by summing the DC voltage sources. There are many possibilities to feed the partial basic unit inverters to enhance the number of output voltage levels.

If all DC voltage sources in Fig. 2 are equal to V_{dc} ($V_1 = V_2 = ... = V_n = V_{dc} = 1$ per unit (p.u.)), the inverter is called symmetric multilevel inverter. The effective number of output voltage levels in this inverter is the same as the symmetric cascade inverter and is given by (2). The maximum output voltage for this topology is equal to the sum of the DC voltage sources. The maximum input voltage to the H-bridge (V_{abmax}) of this new topology is as follows:

$$V_{ab\max} = nV_{dc} \qquad (9)$$

The switching algorithm is the MCSHPWM; the reference waveforms are sine wave and absolute of sine wave. At each instant, the absolute sine wave and sine wave are compared with the carrier signal (triangular waveforms). To generate m levels, $(m+1)/2$ carriers are needed. The number of carriers used in switching basic switches (half bridges or arms) is $(m-3)/2$, and two carriers are used to switching the H-bridge cell. Fig. 3 shows a proposed topology with four DC voltage sources. The magnitude of each voltage source is considered, $V_{dc} = 1$ p.u. The modulation waveforms to switching are shown in Fig. 4; Fig. 4(a) shows the modulation waveforms to switching basic switches. The switching algorithm for the basic switches is MCSHPWM, but the reference waveform is the absolute of sine wave. For example, if the sine wave is greater than the second carrier and lower than the third carrier, then S_2, S_3, and S_5 are turned on and the second level is produced. The modulation waveforms to switching H-bridge cell for the proposed cascaded topology is shown in Fig. 4(b). Fig. 5 shows the circuit that produces gates signals. In any arm, one switch is turned on and the other is turned off. The operation of the proposed multilevel converter is described by Fig. 6, which shows the relation between the input signals of the switches gate (switching) and the output waveform of voltage.

The input signals of the basic switches (arms) gate at one period are shown in Fig. 6(a). With this switching, the input voltage of the H-bridge cell (V_{ab}) is produced, as shown in Fig. 6(b). Table 2 presents the output voltage level and configurations of the switches for half period in the proposed configuration. Figure 6(c) shows the input signals of the H-bridge switches gate. The switching function of the H-bridge cell produces zero level and inverses
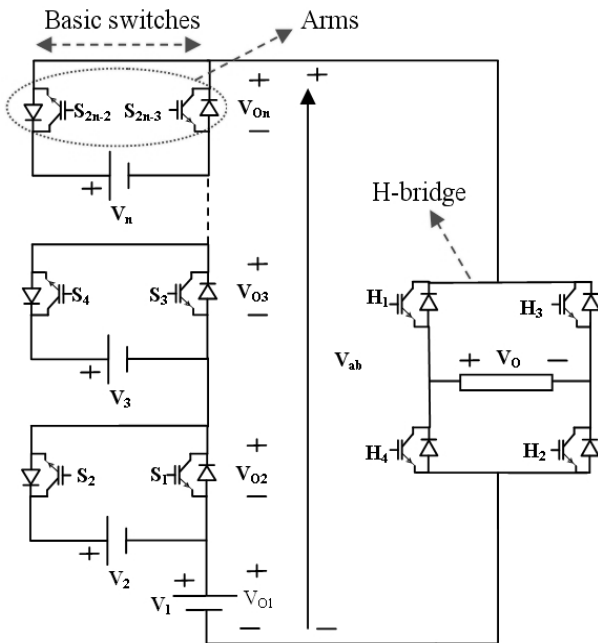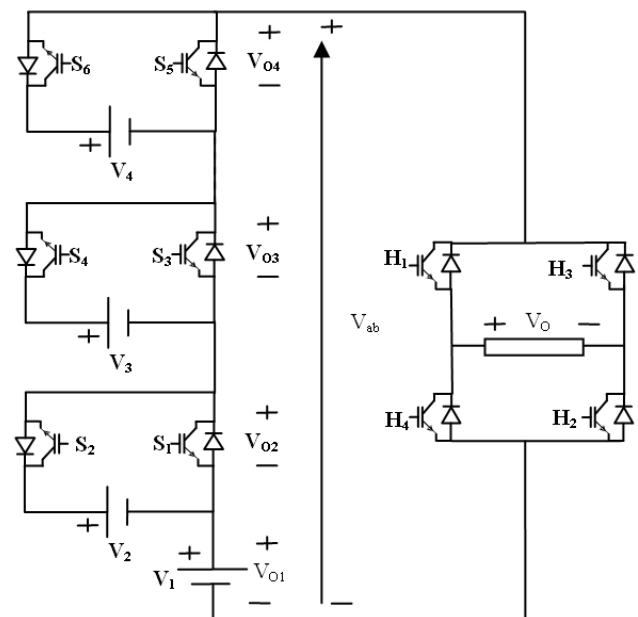

Fig. 2. Proposed cascade topology

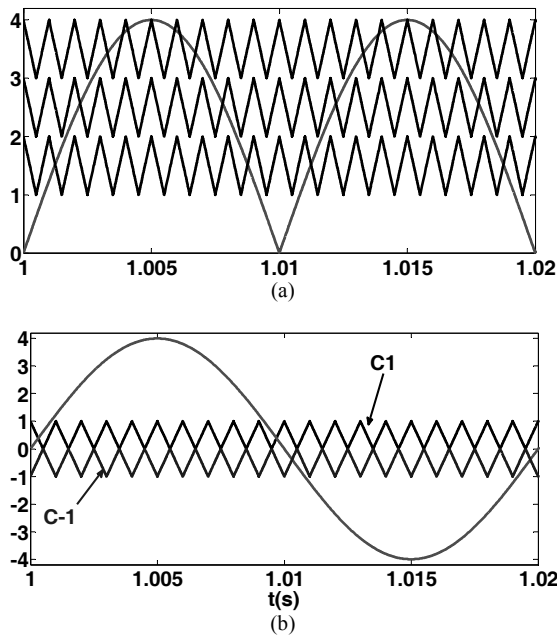**Fig. 3.** Proposed topology with four DC voltage sources.

(a)

(b)

Fig. 4. Modulation waveforms to switching the nine-level proposed topology.

Table 2. Output voltage level and configurations of switches for half period in the proposed topology

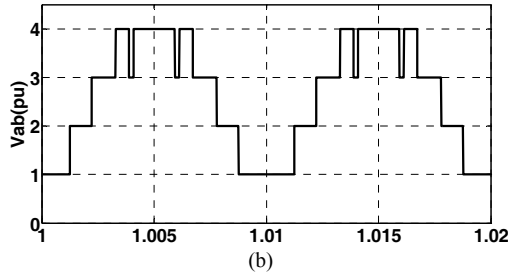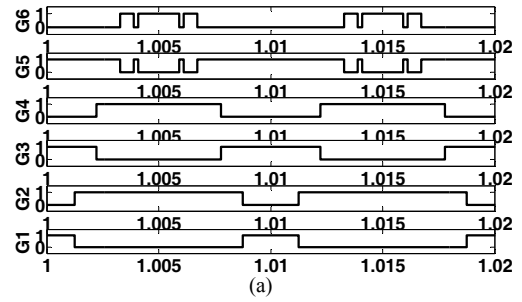| State	Switches on	Output level
1	H_1, H_3 or H_2, H_4	0
2	S_1, S_3, S_5	1
3	S_2, S_3, S_5	2
4	S_2, S_4, S_5	3
5	S_2, S_4, S_6	4
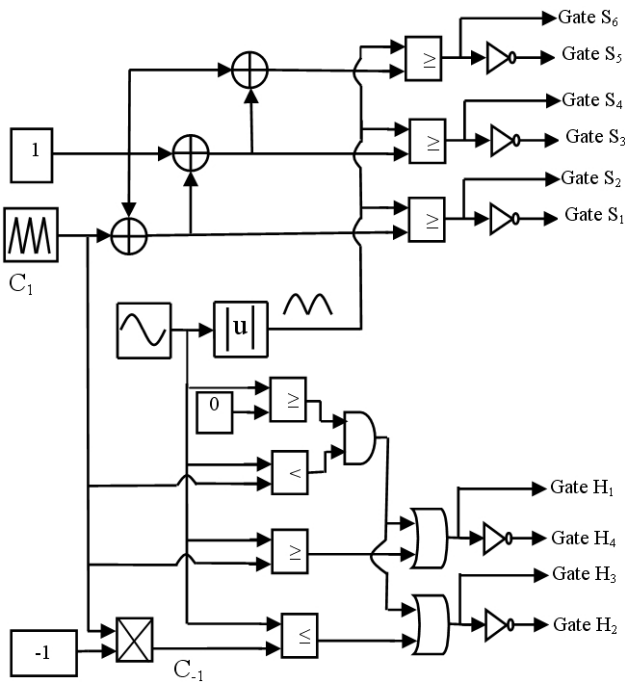
Fig. 5. Gates signals generator.
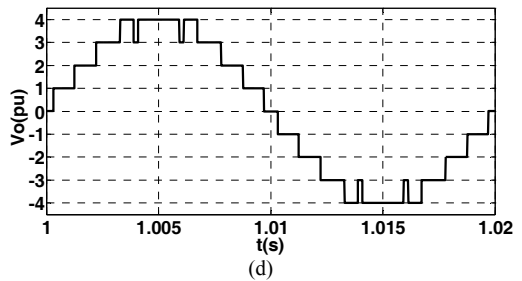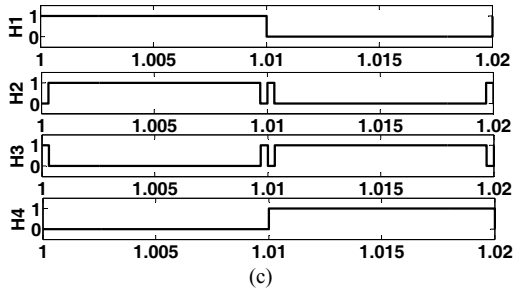
Fig. 6. Operation of the proposed converter: (a) input signal of the basic switch; (b) input voltage to the H-bridge cell; (c) input signal of H-bridge; and (d) output voltage.

waveform in half period to obtain output voltage. Both switches H_1 and H_4 or H_2 and H_3 cannot be on concurrently because a short circuit across the voltage V_{ab} would be produced. The output voltage waveform shown in Fig. 6(d) is a typical staircase nine-level waveform.

If the voltage source V_1 is eliminated from Fig. 2, then the proposed multilevel inverter can be used as asymmetric converter. The corresponding asymmetrical topology provides more flexibility to the designer and can generate a large number of levels without increasing the number of switches. In this paper, the DC voltage source levels are chosen according to a geometric progression with a factor of two (binary) in the asymmetric state. The number of output voltage levels and the maximum output voltage are

calculated by (5) and (7), respectively, which is similar to the AMC cascade based on a geometric progression with a factor of two.

Fig. 7 shows the configuration of a 15-level proposed multilevel inverter. It has a main H-bridge inverter H_1–H_4, six basic switches S_1–S_6, and three DC sources. The supplying voltages are $V_1 = 1$ p.u., $V_2 = 2$ p.u., and $V_3 = 4$p.u.

Fig. 8 shows the operation of the proposed asymmetric multilevel inverter. The function of the basic switches is to control the connection of the DC sources in order to construct the staircase output voltage. In the asymmetric state, the switching algorithm is MCSHPWM, which is similar to the proposed symmetric converter. The required gating signals of the basic switches are shown in Fig. 8(a). Meanwhile, the input voltage to the H-bridge cell is presented in Fig. 8(b); this voltage has one polarity. Figure 8(c) shows the input signals of the H-bridge switches gate. Zero level is produced with basic switches, and the H-bridge cell only inverses waveform in half period. The output voltage is shown in Fig. 8(d).

The main advantage of the proposed asymmetric structure is the generation of considerable number of DC voltage levels with less number of DC voltage sources and switches. In each arm of this circuit, one DC voltage source is common between two switches, resulting in the reduction of the number of switches, losses, installation area, and cost of the converter.
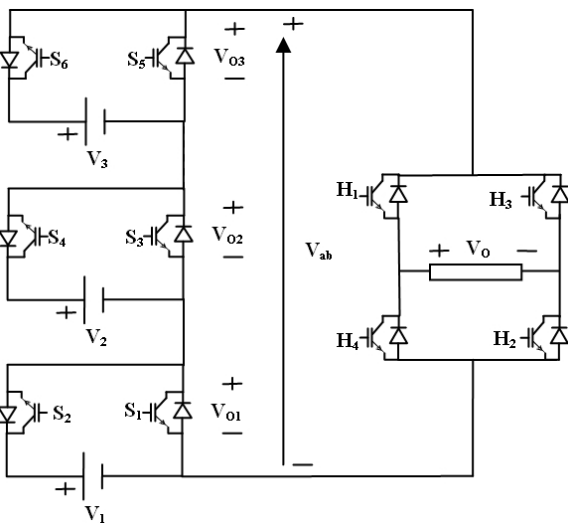

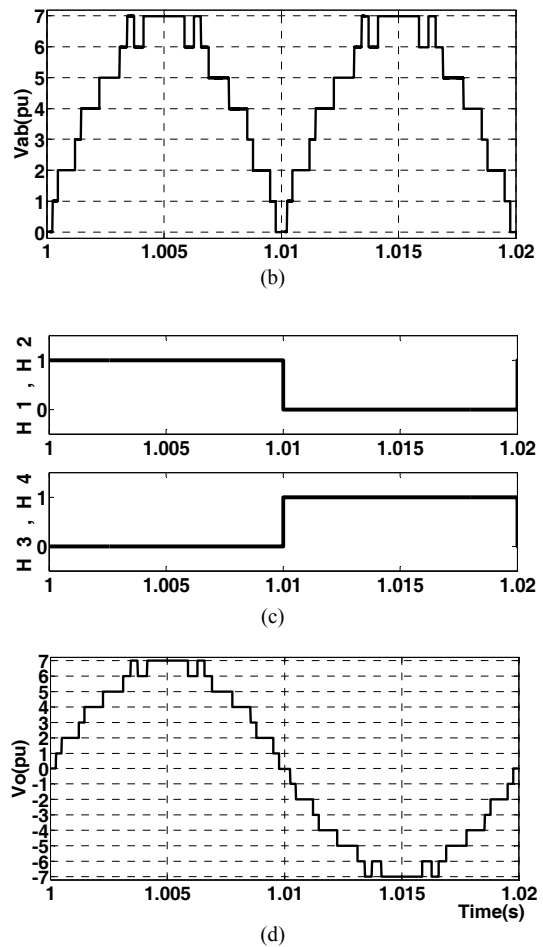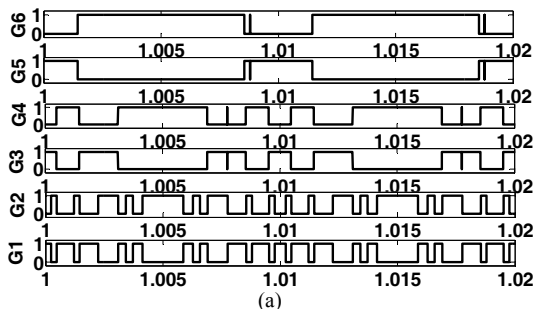**Fig. 7.** The proposed 15-level asymmetric multilevel inverter.

(a)

Fig. 8. Operation of the proposed converter: (a) input signal of the basic switch; (b) input voltage to the H-bridge cell; (c) input signal of H-bridge; and (d) output voltage.

4. Comparison Study

The main purpose of this paper is to reduce the components of the cascaded multilevel inverters. The proposed multilevel converter can generate DC voltage levels that are the same as the cascade topology with less number of semiconductor switches. In the proposed multilevel converters, semiconductors that are put on in the arms are switched in two half periods and those put on in the H-bridge cell are almost switched with fundamental frequency. The number of switches is reduced and the devices can be switched at low frequency; therefore, the converters have higher efficiency. These switches have much lower *dv/dt*. The switching algorithm is easy and not complex. Each switch requires one gate driver, the reduction of which is obtained with the reduction of the number of switches. The current and voltage ratings are significant problems that affect the cost of the inverters. In the proposed topologies, the currents of all switches are equal to the rated current of the load. The peak voltage of the basic switches (arms) is equal to the magnitude of one DC

source in symmetric or asymmetric state.

In the AMC, the peak inverse voltage (PIV) of the switches is achieved according to the progression factor. The PIV of switches is represented by the following:

$$PIV == \sum_{i=1}^{K} Vsw, i \qquad (10)$$

Where K and V_{sw} are the number of switches and the peak inverse voltage of the switches, respectively. Tables 3 and 4 summarize the number of switches, DC voltage sources, and PIV for the cascade multilevel and proposed topology, respectively, where m is the number of levels.

The PIV of all the basic switches in the novel cascaded inverter is less than that in the conventional cascaded topology, although the H-bridge cell in the proposed topology needs switches with high capability for the PIV. Additionally, it is important to note that the H-bridge cell needs switches with high capability of withstanding the voltage. However, the drawback of this new group is the high rating of the main H-bridge switches as they have to withstand the whole DC bus voltage. Therefore, this new group of multilevel inverters is recommended for medium-power applications.

Fig. 9 shows the comparison of the number of switches between the topology suggested in this paper and the conventional cascade topology in symmetric and asymmetric states. This figure shows that the suggested topology needs fewer switches for generating same levels of output voltages.

Table 3. Conventional cascade multilevel converter

Type	Symmetric	Asymmetric	
		Binary	Trinary
DC sources	$\dfrac{(m-1)}{2}$	$\dfrac{Ln(m+1)}{Ln2}-1$	$\dfrac{Ln(m)}{Ln3}$
Switches	$2(m-1)$	$4\dfrac{Ln(m+1)}{Ln2}-4$	$4\dfrac{Ln(m)}{Ln3}$
PIV	$2(m-1)$	$2(m-1)$	$2(m-1)$

Table 4. Proposed multilevel converters

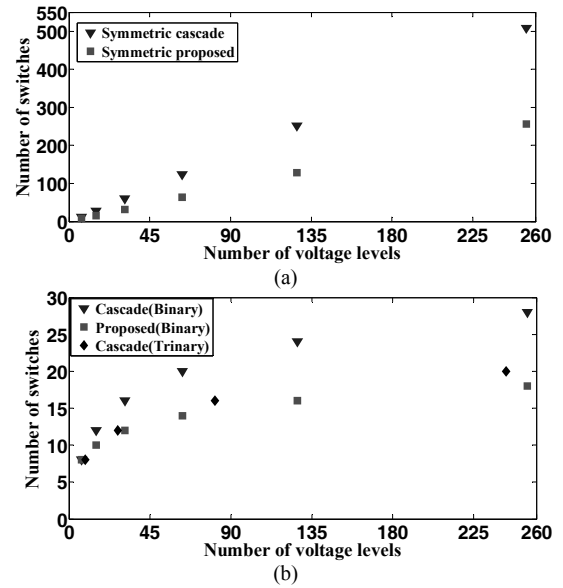| Type	Symmetric	Asymmetric (binary)
DC sources	$\dfrac{(m-1)}{2}$	$\dfrac{Ln(m+1)}{Ln2}-1$
Switches	$m+1$	$2\dfrac{Ln(m+1)}{Ln2}+2$
PIV of basic switches	$m-3$	$m-1$
PIV of H-bridge switches	$2(m-1)$	$2(m-1)$
PIV of all switches	$3m-5$	$3(m-1)$

Fig. 9. Comparison number of switches: (a) symmetric state and (b) asymmetric state.

5. Case Study

DVR is a device used to guard sensitive loads against voltage disturbances such as voltage sag and swell; it can inject a controllable voltage in series with the supply voltage to keep the voltage constant at the load terminals [10]-[12]. The basic configuration of the case study is described in Fig. 10. As can be seen, the voltage source converter (VSC) is installed in series with line. The DVR consists of three single-phase multilevel converters, a disturbance identification unit, a control unit, and a modulation unit. Installing an output LC filter reduces the pulse-modulated voltage into the sinusoidal voltage. The series connection can then be performed by the single-phase transformers. The transformers not only reduce the voltage rating of the inverters but also provide isolation between the inverters and the AC system. In the suggested DVR, the transformers are eliminated. These transformers have disadvantages such as being expensive, requiring a large installation area, the magnetization of DC and surge over-voltages resulting in control problems; in addition, their failure rate is much higher than converters. The suggested inverter used in the DVR does not require any coupling series transformer and has lower cost, smaller size, and higher performance and efficiency. The technique of output feedback control is incorporated to determine the switching actions of the inverters. The measured voltages are the inputs to the disturbance identification unit, giving signals to the control unit, which in turn generates the voltage references. The voltage references are then used to generate the modulating signals for the switches of the converter. The required active power to compensate the voltage disturbances is provided by the energy storage element (batteries). The $V_S(t), V_{inj}(t)$, and $V_O(t)$ are the supply voltage, DVR injection voltage, and

load voltage, respectively. As shown in Fig. 12, the load voltage is as follows:

$$V_O(t) = V_S(t) + V_{inj}(t) \qquad (11)$$

If the supply voltage has disturbances, the injected voltage by the DVR compensates the load voltage.

6. Simulation Results

To examine the performance of the proposed multilevel inverters in generating a desired output voltage, prototypes were simulated; a detailed system, as shown in Fig. 10, has also been modeled by MATLAB/SIMULINK to study the capability of the suggested converters. The system parameters are listed in Table 5. It is assumed that the voltage magnitude of the load bus is maintained at 1 p.u. during the voltage sags/swells conditions.

To show the capabilities of the proposed inverter, an asymmetric 15-level inverter was used in a DVR. The converter consists of three arms with the DC voltage sources V_{dc}, $2V_{dc}$, and $4V_{dc}$. This circuit is capable of producing any per unit level of between −7 and +7.
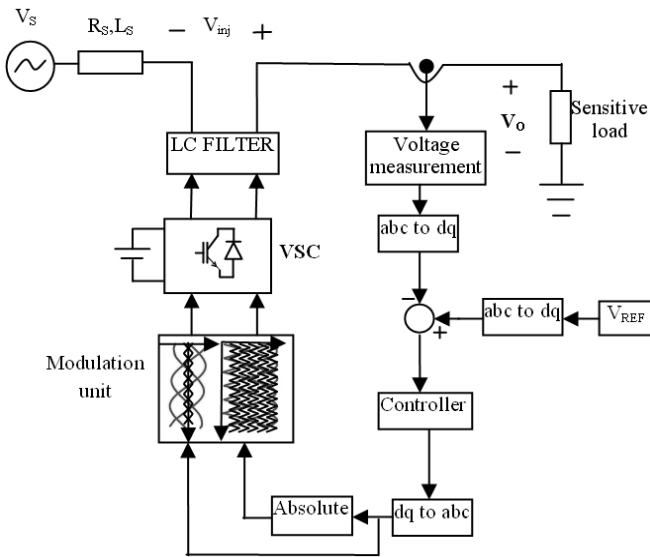

Fig. 10. Block diagram of the case study

Table 5. Case study parameters

Parameters	Value
Source voltage (V_{L_L})	400 V
Nominal frequency	50 Hz
Load impedance	12.08 + i9.424778 Ω
V_{dc}	15 V
Number of DC voltage source in any phase	3
Number of levels	15
Number of switches in any phase	10
Switching frequency	1,050 Hz
L_f, C_f	2.5 mH, 50 µF

The disturbances are discussed in two sections as voltage sag and swell.

6.1 Balanced Voltage Sag

The first simulation results show the balanced three-phase voltage sag. Fig. 11(a) shows a 30% voltage sag initiated at 0.3 seconds and kept until 0.4 seconds, with total voltage sag duration of about 0.1 second. Figs. 11(b) and 11(c) show the voltage injected by the DVR and the compensated load voltage. In the case of normal operation conditions, the load voltage is equal to 1 p.u. and the DVR output voltage is almost zero. During the voltage sag, the supply voltage decreases, whereas the DVR output voltage increases to maintain the load voltage at 1 p.u. as normal operation conditions. When the voltage sag disturbance is cleared, the DVR output voltage gets back to its initial value. It is considered that the proposed converter can generate and inject voltage so that in order for the voltage sag to be compensated.

Fig. 12 shows the output phase voltage of the proposed multilevel inverter at fault time. The multilevel converter generates staircase (near-sinusoidal) output voltage.
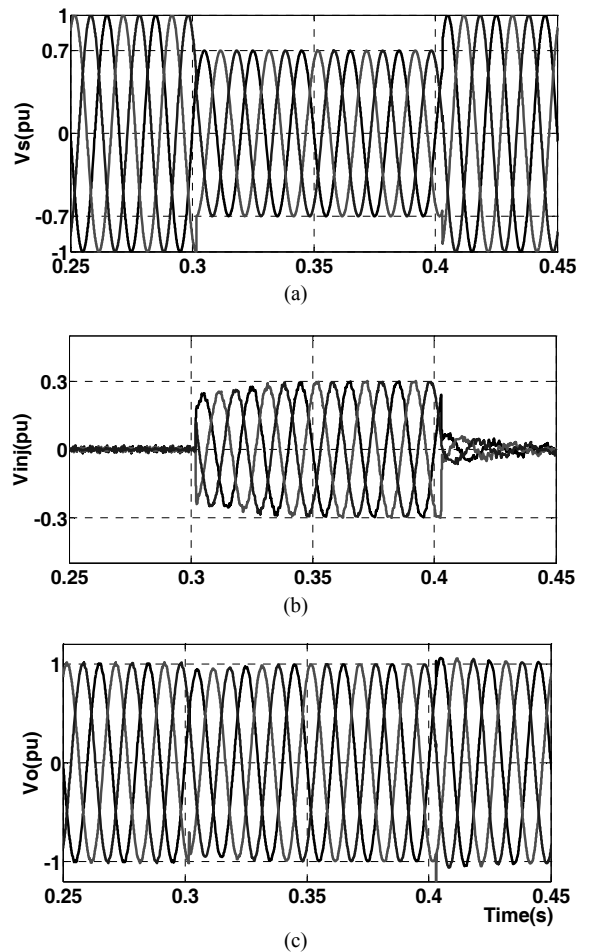

Fig. 11. (a) Supply voltage, (b) DVR injection voltage, and (c) load voltage for the three-phase balanced voltage sag.

6.2 Balanced Voltage Swell

The second simulation results show the DVR performance during a voltage swell condition. Fig. 13 shows that the three-phase voltage swells at supply voltage, DVR output voltage, and load voltage, respectively. As shown from the figure, the amplitude of supply voltage was increased by about 30% from its nominal voltage. The simulation results show that the suggested converter can compensate voltage swell, in addition to voltage sag.

Fig. 14 shows the output phase voltage of the proposed multilevel inverter at fault time. The multilevel converter generates staircase output voltage.
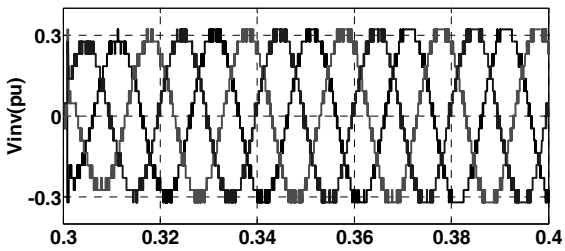
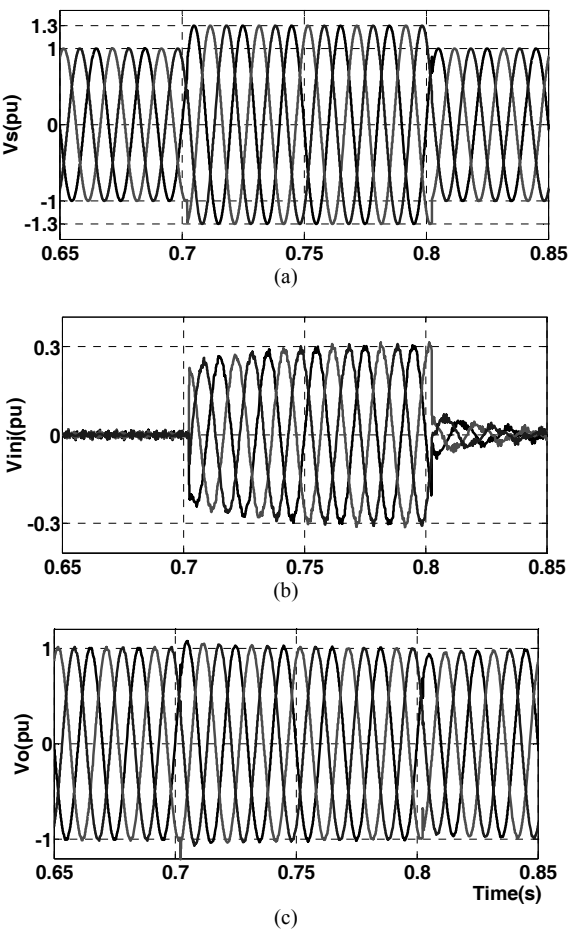**Fig. 12.** Output phase voltage in fault (sag) time.

(a)

(b)

(c)

Fig. 13. (a) Supply voltage, (b) DVR injection voltage, and (c) load voltage for the three-phase balanced voltage swell.
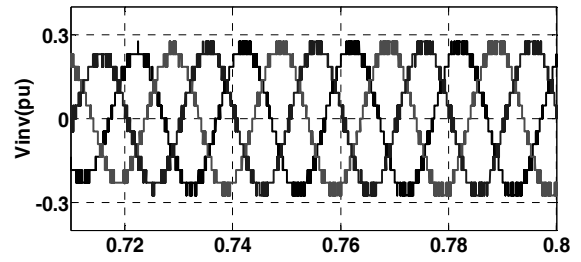
Fig. 14. Output phase voltage in fault (swell) time.

7. Experimental Results

In order to validate the proposed concept, the asymmetric inverter in Fig. 15 was constructed and tested in the 31-level mode. This multilevel inverter can generate staircase waveform with maximum of 150 V on the output. For the 31-level mode, a single-phase resistive-inductive load with parameters of $R = 170\ \Omega$ and $L = 400$ mH was connected to the output voltage. The converter consists of four arms and one H-bridge cell with DC voltage sources of 10, 120, 40, and 80 V.

Fig. 16 shows photographs of the prototype. The prototype inverter was built using BUP403 (600 V, 42A) IGBTs as switching devices, IRS2113 as IGBT driver, and BYW (56 V) as fast-recovery diodes. The IC ATMega 64 microcontroller by ATMEL Company was used to generate the switching patterns.
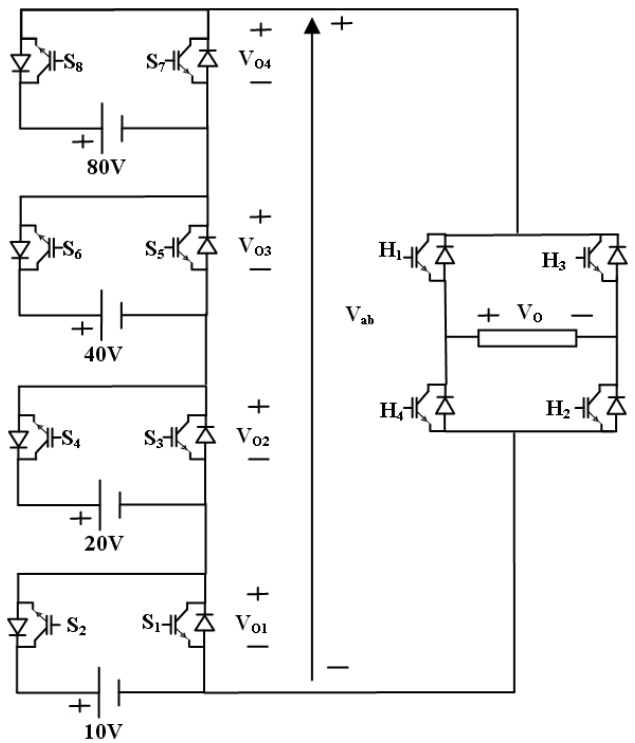
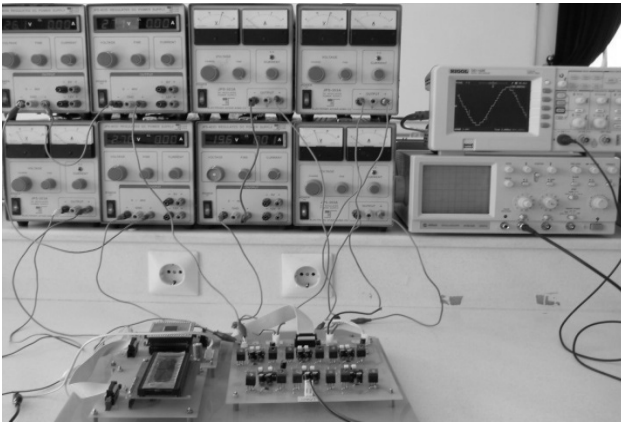**Fig. 15.** The proposed 31-level asymmetric multilevel inverter.

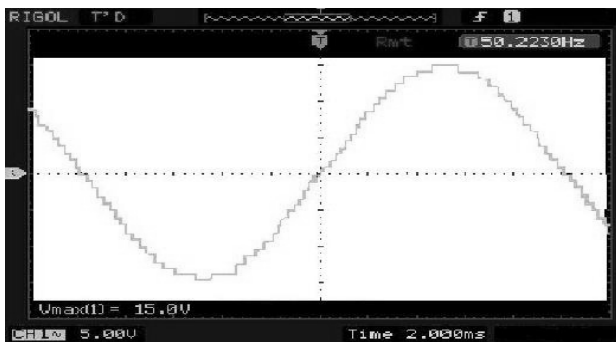**Fig. 16.** Photographs of the prototype.

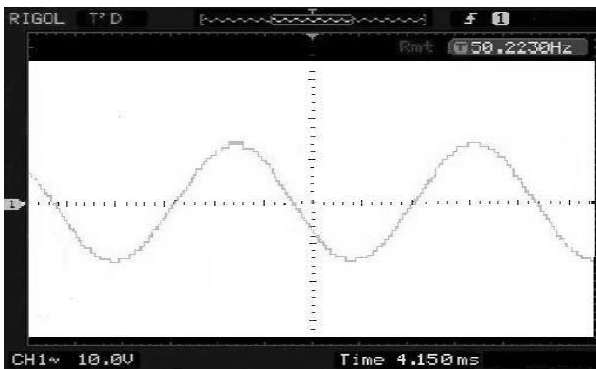**Fig. 17.** The output voltage, 5*10 volt/div.

Fig. 18. Measured load voltage, 10*10 volt/div.

Figs. 17-19 show the experimental waveforms of the voltage and current of load. Fig. 17 shows the 31-level output phase voltage in the no-load state, and the load voltage in the R-L load is shown in Fig. 18. The output voltage is almost 50 Hz staircase waveform with amplitude of 150 V. As can be seen, the results verify the ability of the proposed inverter for the generation of desired output voltage waveform.

Fig. 19 shows the load current, which is considered to be almost sinusoidal because it is inductive.

As can be seen, the high-resolution 31-level inverter with minimum device count was implemented. The 31-level PWM voltage waveform is nearly sinusoidal and has very good harmonic context.
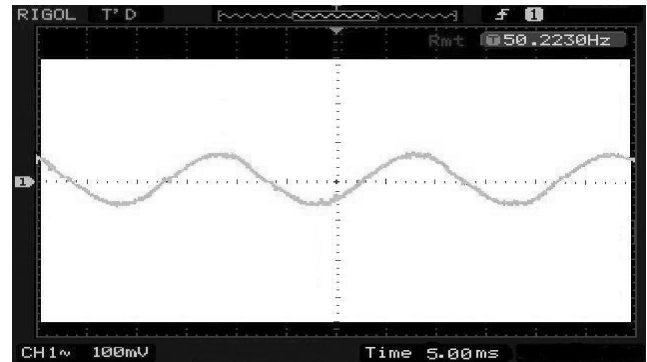

Fig. 19. Measured load current, 100 m*10 A/div.

These results confirm the high performance of the proposed inverter without increasing the number of switches.

8. Conclusions

In this paper, a novel topology was presented for multilevel converter, which has reduced number of switches. The suggested topology needs fewer switches for realizing voltages for the same levels of output voltages. This point reduces the installation area and the number of gate driver circuits. Therefore, the cost of the suggested topology is less than the conventional topology. Based on the presented switching algorithm, the multilevel inverter generates near-sinusoidal output voltage, causing very low harmonic distortion. The suggested inverter used in DVR does not require any coupling series transformer and has lower cost, smaller size, and higher performance and efficiency. Simulation results verified the validity of the presented concept.

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Mohamad Reza Banaei was born in Tabriz, Iran in 1972. He received his M.Sc. degree in Control Engineering from the Polytechnic University of Tehran, Iran in 1999 and his Ph.D. degree in Power Engineering from the Electrical Engineering department of Tabriz University in 2005. He is an Assistant Professor in the Electrical Engineering department of Azarbaijan University of Tarbiat Moallem, Iran since 2005. His main research interests include power electronics, renewable energy, modeling and controlling of FACTS devices, and power systems dynamics.

Ebrahim Salary was born in Khoram Abad, Iran in 1981. He received his B.S. degree in Power Electrical Engineering from Dezful Azad University, Dezful, Iran in 2004 and his M.S. degree from Tarbiat Moallem University of Azarbaijan, Tabriz, Iran in 2010. His main research interests are power electronics and renewable energy.