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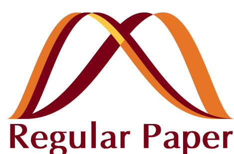
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ONO Ruptures Caused by ONO Implantation in a SONOS Non-Volatile Memory Device

Sang-Yong Kim† and Il-Soo Kim
Department of Semiconductor System, Korea Polytechnic College IV, Cheongju 361-857, Korea

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The oxide-nitride-oxide (ONO) deposition process was added to the beginning of a 0.25 μm embedded polysilicon-oxide-nitride-oxide-silicon (SONOS) process before all of the logic well implantation processes in order to maintain the characteristics of basic CMOS(complementary metal-oxide semiconductor) logic technology. The system subsequently suffered severe ONO rupture failure. The damage was caused by the ONO implantation and was responsible for the ONO rupture failure in the embedded SONOS process. Furthermore, based on the experimental results as well as an implanted ion's energy loss model, processes primarily producing permanent displacement damages responsible for the ONO rupture failure were investigated for the embedded SONOS process.

Keywords: Polysilicon-oxide-nitride-oxide-silicon, Implantation, Non-volatile semiconductor memory devices, EEPROM (Electrically erasable programmable read-only memory), Threshold voltage

1. INTRODUCTION

Non-volatile semiconductor memory devices are mainly based on floating gate devices and quantum trap devices. The increasing demand for low power, low voltage, high reliability, high program/erase speed and low manufacturing costs for high density EEPROMs (electrically erasable programmable read-only memories) has been the driving force for quantum trap devices, especially SONOS (polysilicon-oxide-nitride-oxide-silicon) devices, the most attractive candidate [1,2].

We developed an embedded SONOS process using 0.25 μm technology that allows for the implementation of non-volatile SONOS memory cells along with high performance 2.5 V logic transistors and 3.3 V I/O's on the same chip with only four additional mask steps.

However, our system severely suffered from ONO rupture failures that occurred during endurance cycling. A significant percentage of customer sample parts experienced catastrophic NV (Non-Volatile) failures prior to reaching the endurance test goal and we have made every effort to resolve this endurance failure [3,4].

† Author to whom all correspondence should be addressed:
E-mail: ksy@kopo.ac.kr

1.1 The phenomena of ONO rupture

More than 10% of the parts failed before reaching 1,000 cycles. However, a very high percentage of parts that passed 1,000 cycles did not fail for up to 1,000,000 cycles and beyond [5,6]. The source of this endurance failure was not caused by a shift in the threshold voltage but by an ONO rupture in some failed bits, which originated from weak spots such as pin holes, particles, chemical contamination, surface roughness, local thinning, substrate defects, causing the 2 Mb SONOS gate array current to increase from about 6 μA to 1 mA.

This caused an additional load on the negative charge pump, which in turn caused a full array NV (Non-Volatile) failure due to a weakened store cycle, as seen in Fig. 1.

Figure 2 shows the positive current ramping stress test results used to characterize the ONO rupture failure. This exhibited that our current embedded SONOS process possessed a very severe reliability issue caused by a lack of ONO quality.

Figure 3 shows the ONO rupture failure points in the planar type ONO capacitor test pattern that were found by the optical beam induced resistance change (OBIRCH) test and de-processing and therefore shows us that localized weak ONO spots are responsible for the ONO rupture failures. Therefore, we must quantify the ONO rupture failure in order to obtain a reliable embedded SONOS Process [7,8].

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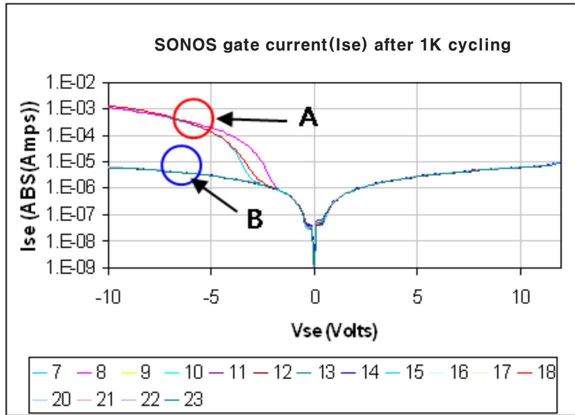

Fig. 1. The SONOS gate array current through the ONO after 1 K cycling, A : the ONO rupture failed parts, B : the good parts.

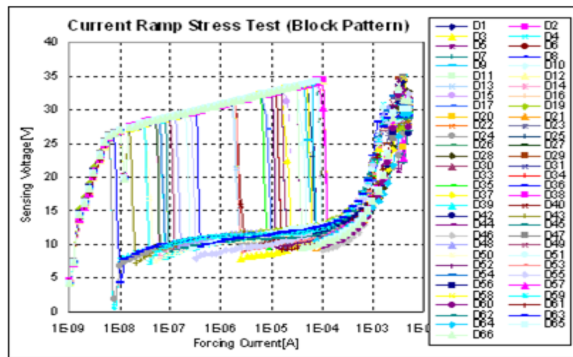

Fig. 2. The positive current ramping stress test (planar ONO capacitor pattern 21,000 μm^2).

2. EXPERIMENTS

Figure 4 shows the simple flow of our current embedded SONOS process using 0.25 μm technology. Basically, in order to preserve the characteristics of the logic transistors and other components already set up in our manufacturing line, all of the additional implemented steps for the SONOS transistor needed to be processed before the logic CMOS well formation process.

In this paper, we present only the SONOS transistor formation process with the exception of the logic CMOS formation process. The first active areas were defined by photolithography and etching processes. The first active areas are areas in which the SONOS transistor, logic transistors, and other components were formed. After the formation of the active areas, additional implantation, called the Cell Vt implant, was performed in order to adjust the threshold voltage of the SONOS transistor to about ~0 V using phosphorus. Then the ONO multi-dielectric layer was deposited onto the whole wafer area, followed by a densification process. After the ONO multi-dielectric layer deposition and densification process, the ONO multi-dielectric layer regions, in which the SONOS transistor was formed, were defined through the photolithography and etching processes. After the ONO regions for the SONOS were defined, the logic well was formed and the p-well regions for SONOS transistor were formed through this logic well process. Thereafter, all of the remaining processes remained the same as the conventional logic CMOS process and therefore the detailed process sequences are not shown here.

We focused on the fact that in our embedded SONOS process, the Vt adjustment implantation, the punch-through implantation, the channel stop implantation as well as the pwell implantation for the logic NMOS transistor were directly introduced

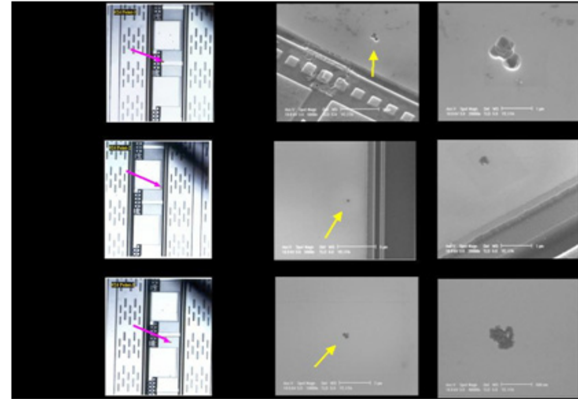

Fig. 3. The OBIRCH test and the de-processing results in the planar type ONO capacitor pattern.

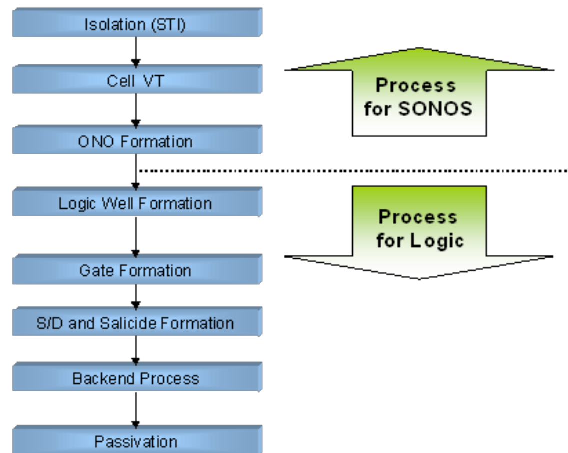

Fig. 4. The simplified embedded SONOS process flow.

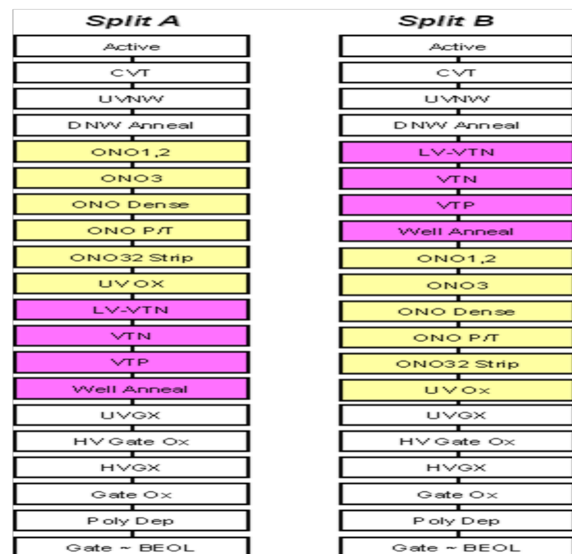

Fig. 5. The schematic process flow for the ONO rupture improvement in the embedded SONOS process, Split A : the current baseline process flow, Split B : the new process flow.

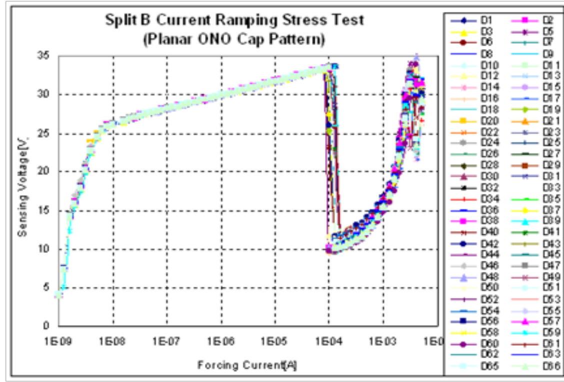

Fig. 6. The positive current ramping stress test in Split B (new process split group), (planar ONO capacitor pattern 21,000 μm^2)

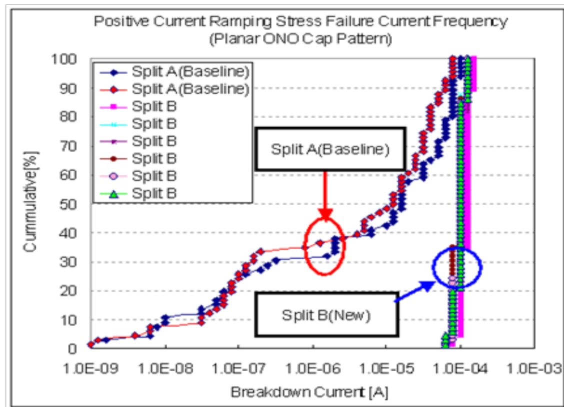

Fig. 7. The failure current frequency in the positive current ramping stress test (planar cap pattern 21,000 μm^2)

into the ONO for the SONOS transistor, so we postulated that the ONO rupture failure of the SONOS was due to process induced ONO damage, not by bad intrinsic ONO quality, emphasizing ONO implantation damage. To demonstrate our hypothesis on the root-cause of the ONO rupture failure,

we prepared two kinds of samples. One was processed with our current embedded SONOS process (Fig. 5 Split A) and the other was processed with a new embedded SONOS process (Fig. 5 Split B), in which we transferred all of the well implantation processes from the after ONO multi-dielectric layer deposition process to a before ONO multi-dielectric layer deposition process. Table 1 represents the detailed implantation conditions for the logic NMOS transistor.

3. RESULTS AND DISCUSSION

3.1 Experiment results

For the examination of ONO rupture reliability, a planar type ONO capacitor test pattern (area = 21,000 μm^2) was submitted to an accelerated test using positive current ramping stress measurements. Figure 6 shows the positive current ramping stress test results in the new process group (Split B) in which all of the well implantation processes were fulfilled before the ONO multi-dielectric layer deposition process. It showed a very good and uniform ONO quality in comparison to the current embedded SONOS process.

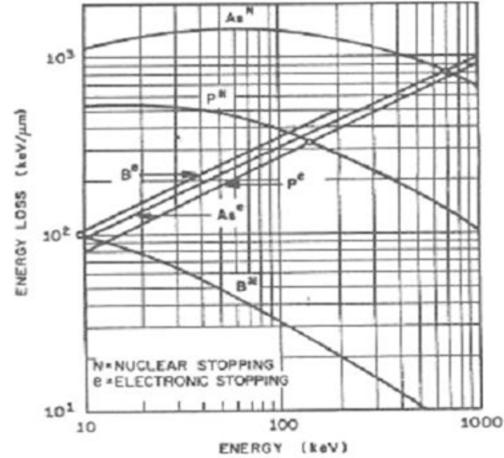

Fig. 8. The energy loss for As, P and B at various energies.

Table 1. The implantation conditions for the logic NMOS transistor.

V_t adjust imp.	Boron, 4.1E12, 20 keV
Punch-through imp.	Boron, 6.5E12, 70 keV
Channel stop imp.	Boron, 3.4E12, 180 keV
P-well imp.	Boron, 3.5E13, 500 keV

Figure 7 represents the failure current frequency in the positive current ramping stress test in the planar type ONO capacitor test pattern. The 1 μA positive stress current for 34 μs was thought to be a marginal current level for the ONO rupture failure screening, so therefore, the ONO rupture failure would be over 30% in our current embedded SONOS process (Split A), whereas it would never occur in the new embedded SONOS process (Split B). It was very evident that the ONO implantation significantly degraded the ONO quality and was completely responsible for the ONO rupture reliability issue in the current embedded SONOS process.

Thus, we can obtain an ONO rupture free embedded SONOS process with a very good and a very reliable ONO quality by switching all of the well implantation processes from after the ONO multi-dielectric layer deposition process to before the ONO multi-dielectric layer deposition process.

3.2 Implantation damage mechanism

As an implanted ion moves through a solid target such as silicon, silicon dioxide, or silicon nitride, it transfers energy by colliding with the target nuclei, which is referred to as nuclear collisions, and by coulombic interaction with the electrons in the target material, which is referred to as electronic collisions. In the latter mechanism, the energy transferred to the electrons can lead to the excitation of the electrons to higher energy levels, or to ionization by the ejection of electrons from their atomic orbits. The energy loss due to such target interactions gradually slows the implanted ion, eventually bringing it to a stop. The total rate of energy loss of an implanted ion is given by the sum of the energy loss through nuclear collisions and electronic collisions. Fig. 8 shows that the nuclear stoppage increases at low energies, reaches a maximum at some intermediate energy, and decreases at higher energies, because at a high velocity the implanted ions move past the target nuclei too quickly to efficiently transfer energy to them. It is important to note that the energy loss due to nuclear collisions increases with the mass of the implanted ion and thus heavy ions, such as arsenic or phosphorus,

will transfer much more of their energy through the nuclear collisions than light ions, such as boron. When energetic ions strike a solid target, they lose their energy in a series of nuclear and electronic collisions. However, only the nuclear collisions result in the displacement of the atoms which compose a solid target. If the energy transferred to the atom of a solid target is less than the required energy needed to displace it from its lattice site, no displacement event occurs but if the energy transferred to the atom of a solid target is more than the required energy needed to displace it from its lattice site, a single point defect, multiple defects, or defect clusters are created.

As shown in Fig. 8, at the initial impact energies, most of the energy loss for the light ions, such as boron, is due to electronic collisions which do not produce displacement damage. However, as the boron ions penetrate deeper into the lattice of a solid target, they lose energy and eventually, a cross-over point is reached, below which nuclear stopping predominates. Thus, most of the solid target lattice damage occurs in the part of the light ion trajectory that is beyond that point.

As shown in Table 1, the implantations through the ONO multi-dielectric layer consist of four steps, which are the V_t adjust implantation, the punch-through implantation, the channel stop implantation and the pwell implantation and according to Fig. 8, in the case of over an 180 keV boron ion has an initial nuclear energy loss of less than 2 eV/ Å. Thus, the boron ion will lose less than 5 eV from nuclear collisions for each lattice plane of silicon, silicon dioxide and silicon nitride. Since 5 eV is less than the displacement energy in the silicon, silicon dioxide and silicon nitride lattices at the initial implantation stage, it does not displace the atom of the lattice through nuclear collisions. Therefore the channel stop implantation and pwell implantation scarcely produced any displacement defects in the block oxide, trap nitride, tunnel oxide as well as the silicon surface because their implantation energies are all over 180 keV. However, in the case of a less than 70 keV boron ion, the initial nuclear energy loss was greater than 4 eV/Å. Thus the boron ion will lose more than 10 eV from nuclear collisions for each lattice plane of silicon, silicon dioxide and silicon nitride. This 10 eV or more is able to displace the atom from the silicon, silicon dioxide and silicon nitride lattice site at the initial implantation stage. Therefore the punch-through implantation and the Vt adjust implantation can make displacement defects in the block oxide, trap nitride, tunnel oxide as well as the silicon surface because their implantation energies were all less than 70 keV. Although many of these displacement centers were recovered by the following thermal annealing, some damages never healed so these remaining displacement centers increased the leakage current and the rupture failure of the ONO multi-dielectric layer, and decreased the charge-to-breakdown and the breakdown voltage of the ONO multi-dielectric layer.

4. CONCLUSIONS

We appended the ONO deposition process to the beginning of the 0.25 μm embedded SONOS process before all of the logic well implantation processes in order to maintain the characteristics of the basic CMOS logic technology. This caused severe ONO rupture failure. We postulated that the ONO rupture failure originated from the ONO implantation damages and prepared two kinds of samples to investigate this issue: one sample was processed with the current embedded SONOS process and one sample was processed with a new embedded SONOS process in which all of the logic well implantations were performed before the ONO deposition process. Through these investigations, we demonstrated that the ONO implantation damage was the root cause of the ONO rupture failure in the current embedded SONOS process.

According to the implanted ion's energy loss model, both the Vt adjustment implantation and the punch-through implantation mainly caused the displacement damages in the block oxide, trap nitride, tunnel oxide as well as in the silicon surface through nuclear collisions in the current embedded SONOS process.

Consequently, we can obtain an ONO rupture free embedded SONOS process with a very good and reliable ONO quality if we only transfer all of the logic well implantation processes from after the ONO deposition process before the ONO deposition process.

REFERENCES

[1] M. H. White, D. A. Adams, and J. Bu, IEEE Circuits and Devices Mag. **16**, 22 (2000) [DOI: 10.1109/101.857747].

[2] M. Boutchich, D. S. Golubović, N. Akil, and M. van Duuren, Microelectron. Eng. **87**, 41 (2010) [DOI: 10.1016/j.mee.2009.05.019].

[3] M. P. M. Jank, M. Lemberger, A. J. Bauer, L. Frey, and H. Ryssel, Microelectron. Reliab. **41**, 987 (2001) [DOI: 10.1016/s0026-2714(01)00053-1].

[4] S. Kumar and E. L. Russell, IEEE International Integrated Reliability Workshop Final Report (Lake Tahoe, CA 2001) p. 34 -40.

[5] K. Mameno, H. Nagasawa, A. Nishida, and H. Fujiwara, Nucl Instrum Meth Phys Res B **121**, 311 (1997).

[6] P. Chakraborty, S. S. Mahato, T. K. Maiti, M. K. Bera, C. Mahata, S. K. Samanta, A. Biswas, and C. K. Maiti, Microelectron. Eng. **86**, 299 (2009) [DOI: 10.1016/j.mee.2008.10.008].

[7] S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era, 2nd ed. (Lattice Press, Sunset Beach, 2002).

[8] J. H. Han, J. H. Kim, S. H. Lee, and C. Kim, Solid-State Electron. **49**, 1857 (2005) [DOI: 10.1016/j.sse.2005.10.006].