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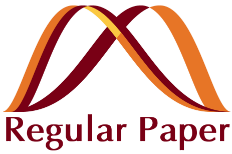

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Macro Modeling and Parameter Extraction of Lateral Double Diffused Metal Oxide Semiconductor Transistor

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High voltage (HV) integrated circuits are viable alternatives to discrete circuits in a wide variety of applications. A HV device generally used in these circuits is a lateral double diffused metal oxide semiconductor (LDMOS) transistor. Attempts to model LDMOS devices are complicated by the existence of the lightly doped drain and by the extension of the poly-silicon and the gate oxide. Several physically based investigations of the bias-dependent drift resistance of HV devices have been conducted, but a complete physical model has not been reported. We propose a new technique to model HV devices using both the BSIM3 SPICE model and a bias dependent resistor model (sub-circuit macro model).

Keywords: High voltage lateral double diffused metal oxide semiconductor, Gate-oxide thickness, Breakdown voltage, Metal oxide semiconductor SPICE, Metal-oxide semiconductor field-effect transistor

1. INTRODUCTION

High voltage lateral double diffused metal oxide semiconductor (HV LDMOS) devices are widely used in various applications, such as LCD drivers or RF devices. More recently, HV LDMOS devices have been used in complex analog circuits. Accurately modeling LDMOS transistors for circuit simulation is one of the most important aspects to be considered [1]. The modeling of LDMOS devices is complicated due to the existence of an lightly doped drain (LDD) region and an extended gate region [2]. The BSIM3 SPICE model is widely used as the best model for sub-micron MOS devices, but does not sufficiently model HV devices. In the absence of a suitable physical predictive compatible SPICE model for LDMOS transistors, it was decided to employ a more practical and flexible sub-circuit approach based on the widely used BSIM3 SPICE models [3]. Figure 1 shows the schematic structure of the LDMOS transistors used for 12, 30, 40 and 50 V applications with a gate-oxide thickness (Tox) of 300 Å, channel length of 1.8 μm and fabricated with a 0.3 μm CMOS technology.

The two key specifications of LDMOS transistors are a low on-resistance (Ron) and a high breakdown voltage (BV). However, these two parameters conflict with each other. For example, increasing the N-well dose not only cause the BV to increase, but also causes the Ron to increase. Device (a), by virtue of the presence of an N-buried layer, has a low Ron and low BV, whereas device (b) has a high Ron and high BV due to the reduced surface field (RESURF) effect.

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2. MODELING

2.1 Limitations of the conventional SPICE model

2.1.1 Quasi-saturation effect

As shown in Fig. 2, the drain current is limited to a certain extent at high gate voltages. This is referred to as the “quasi-saturation effect.” The conventional MOS SPICE model is incapable of modeling this effect, as can also be seen in Fig. 2. Process and device simulations were performed to examine the origin of this effect.

As shown in Fig. 3(a), by increasing V_{gs}, the depletion regions spread outwards and upwards from P-Body and P-Substrate and, therefore the current flow is confined to the undepleted regions. The flows of current through these regions cause the quasi-saturation effect.

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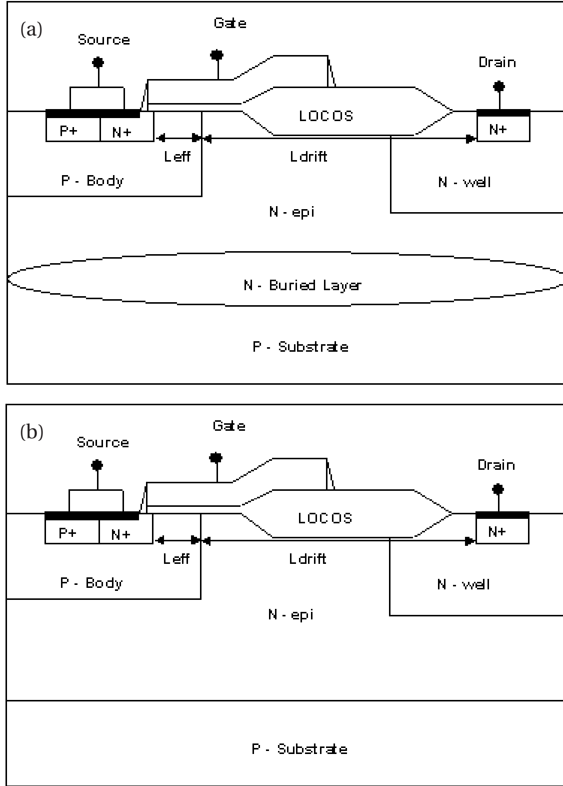

Fig. 1. Cross-section of LDMOS device (a) with N-buried layer and (b) without N-buried layer.

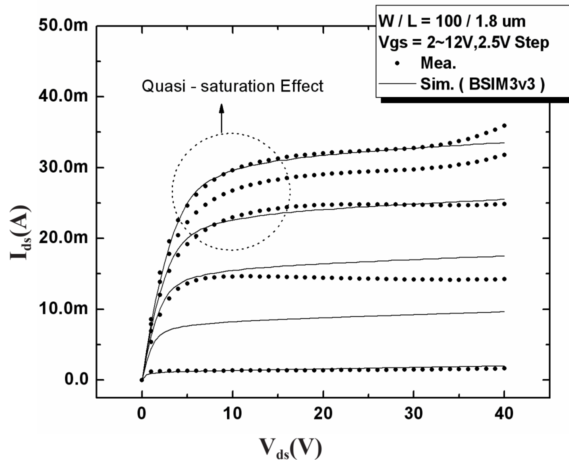

Fig. 2. Drain current vs. drain bias (I_d-V_{ds}) characteristics of an HV LDMOS obtained using the conventional MOS SPICE model.

2.1.2 Bias-dependant resistance

Figure 3(b) shows a simulation of the HV LDMOS transistor at a constant V_{gs}. The drift resistance increases with increasing V_{ds} due to the extension of the depletion region that is formed in the drift region. The current path in the drift regions extends with increasing V_{gs} at a constant V_{ds}. Therefore, the drift resistance must be a function of V_{ds} and V_{gs}.

2.1.3 Different I_d-V_{gs} characteristics

In general, the saturation drain current of a metal-oxide semiconductor field-effect transistor (MOSFET) is modeled by

$$\left.\begin{aligned} & I_{ds} \propto (V_{gs} - V_{th})^{a} \\ & 1 < a < 2 \quad \textit{for Short channel} \\ & a = 2 \quad\quad \textit{for Long channel} \end{aligned}\right\} \tag{1}$$

where V_{th} is the threshold voltage. We can find the value, “a,” viz. the slope of the line, from Fig. 4(b). As shown in Fig. 4(a), while V_{gs} is greater than V_{th}, the drain current of a short channel n-MOSFET increases linearly and that of a long channel n-MOSFET increases hyperbolically, whereas the drain current characteristics of an HV LDMOS are different from those of a conventional MOSFET. The conventional SPICE model is sufficient to model 1.8 V CMOS devices, but not for modeling HV LDMOS devices. Because R_{din} is a function of only V_{gs}, as shown in Eq. (2), the drain current of an HV LDMOS device increases complexly (where “a” is about 0.8), as shown in Fig. 2, and consequently the BSIM3 cannot model the quasi-saturation effect and its accuracy is poor. Therefore, we propose a sub-circuit macro model to overcome these limitations.

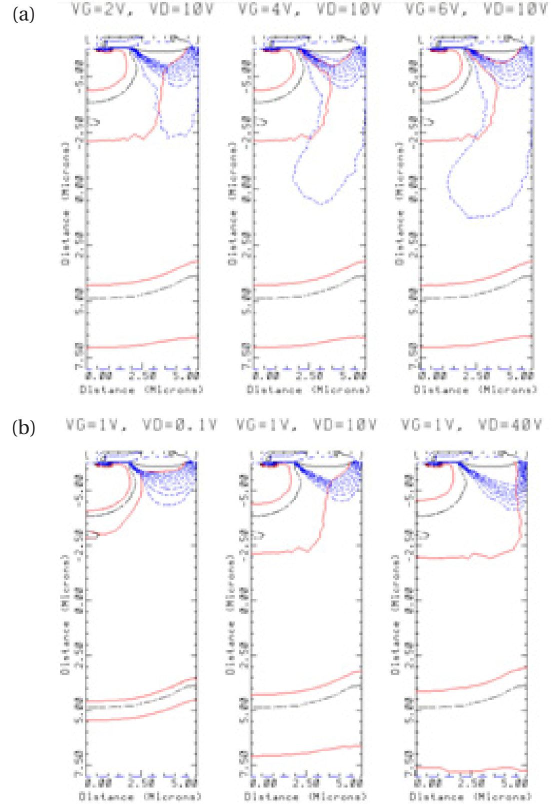

Fig. 3. Simulation of HV LDMOS device showing the limitation of the drain current at high gate voltages: current flow (blue dot line), depletion region (red line), junction interface (black line) (a) gate bias sweep with a fixed drain bias, (b) drain bias sweep with a fixed gate bias.

2.2 Macro modeling

The LDMOS sub-circuit model implemented in this work is shown in Fig. 5. R_{din}, as shown in Eq. (2), is the built-in bias dependent resistor model in BSIM3 and R_{dex} is the bias dependent resistor model of the drift region. We discuss the R_{dex} in this section. R_{din} is modeled by Liu et al. [4].

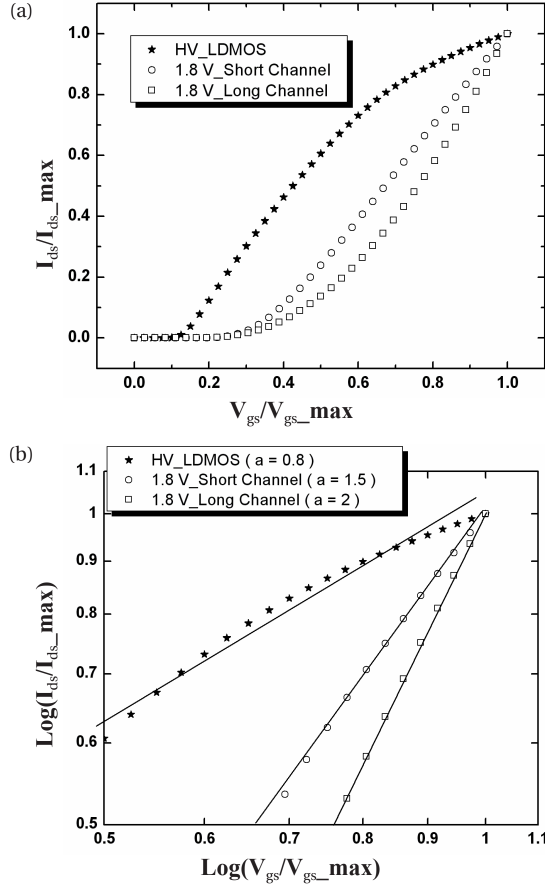

Fig. 4. Normalized drain current vs. gate bias (Id-Vgs) characteristics of 3 types of devices, Vds = Vcc (40 V for LDMOS, 1.8 V for MOSFET).

$$R_{din} = \frac{R_{dsw}(1 + Prwg * V_{gs})}{W} \qquad (2)$$

where Rdsw is the parasitic resistance per unit width, W is the channel width, and Prwg is the gate bias effect coefficient of Rdsw. As mentioned above, R_{dex} can be defined by Eq. (3), because the resistance of the drift region is dependent on V_{gs} as well as V_{ds}.

$$R_{des} \equiv f(W, T, V_{ds}, V_{gs}) \qquad (3)$$

We investigated the most appropriate mathematical formulations to describe R_{dex}. The following continuous mathematical expression is proposed for the drift resistance:

$$R_{dex} = \frac{100u + Wo}{W + Wo}(1 + TCR_{dex} \times (\frac{T}{25} - 1)) \times f(V_{gs}, V_{ds}) \qquad (4)$$

$$\begin{aligned} f(V_{gs}, V_{ds}) &= p0 + pg1 * V_{gs} + pg2 * V_{gs}^{2} + pg3 * V_{gs}^{3} \\ &+ pg1 * V_{ds} + pd2 * V_{gs}^{2} + pd3 * V_{ds}^{3} \\ &+ pdg11 * V_{ds} * V_{gs} + pdg12 * V_{ds} * V_{gs}^{2} \\ &+ pdg22 * V_{ds}^{2} * V_{gs}^{2} + pdg21 * V_{ds}^{2} * V_{gs} \end{aligned} \qquad (5)$$

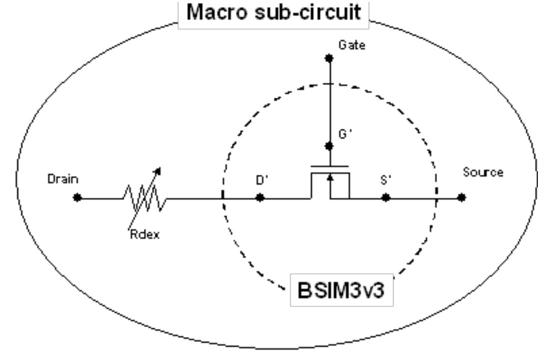

Fig. 5. Schematic of BSIM3 and macro sub-circuit models.

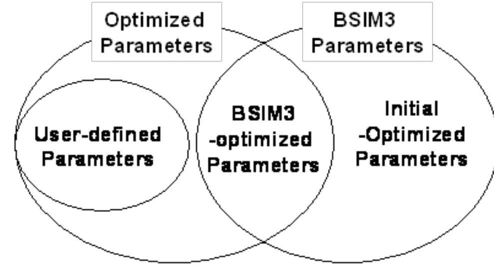

Fig. 6. Schematic of optimized parameters.

where T is the temperature, Wo is the width offset, pxxx is the bias coefficient for $V_{gs}[V_{ds}]$ and TCR_{dex} is the temperature coefficient for R_{dex}.

3. RESULTS AND DISCUSSION

This section describes how to optimize the parameters for the HV LDMOS devices. As shown in Fig. 6, there are three kinds of parameters in our sub-circuit model: the user-defined parameters, BSIM3-optimized parameters and initial-optimized parameters.

First of all, we extracted the initial-optimized parameters with parameter extraction tools such as UTMOST or BSIMProp+ [5], and then optimized the user-defined and BSIM3-optimized parameters. The user-defined and BSIM3-optimized parameters are listed in Table 1. We used the built-in optimizer in the circuit simulator, such as HSPICE or Smart-SPICE, to optimize these parameters. We also used the macro modeling routine in UTMOST. The latter method was more convenient than the former one, because all of the optimization work was performed in a GUI environment.

In the previous section, we described various strategies for the optimization of the parameters. The I-V characteristics that were simulated using our macro model with the optimized parameters are shown to validate the sub-circuit macro model. Figure 7 shows that the simulated I-V characteristics are well matched with the measured I-V data.

4. CONCLUSIONS

HV integrated circuits are viable alternatives to discrete circuits in a wide variety of applications. The HV device that is generally used in these circuits is the LDMOS transistor. In this work, we described the electrical characteristics of HV LDMOS devices and the limitations of the conventional SPICE model for

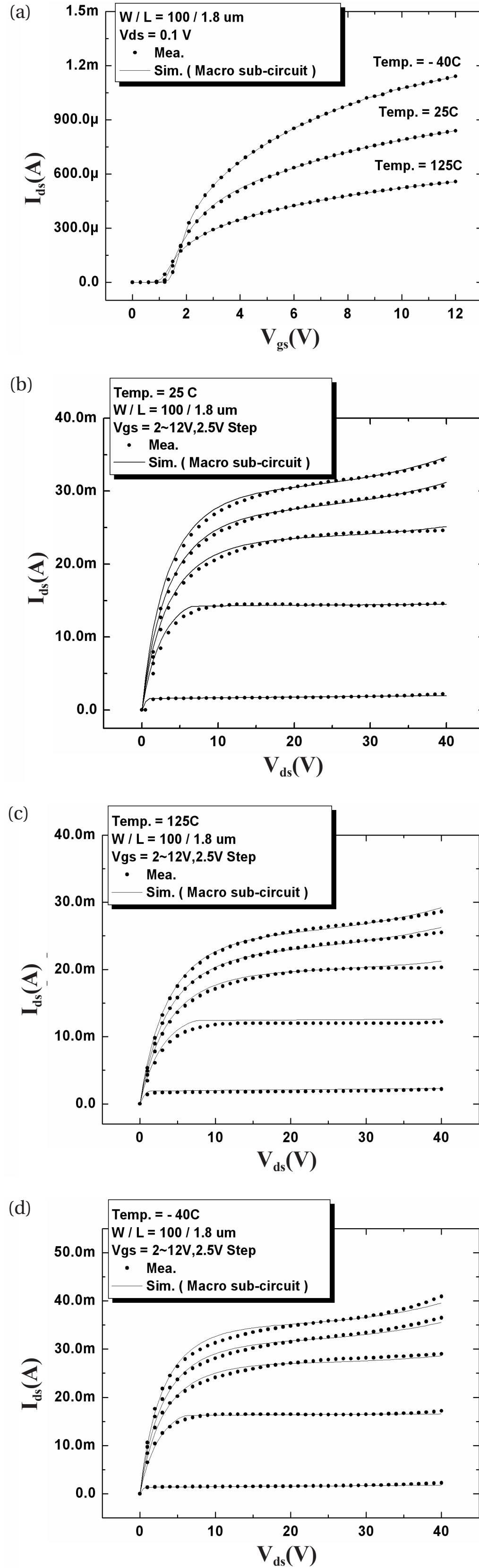

Fig. 7. Measured vs. modeled I-V characteristics, (a) I_d-V_{gs} data, temperature = -40°C, 25°C, 125°C, (b-d) I_d-V_{ds} data, temperature = 25°C, 125°C, -40°C.

Table 1. List of optimized parameters (user-defined parameters and BSIM3-optimized parameters).

Parameter	Description	Remark
vth0	Long channel threshold voltage	BSIM3-
dvt0	1st-coeff. short-channel effect on vth0	optimized
dvt1	2nd-coeff. short-channel effect on vth0	parameter
u0	Mobility at room temp.	
ua	1st-order mobility degradation coeff.	
vsat	Saturation velocity at room temp.	
prwg	Gate bias effect coefficient of rdsw	
rdsw	Parasitic resistance per unit width	
pclm	Channel length modulation parameter	
pvag	Gate dependence of early voltage	
p0	Offset resistance for Rdsx	User-
pg1	1st-coeff. Vgs	defined
pg2	2nd-coeff. Vgs	parameters
pg3	3rd-coeff. Vgs	
pd1	1st-coeff. Vds	
pd2	2nd-coeff. Vds	
pd3	3rd-coeff. Vds	
pdg11	1st-1st-coeff. Vgs and Vds	
pdg12	1st-2nd-coeff. Vds and Vgs	
pdg21	1st-2nd-coeff. Vgs and Vds	
pdg22	2nd-2nd-coeff. Vgs and Vds	
TCRdex	Temperature coefficient for Rdex	
W0	Offset width for Rdsx	

LDMOS devices. Attempts to model LDMOS devices are complicated dues to the existence of the LDD and the extension of the poly-silicon and the gate oxide. Several physically based investigations of the bias-dependent drift resistance of HV devices have been conducted, but a complete physical model has not been reported. The limitations of the conventional SPICE model can be overcome by using a macro model and, consequently, we proposed an accurate LDMOS macro model for circuit simulation. We also present a parameter extraction methodology for the LDMOS macro model. The proposed macro model can be used to obtain accurate circuit simulation results for LDMOS devices.

REFERENCES

[1] Y. S. Kim, J. G. Fossum, and R. K. Williams, IEEE Trans. Electron Devices **38**, 1641 (1991) [DOI: 10.1109 / 16.85161].

[2] J. Olsson, R. Valtonen, U. Heinle, L. Vestling, A. Soderberg, and H. Norde, IEEE International Conference on Microelectronic Test Structures (Goteborg, Sweden 1999) p. 135. [DOI: 10.1109/ ICMTS. 1999. 766231].

[3] D. Moncoqut, D. Farenc, P. Rossel, G. Charitat, H. Tranduc, J. Victory, and I. Pages, Proceedings of the 1996 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (Minneapolis, MN 1996 Sep. 29-Oct. 1) p. 216. [DOI: 10.1109/ BIPOL. 1996. 554651].

[4] W. Liu, X. Jin, J. Chen, M. C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Juang, R. Tu, P. K. Ko, and C. Hu, *BSIM3v3.2.2 MOSFET Model Users' Manual* (University of California, Berkeley, 1999).

[5] T. Myono, E. Nishibe, S. Kikuchi, K. Iwatsu, T. Suzuki, Y. Sasaki, K. Itch, and H. Kobayashi, IEICE Trans. Fund. Electron. Comm. Comput. Sci., 412 (2000).